BARCO

BARCO Projection Systems

SECTION W

service sheet

Noordlaan 5 B-8720 Kuurne - Belgium Telex 85.305 Tel. (056)36.82.11 Telefax (056)35.16.51

The video block diagram. This text gives a brief description of all units, used to achieve an analog amplified clamped video output, which in turn controls the CRT cathode.

The following units can be distinguished:

- 761773 The Controller.
It generates I2C control signals to select a certain video source and it also includes a text generator.

- 761749 The TTL input board.
It converts the digital incoming RGB (EGA/CGA) signal to an analog RGB output.

- 761748 The analog input board.
It makes a selection between the several input sources and clamps the green output, to insert text from the text generator.

- 761753 The Decoder.
It converts the video information (Video/sVideo) into a analog RGB signal. It also contains the clamp pulse shaper, the video output amplifying + clamping circuitry.

- 761750 The CRT driver.
It drives the cathode of the CRT

The controller. The heart of the digital projector is situated on the controller. It contains a 8088 uprocessor which gets its information out of an EPROM. The link with the several modules is established by using I2C communication, generated in a peripheral interface IC3. The controller unit contains also a text generator which adds text (control bars, warnings, menus) on the screen. The generators output consists out of a RGB and a control signal for Inserting text.

The TTL input unit This unit receives a digital RGB input signal. It's generated by a computer and can be in CGA as well as EGA format. The modules output consists of current sources. The module is selected by the +TTL signal, coming from the analog input module.

The RGB analog input unit.

Its major task is making the choice between the several input sources

- TTL source
- Video source (luminance together with chrominance)
- SVHS source (chrominance separated from luminance)
- RGsB source
- RGBs source

The different sources are fed to differential amplifiers. Their current source is controlled by a switch (in fact switching transistors) which in turn is manipulated by the controller. The controllers I2C information is translated in a serial-parallel converter. Its outputs are used to control the different switches.

If the video information (VHS or SVHS) is selected, the video signal output is fed into the decoder module to attain an analog RGB signal. First of all the chrominance filtered out of the VHS signal. Afterwards the chrominance is separated into R-Y and B-Y signals by means of a TDA 4555. These signals, together with the luminance signal (Y) are amplified later on in the TDA 4565. At last the analog RGB signals are generated and delivered back to the RGB analog input module.

Each color output (R,G,B) of the selected source can be turned off, on controllers demand.(eg. for adjustment purpose)

When an information text, from the internal text generated, has to be added to the screen the Insert signal (I) becomes high. It pulls the external video information down and clamps the green output to be able to reinstall the right black level. The text information is added afterwards. The analog RGB output is amplified and clamped on the three colors afterwards an fed to the respective CRT cathode drivers.

The blanking generator on the Decoder unit.

First of all the vertical blanking, generated on the vertical subunit, is used.

On the other hand, the horizontal blank is built up out of a capacitor which is forced to discharge through a transistor. The transistor is controlled by the sand-castle pulse (from vertical deflection unit) in case a video source is selected. Otherwise the horizontal flyback pulses (from the hor. defl. unit) are used instead. The capacitor voltage is fed to two OPAMPS to achieve left and right blanking. The among of blanking is adjusted by two digital potentiometers in IC5.

The CRT driver

Its major task is to charge or discharge the cathode capacitance to control the brightness of the CRT spots, making use of its input signal.

TTL INPUT BOARD 76 1749

FPLA
CGA/EGA

BLUE 1
BLUE 5
GREEN 15
GREEN 7
RED 14
RED 12
+TTL

R G B
2 4 6

CONTROLLER BOARD

2864
EEPROM
IC8

8256
PERIPHERAL
INTERFACE
IC3

8088
MICROPROCESSOR
IC2

6264
TEXT RAM
IC38

74166
PAR/SER CONVERTER
IC34

SCL SDL

5 6 3 1
I R G B

K K K

RGB DRIVER RGB DRIVER RGB DRIVER

B 3 5 BLK G 3 5 BLK R 3 5 BLK

INPUT INSERT BOARD 76 1748

+12V
4

SVHS
+SVHS
VIDEO
+VIDEO
TTL
+TTL
+RGB
RGB
RGBS

SER/PAR
DECODER

CLAMP 1

VER SYNC OUT 2
VER SYNC IN 21 22
HOR SYNC OUT 4
HOR SYNC IN 17 18
INPUT RED 13 14
INPUT GREEN 5 6
INPUT BLUE 1 2
VIDEO INPUT 25 26
LUMINANCE 7 6
CROMINANCE 13 12

R Q203
G Q303
B Q403
COLOR ON/OFF

INSERT Q404

INSERT
Q202 B
Q302 G
Q402 R

CLAMP

FROM TEXT
GENERATOR

LM 1203

CLAMP

1
4
7

4
6

DECODER 76 1753

3
21

TDA 4555
CROM

-(R-Y)
-(B-Y)

TDA 4565

Y

-(R-Y)
-(B-Y)
Y

DEMATRIX

B G R

+5V
-7V

+5V
VIDEO
-7V

V_BLANK
LP SC

The vertical deflection block diagram

As shown on the diagram the vertical raster circuitry is composed of several sub units outlined by dashed lines.

The following units can be distinguished:

-S761765 The NS-correction unit (+ horizontal shift board)
It generates a sawtooth and parabolic wave form on horizontal line frequency for NS correction purpose. It also couples the NS-correction inductive to the deflection current.

-S761758 The NS-subunit
The geometric corrections are adjusted here, using the wave forms, generated on the NS-unit.

-S761768 The vertical deflection board
It contains an auto-locked oscillator which generates a sawtooth on vertical line frequency and three output amplifiers for the vertical deflection coils.

-S761769 The subunit vertical deflection
The DC output shift-current is adjusted here using IC5. It also generates the EW corrections and the top,bottom blanking.

-S761775 The main frame
Most of the connections between the several modules are implemented on the main Frame. It also contains the inversion switches.

The Vertical oscillator

The vertical oscillator is composed of C13,C14,Q3 and Q8. The capacitors charge to a certain vertical hold level, adjusted by a potentiometer. From that moment on Q3 and Q8 (= a FET configuration) conduct and discharge the capacitors immediatelly.

The horizontal/composit sync ,comming from the RGB analog input module 761748 (including video or luminance or int.hor sync or TTL hor sync or separated hor/comp sync), is fed into a video sync separator (2595) which delivers a composite sync output. It's integrated afterwards ,to neglect the horizontal sync pulses, and forces C13,C14 to discharge immediatelly which results in a synchronized vertical oscillator. The vertical hold potentiometer can be used to adjust the free running oscillator frequency by changing the vertical hold level.

A second way for synchronizing the oscillator ,which has the priority, can be achieved using an external separate vertical sync signal or the internal vertical sync which is also available on the RGB analog input board 761748.

The oscillator output signal can be linearised using a feed back signal which is mainpulated by a digital potentiometer (marked with B: = Barco designed IC). That output is amplitude controlled afterwards, which in turn is fed into three separated vertical output amplifiers.

The DC output current is installed by three digital potentiometers (marked B) ,situated on the subunit in Ic5. It's used to shift the picture vertical. The output stages are connected to the inversion switches which in turn are connected to the deflection coils.

NS-Corrections

On the other hand, some corrections have to be added to the deflection current to correct the Top and Bottom bow and keystone errors. Therefore we generate a sawtooth, its inverse and a parabolic waveform, on horizontal scan frequency using the horizontal flyback pulses (350V PU) comming from the horizontal deflection board. The parabolic wave is achieved by multiplying the sawtooth with itself in a 1496 Ic. These three waveforms are fed to the NS-subunit to be demultiplexed.

Due to the OPAMP (Ic4) configuration, the gate of the demultiplexer is set during the top part of the screen and reset during the bottom half screen part. The OPAMP gets therefore +6V on the non inverting input and the vertical sawtooth (VDB = vertical deflection blue) on the inverting input.

The demultiplexer outputs are manipulated by four potentiometers of Ic200(red),respective Ic201(blue) and 202(green). Two for the top and two for the bottom corrections. The common output is modulated on the vertical sawtooth (VDB) afterwards using Ic40,60 and Ic20. The modulator output current is then inductive coupled using a transformer ,in series with the deflection coil.

Three scan fail detections are included, to detect a failing vertical deflection output.

VERTICAL DEFLECTION

NS-CORR 761765

VERTICALBOARD 761768

MAIN FRAME 761775

NS-SUBUNIT 761758

VERT.OSC

IC280

IC281

IC282

40538 DMUX

GATE

MULTI-PLEXER MCM96

BOT. KEYSTONE

TOP. KEYSTONE

BOT BOW

TOP BOW

SHIFT

VER SUBUNIT

INVERTION

VER DEFL COIL

VERT HOLD

50 / 60 HZ DETECTOR

VIDEO INPUT / COMP SYNC

VER SYNC IN

VER AMPL

SCAN FAIL

The horizontal deflection diagram.

This diagram explains the horizontal deflection and all units needed to achieve a correct synchronized deflection.

The following units are implemented:

-761768 The vertical deflection board.
It generates the drive pulses for the horizontal oscillator

-761769 The vertical deflection subunit.
The EW and vertical midline bow and skew (using phase) corrections are derived here.

-761766 The horizontal deflection unit.
It includes the horizontal oscillator which is controlled by the drive pulses, and several protection circuits.

-761765 The NS-correction board.
It's used only to manipulate the DC-current in the horizontal deflection coils to achieve a horizontal shifting picture.

-761775 The main frame.
Most of the connections between several modules are implemented on the main frame. The inversion switches are also mounted on the frame circuit.

The drive pulses

The horizontal/composite sync, coming from the RGB analog input module 761748 (including video or luminance or int.hor.sync or TTL hor. sync or separated hor/comp sync), is fed into a video sync separator circuit 2595 as already mentioned in the vertical deflection description.

The 2595 includes a horizontal oscillator which must be tracked with the horizontal sync pulses. The internal phase comparator range is only 680 Hz, so larger frequency changes must be corrected with an external frequency correction circuit.

This is achieved by using two phase comparators. When the internal oscillator frequency gets too high, the PLL IC6 output becomes higher and activates Q9 through Ic7 .The PLL output adjusts the oscillator through the conducting Q9.

On the other hand, when the internal frequency gets to low, the comparator Q17,Q18 will become low and Q9 will be activated again through Ic7. The PLL output will be able to adjust the oscillator again.

The synchronized horizontal pulses are converted to driving pulses by two one shots (IC5) and can be phase shifted by modifying the time constant of the first one shot.

The horizontal deflection oscillator.

The oscillator itself is described in detail in the text of module 761766 and isn't repeated here. It uses two mosfet switches, a recuperation capacitor C33 ,the diodes implemented in the mosfets, the deflection coil and a parallel capacitor. The drive pulses are used to control the mosfets.

The oscillator output is connected to the deflection coils through the inversion switch situated on the frame , together with a DC-shift current. The green shift signal is also fed to the Red and Blue circuit to attain a better Red on Green and Blue on green shift. The horizontal scan width of the three CRTs separately adjusted by means of the HOR WIDTH variable coils.

Protections.

The current through the mosfets is measured by taking the voltage over a wire resistance. The voltage controls Q21 which in turn activates a mono-flop. Its output pulls the drive pulses down.

Whenever the D-S voltage of the mosfets becomes dangerous high the output of Ic1 gets low and pulls the drive pulses down. This is nonreversal due to the feed back diode which locks Ic1.

A scan fail detection is also adapted to each CRT output

Power supply

The power supply situated on the horizontal deflection board is used to generate a 1000V voltage. It's used to protect the mosfets against a too high D-S switching voltage.

Geometric corrections

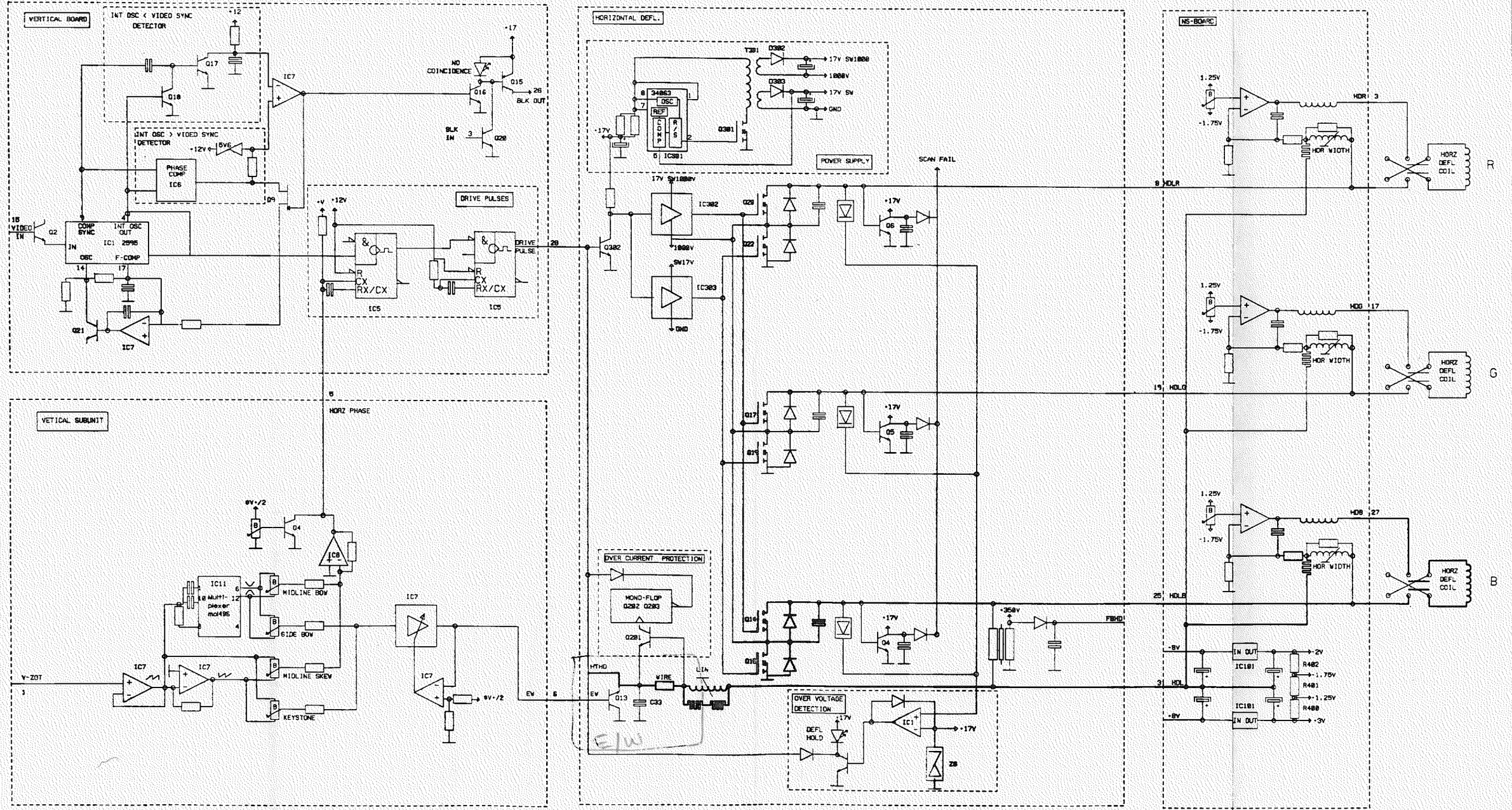
To correct the different geometric errors, the deflection current has to be modified. The vertical sawtooth, coming from the vertical oscillator, is fed twice in a multiplier Ic11 to generate a parabolic wave form on vertical raster scan.

The sawtooth and its inverse is used to correct the vertical midline skew, by modifying the phase of the driving pulses. The vertical keystone correction (EW) uses the same sawtooth signals but modifies the amplitude of the deflection current.

Bow corrections are similar achieved but use the parabolic wave form instead

To achieve an equal correction on several line frequencies, we have to modify the amount of correction. This is done by using the frequency dependent voltage $V+, which is derived of the HTHD voltage on the horizontal deflection board.

HORIZONTAL DEFLECTION



BARCO

BARCO Projection Systems

SECTION X

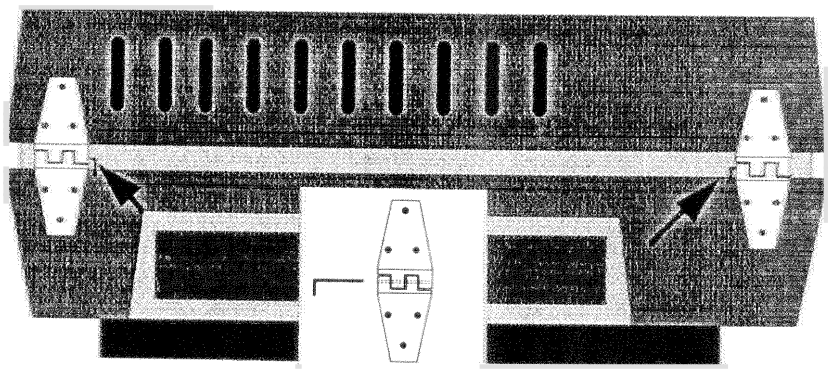
service sheet

Noordlaan 5 B-8720 Kuurne - Belgium Telex 85.305 Tel. (056)36.82.11 Telefax (056)35.16.51

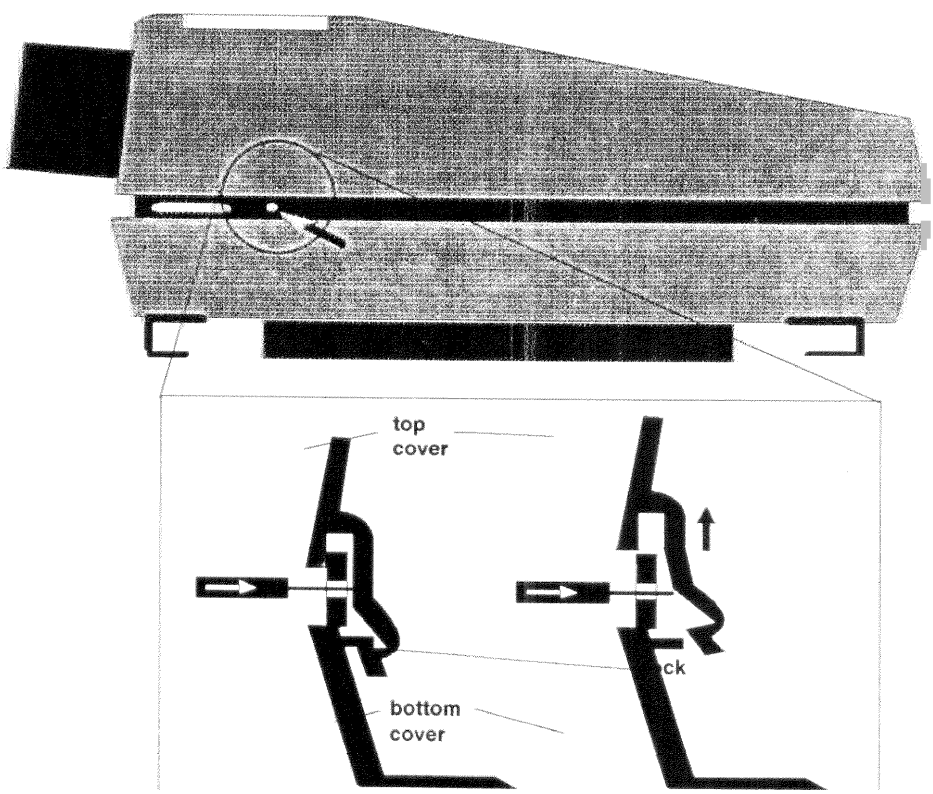
Cabinet Removal

Top cover removing

Pull out the two hinge-joints at the rear of the projector



Unlock the top cover from the bottom cover by pushing the lock on both sides of the cabinet by means of a screwdriver

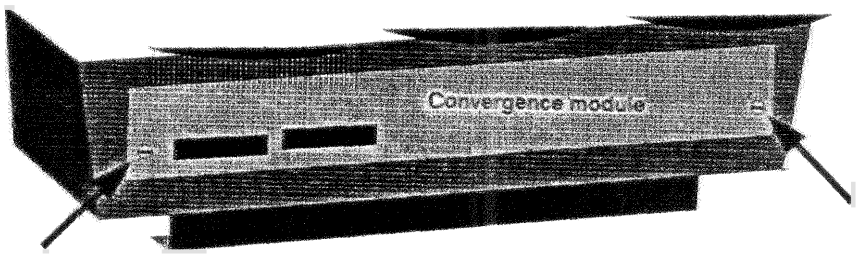


Bottom cover removal

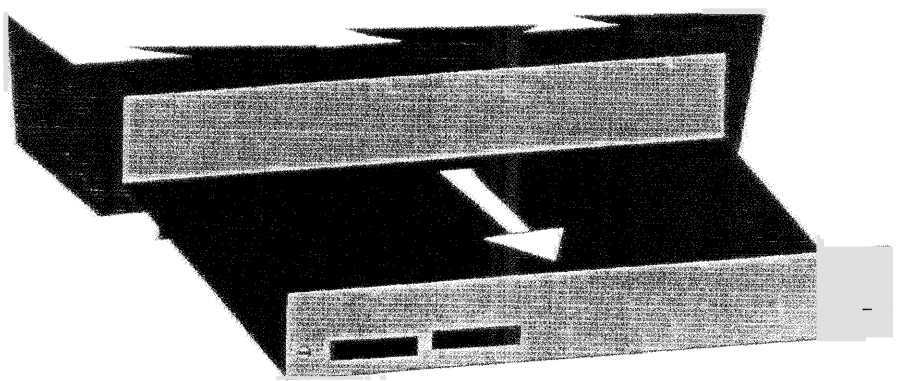
Remove the convergence module

Loosen the board fixation screws on both sides of the Convergence module

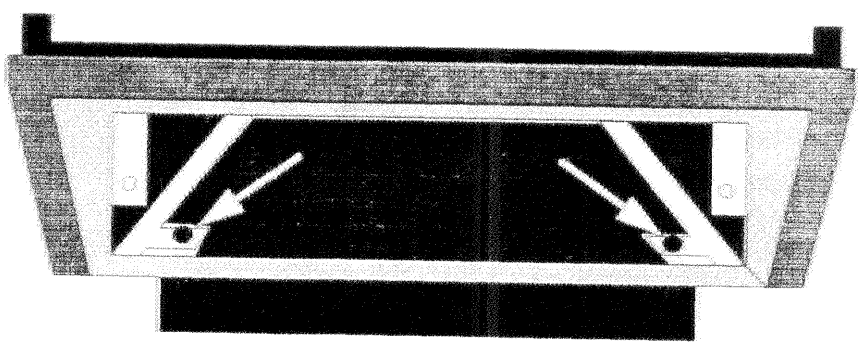
Front view projector



Pull out the Convergence module



Remove the two bolts inside the projector, at the left and the right side, which secure the bottom cover to the projector support.

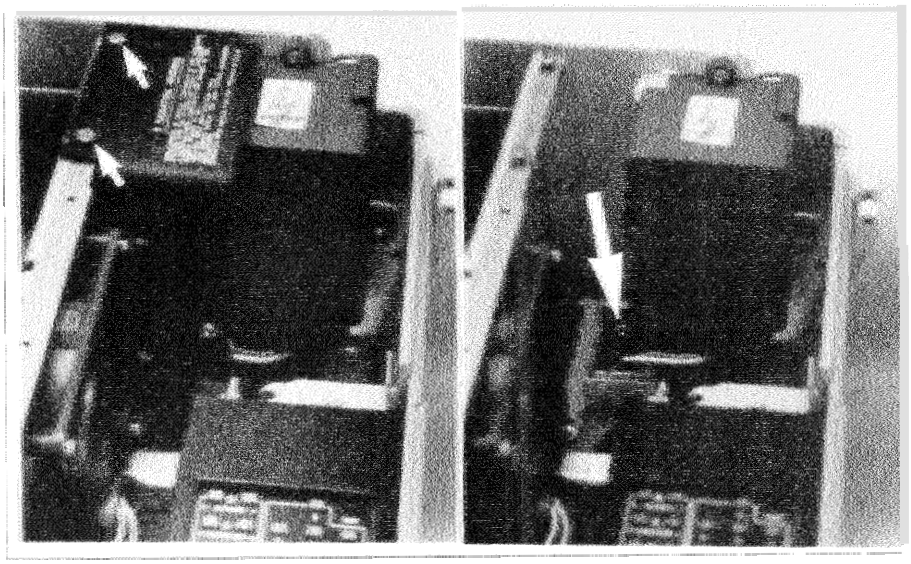


For the same purpose as before, two bolts are provided at the rear side of the projector. To have access to one of the two bolts, the EHT module has to be removed.

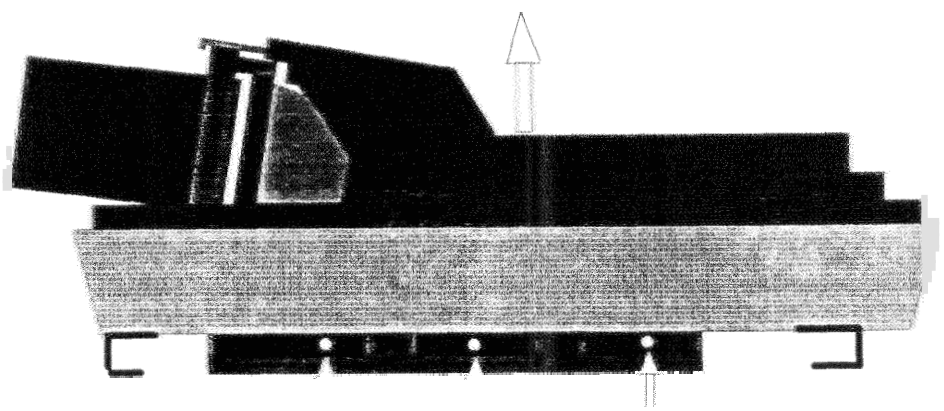
Remove the two screws which secure the heatsink plate of the EHT board to the metallic main frame.

Pull the EHT module upwards to release the module connector from main frame connector.

Remove the two bolts , at the left and the right side, which secure the bottom cover to the projector support.(nutdriver 8mm).



Remove the three bolts, on each side of the projecor, which secure the metallic main frame to the projector support.



Lift projector assembly out of bottom cover

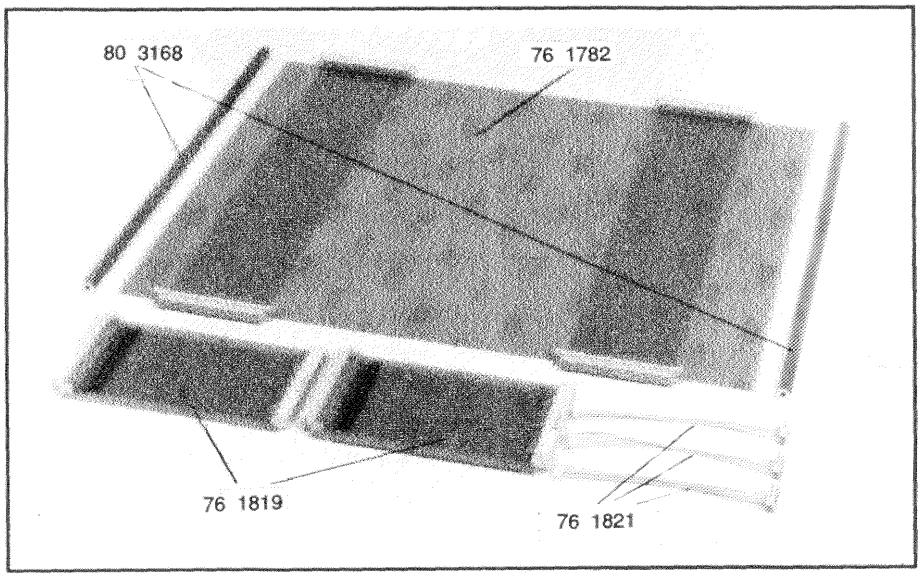
SERVICE KIT 98 27600

Introduction

Repairing the Barco 800 series projectors on component level is made posible by using the extension boards and the extensions cable units, delivered as **service kit**.

Contents of the kit:. **Order No. kit: 98 27600**

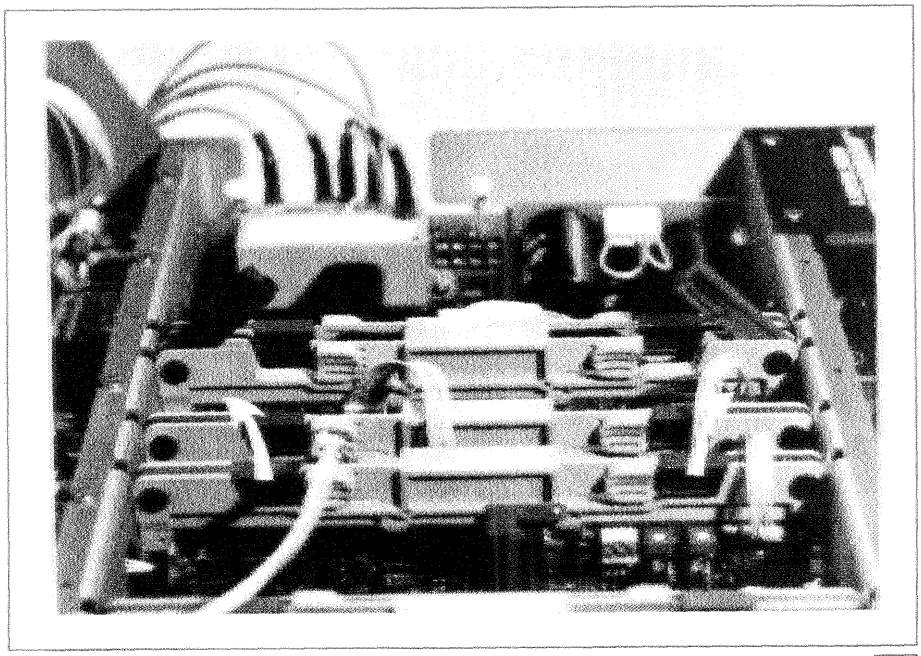
2 Extension boards for Euro cards:	Art. No. 76 1819
1 Extension board for Convergence module:	Art. No. 76 1782
2 Extensions metallic supports	Art. No. 80 3168
3 Extension cable units:	Art. No. 76 1821



Using the extension boards for Euro cards

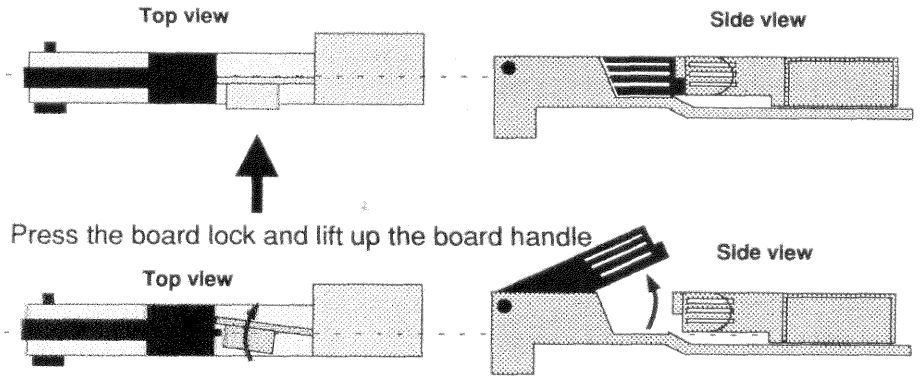
How to extract a module

Each board is locked in the main chassis on both sides



To unlock the board, proceed as follows:

Refer to illustration:



Repeat this action on both side of the module and extract the module out of the main frame.

Example: repairing the decoder module

Unplug the two connection cables to and from the Decoder module

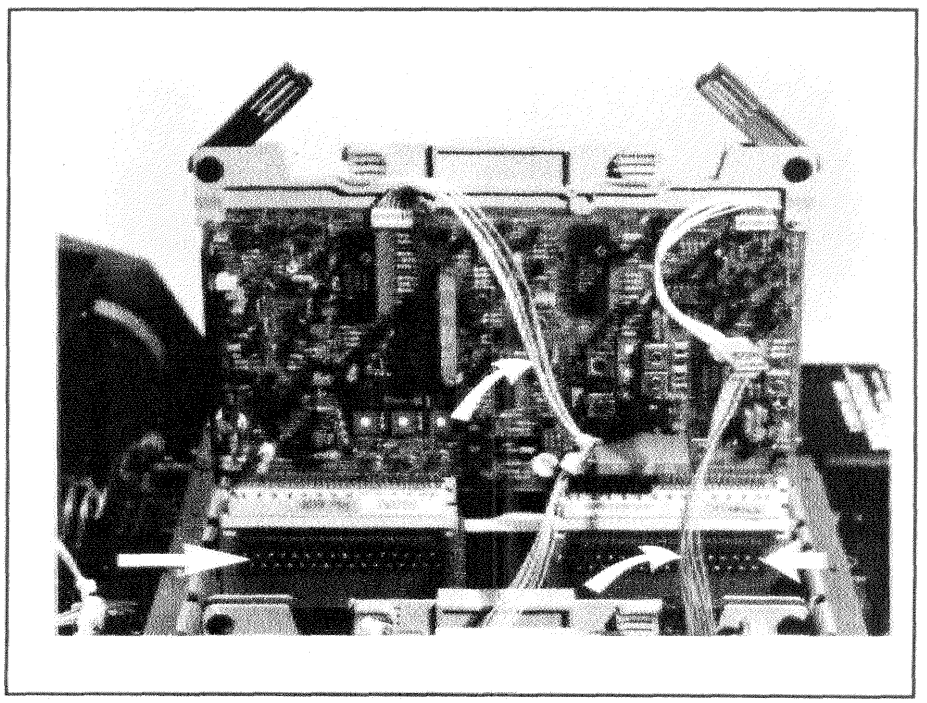
- Remove the Decoder module out of the main frame as already described.

- Plug the extension boards on the two decoder board connectors on the main frame.

Put the Decoder module on the extensions boards

- Reinstall the cable connection by inserting the extension cables.

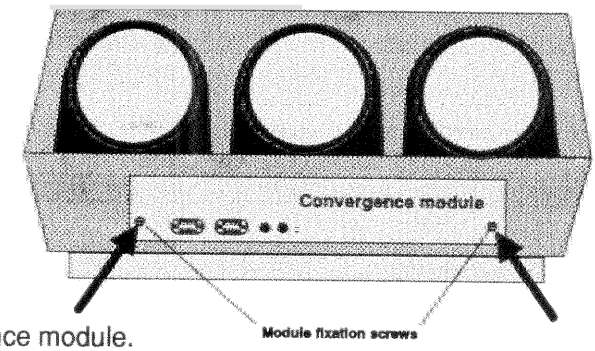
Important: the extension board for Euro card is provided on each printed circuit foil with a measure contact.



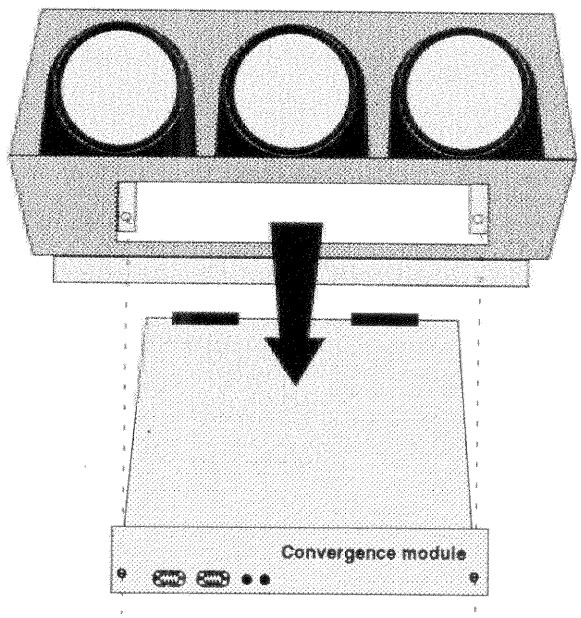
Using the extension board for the Convergence module

Removing the convergence module:

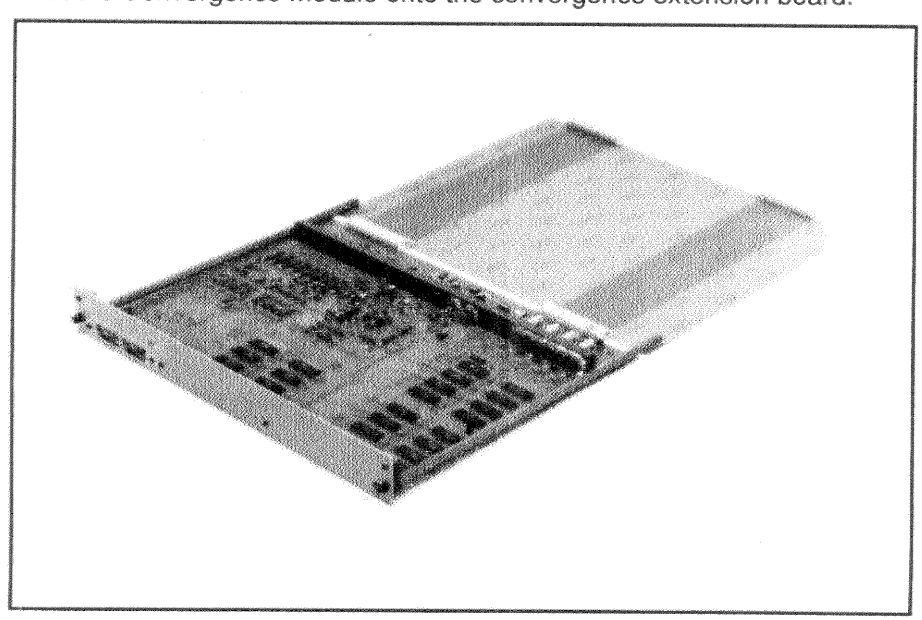
- Loosen the board fixation screws on both sides of the Convergence module.



- Pull out the Convergence module.



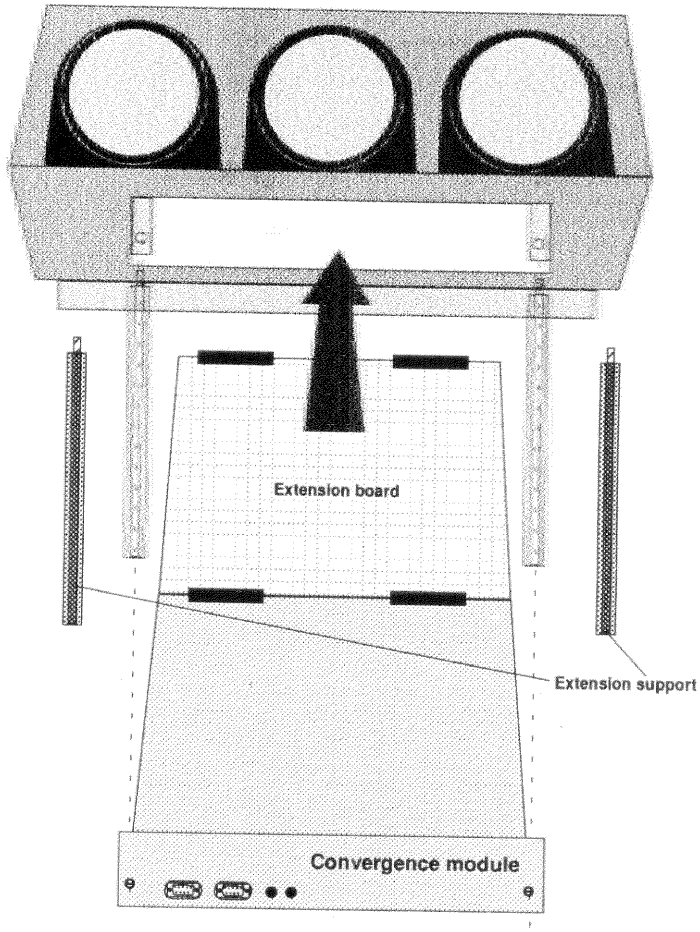
- Put the Convergence module onto the convergence extension board.

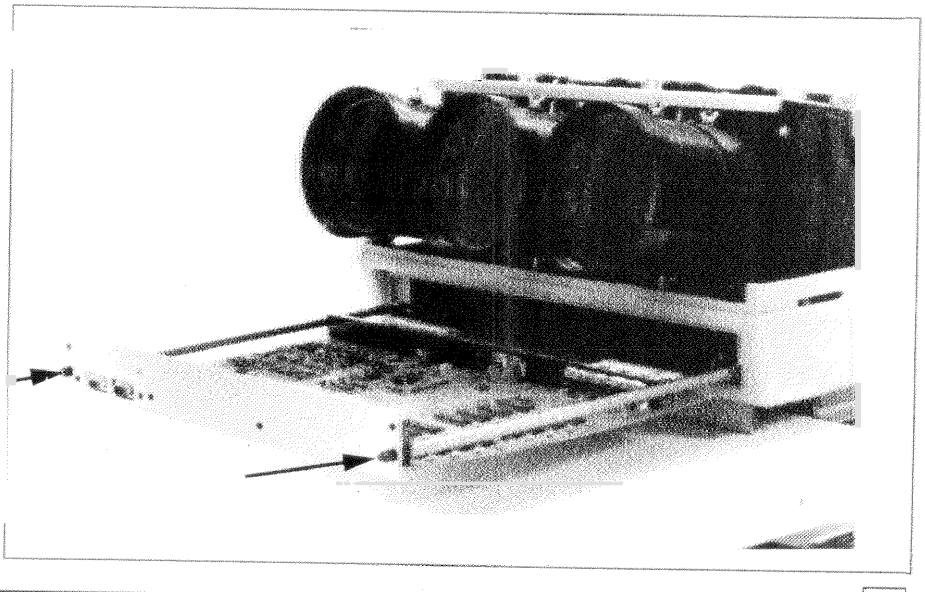


- Screw in on both side on the main frame the metallic extension supports.

- Slide the extension board with the plugged in Convergence module into the projector.

Secure the Convergence module onto the supports by screwing in the two remaining board screws.





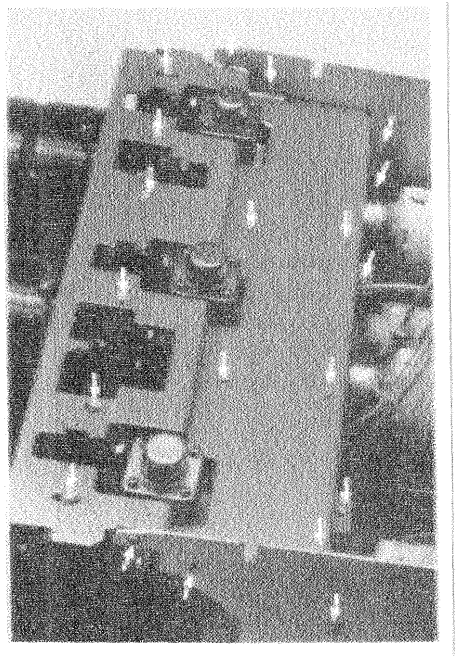
WARNING : CRT HANDLING

The picture tube encloses a high vacuum and care must be taken not to bump or to scratch the picture tube as this may cause the tube to implode resulting in personel injury and property damage. Shatter-proof goggles must always be worn by individuals while handing the CRT or installing it in the projector. Do not handle the CRT by the neck.

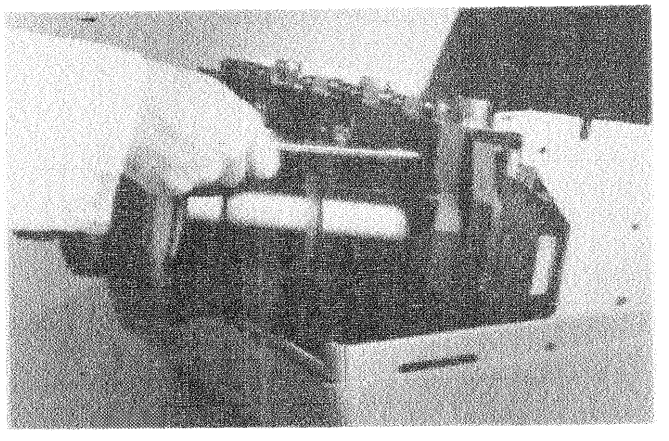
Mechanical disassembly

1. Top cover removal (see installation manual)
2. - Loosen the retaining screws on both sides of the controller module.
   - Turn this module 90°.
   - Secure this position with the retaining screws.

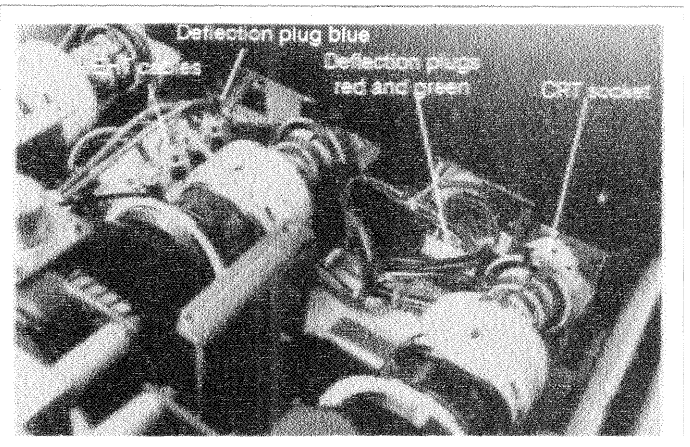
3. Remove the CRT cover plate by :
   - turning out the 20 bolts (nutdriver 7 mm and 8 mm)
   - Remove the cover plate by lifting up.



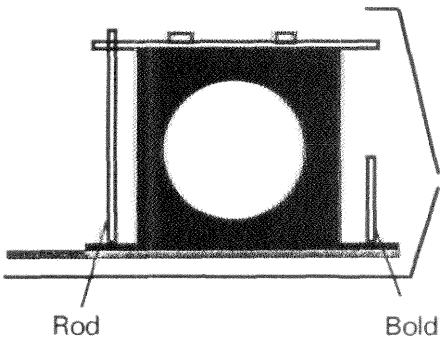
4. Remove the lens of the defective tube by :
   - supporting the lens by hand when removing the bolds.
   - turning out the 4 bolts of this lens (nutdriver 8 mm).
   - sliding the lens to the front of the projector.



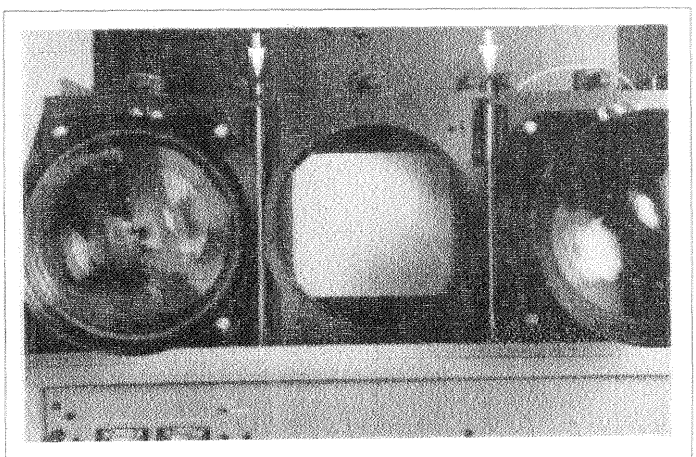
5. Electrical disconnection of:
   - EHT cables by turning the cap anti clockwise to unlock.
   - black groundwire connected to the CRT socket (not visible on image)
   - deflection plug.
   - CRT socket by pulling back the CRT socket off of the end of the CRT.



6. CRT unit removal :
   For Red and Blue :
   - turn out the bold, securing the CRT block to the main frame (see drawing).
   - unscrew the rod on the other side of CRT block and pull it out.
   - take out the defective tube.

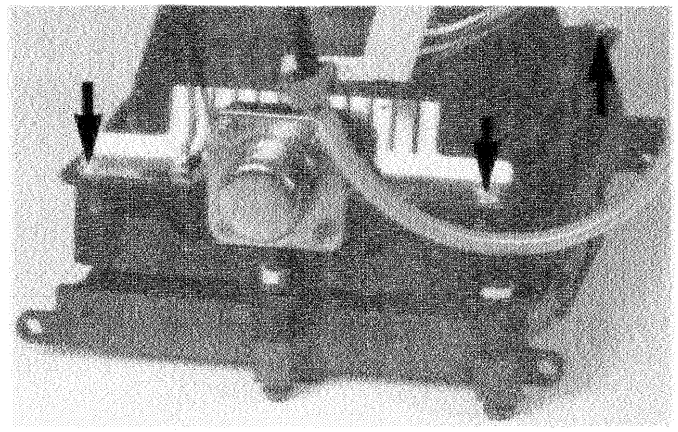


For Green :
- unscrew the rods on each side of the green tube.
- pull out both rods.
- take out the defective tube.



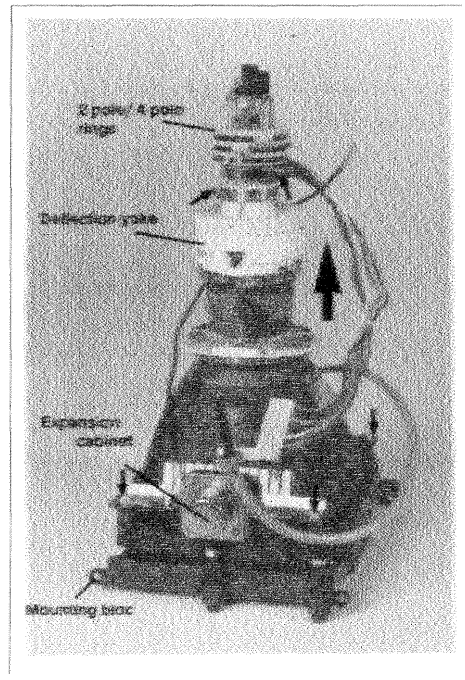
CRT unit disassembly

7. Remove CRT mounting block by screwing out the 4 bolts (nutdriver 8 mm).



8. Loosen the 2pole/4pole magnetic ring retaining screw.
   Slide off the 2pole/4pole magnetic ring of the end of theCRT.

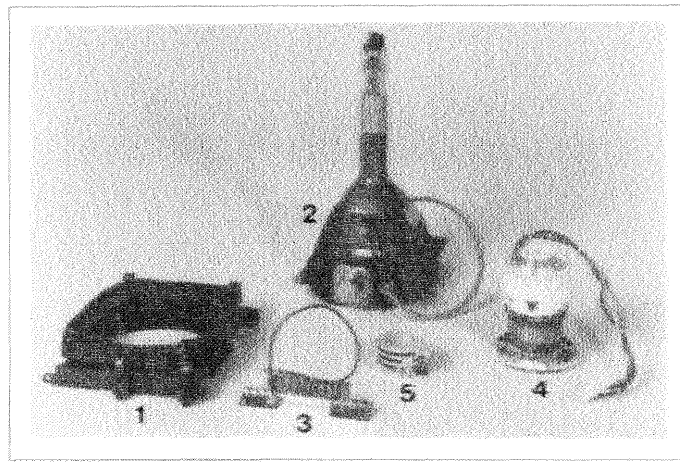
9. Loosen the deflection yoke retaining screw.
   Slide off the deflection yoke of the end of the CRT



Re-assemble the new tube.

10. - slide carefully the deflection yoke <4> over the neck of the CRT <2>. Take care that the deflection wires are on the same side of the EHT connection.
    - secure the retaining screw.
11. - slide now carefully the 2pole/4pole magnetic ring <5> over the neck of the CRT, against the deflection yoke.
    - secure the retaining screw.

12. - place the tube <2> in the mounting block with the expansion tank to the top of the mounting block <1>.
    - positioning the akwadag plate <3>.
    - screw in the 4 screws.



13. Place the CRT unit in the projector. Expansion tank to the top.
Insert the fixation rodsand secure the side bolds (only for red and blue tube).
(see image next to item 6)

14. Re-install the electrical connections :
(see image next to item 5)
- EHT cable
- CRT socket
- deflection plug and black ground wire

15. Mount the lens and secure the four bolds

16. Put back the CRT cover plate and secure with the 20 bolds

17. Put in place the controller module

ADJUSTMENT PROCEDURE AFTER REPLACING A PICTURE TUBE

* Adjustment procedure valable for the three tubes, green, red and blue
- Raster centering (see owner's or installation manual)
- Lens focusing (see owner's or installation manual)
- Left-right, top-bottom focusing (see owner's or installation manual)

* Adjustments only for red and blue tube.
- Adjust the main shift adjustments on the Vertical deflection + sync module and North-south corrections module. (see procedure on the respective service sheet)
- CRT projection angle adjustment (see owner's or installation manual).

Adjustment of the 2 pole/4 pole magnet ring. (The adjustments have to be done separately for each CRT)

See Section CRT unit. Section I

BARCO

BARCO Projection Systems

SECTION Y

service sheet

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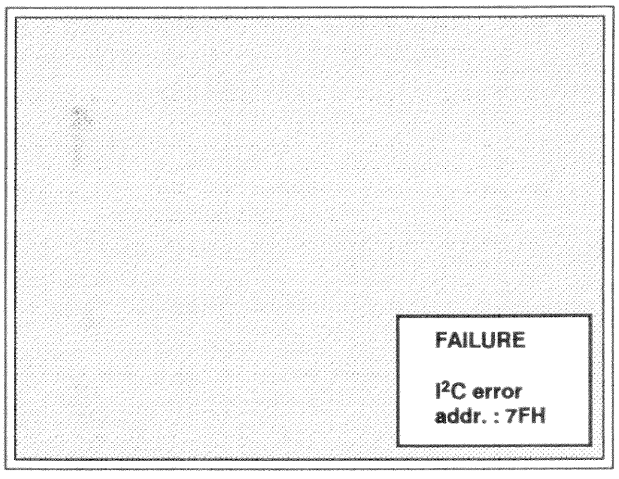
I²C error is displayed on the screen together with the respec tive address,as illustrated on screen picture:

The table below indicates which IC corresponds to the displayed address . Replacement of the indicated IC solves the I²C error.



Convergence module 761772

HEX address	IC	CORRECTION Red/Blue vert./hor.	ZONE
C0H	IC57		1
C2H	IC58		2
C4H	IC45		3
C6H	IC59		4
C8H	IC60		5
CAH	IC49		6
CCH	IC50		7
CEH	IC46		8
D0H	IC51		9
D2H	IC52		10
D4H	IC41		11
D6H	IC42		12
D8H	IC43		13
DAH	IC44		14
DCH	IC53		15
DEH	IC54		16
E0H	IC47		17
E2H	IC55		18
E4H	IC56		19
E6H	IC61		20
E8H	IC62		21
EAH	IC48		22
ECH	IC63		23
EEH	IC64		24

HEX address	IC	CORRECTION Green vert./hor.	ZONE
40H	IC605		22 3
42H	IC606		8 17
44H	IC60		13 12

1	2	3	4	5
6	7	8	9	10
11	12		13	14
15	16	17	18	19
20	21	22	23	24

46H	IC60	14 11
48H	IC607	6 15
4AH	IC608	7 16
4CH	IC609	9 18
4EH	IC610	19 10
50H	IC613	4 23
52H	IC614	5 24
54H	IC611	20 1
56H	IC612	2 21

Vertical deflection + sync module 76 1768

HEX address	IC	CORRECTION
F2H	IC3	top blanking vertical shift red vertical shift green vertical shift blue
F4H	IC2	
F6H	IC1	keystone skew bow vertical centerline bow

N-S corrections + hor. shift 76 1765

HEX address	IC	CORRECTION
F8H	IC200	top bow red bottom bow red top keystone red bottom keystone red
FAH	IC201	top bow green bottom bow green top keystone green bottom keystone green
FCH	IC202	top bow blue bottom bow blue top keystone blue bottom keystone blue
FEH	IC203	centerline bow blue centerline bow red centerline bow green horizontal amplitude
F0H	IC400	horizontal shift red horizontal shift green horizontal shift blue not used

Quad decoder module 76 1753

HEX address	IC	CORRECTION
58H	IC3	saturation R-Y saturation B-Y tint sharpness
		contrast brightness blanking left blanking right

RGB in + RGB switching module 76 1748

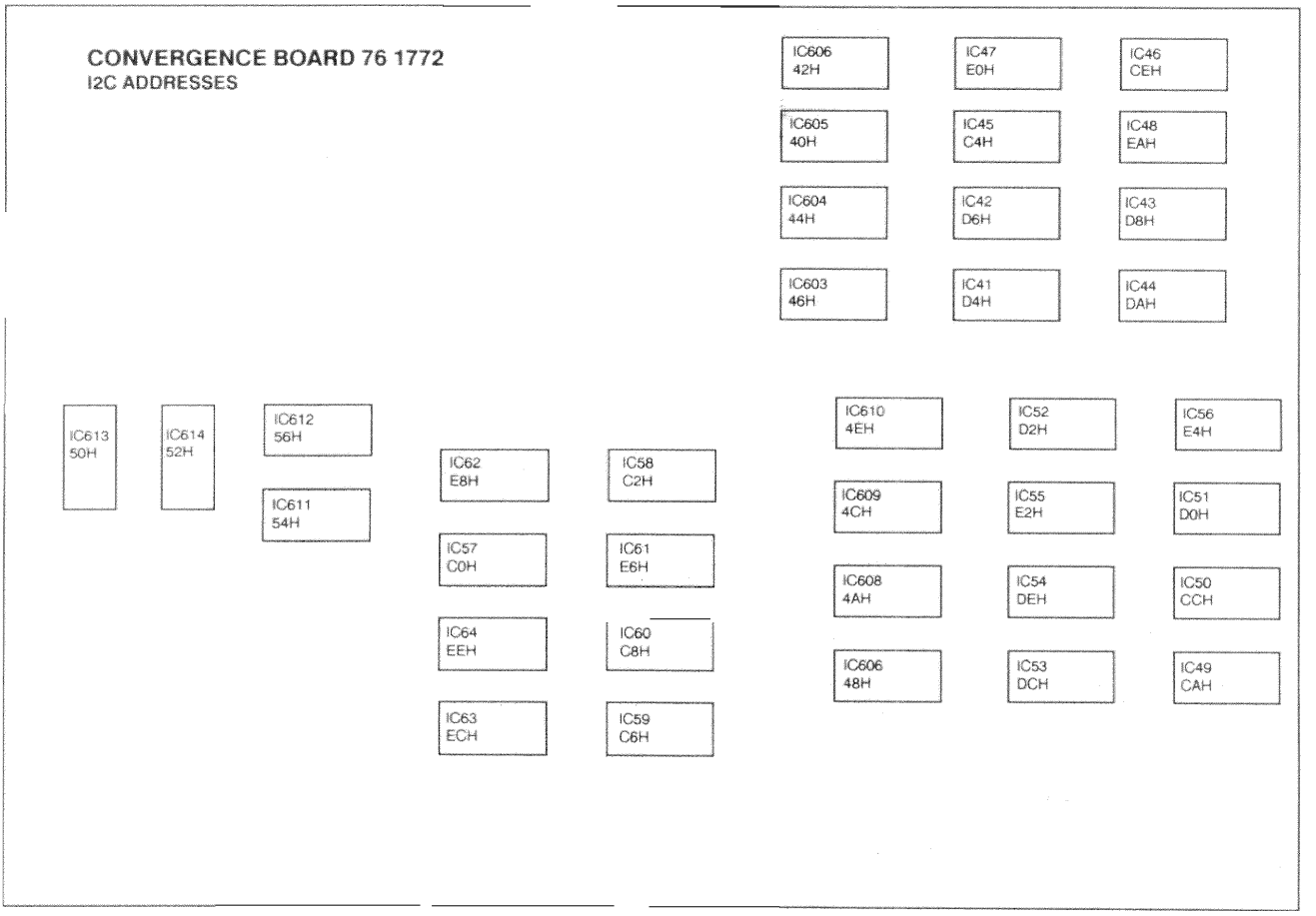
HEX address	IC	CORRECTION
70H	IC2	red on/off green on/off blue on/off sync fast/slow input video input s-video input RGB TTL input RGsB analog input RGBS analog internal pattern

Quad decoder module 76 1822

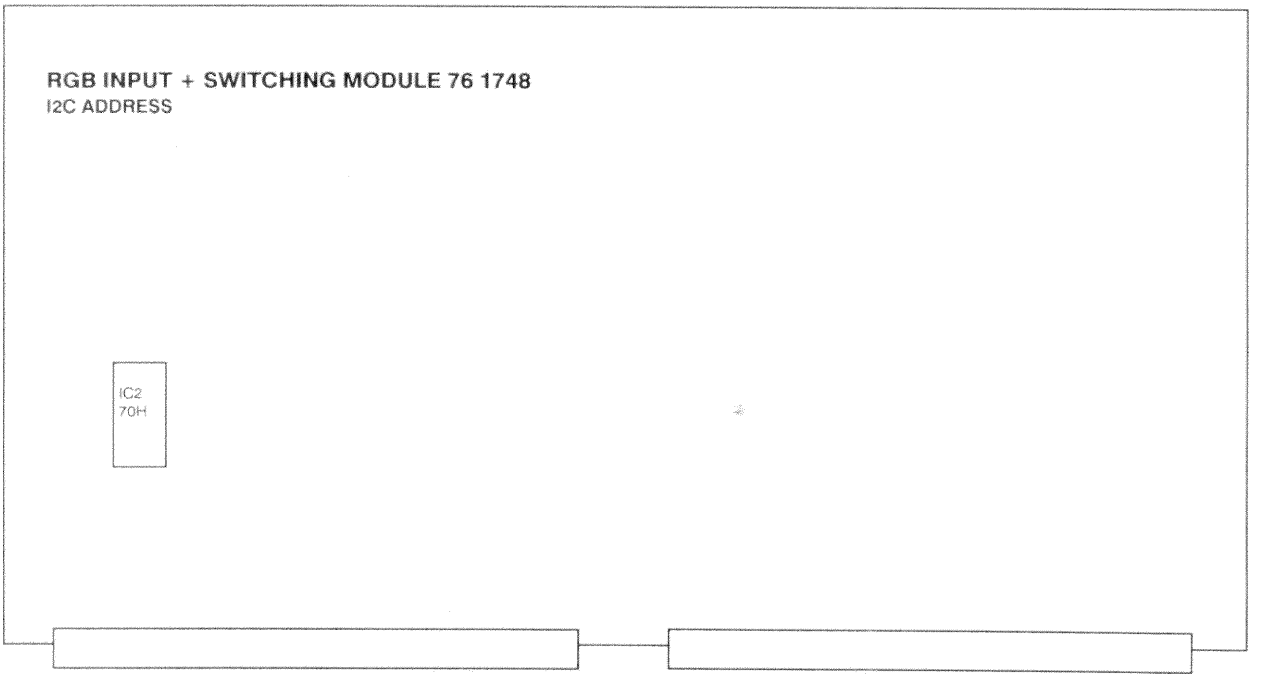
HEX address	IC	CORRECTION
58H	IC3	saturation R-Y saturation B-Y tint sharpness
5AH	IC5	contrast brightness blanking left blanking right
5C	IC1	red gain blue gain red cut off blue cut off

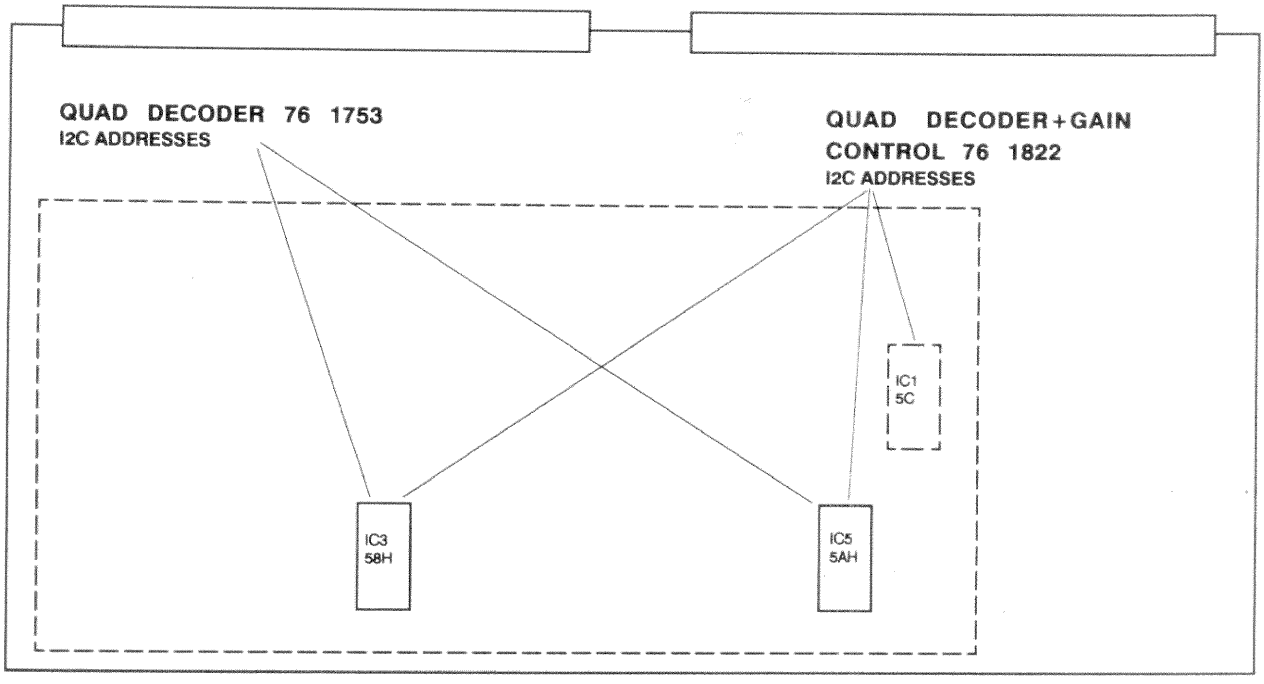
SEE NEXT PAGES FOR LOCATION ON BOARD LEVEL OF THE INDICATED IC's

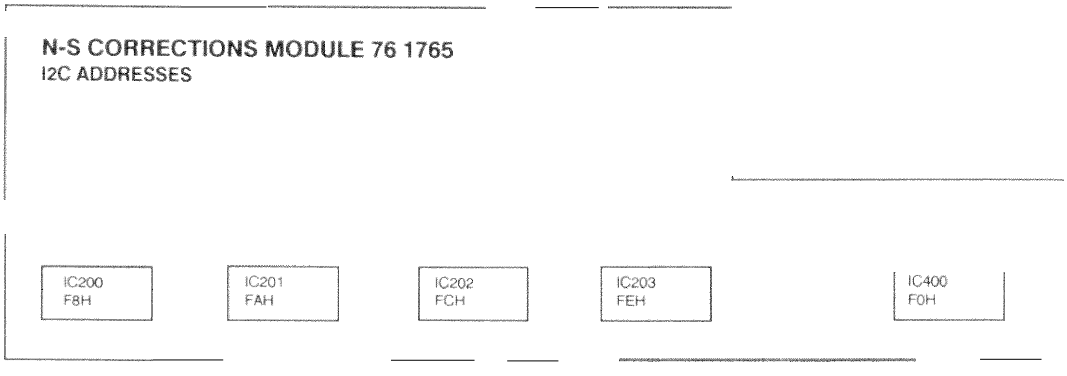
CONVERGENCE BOARD 76 1772
I2C ADDRESSES

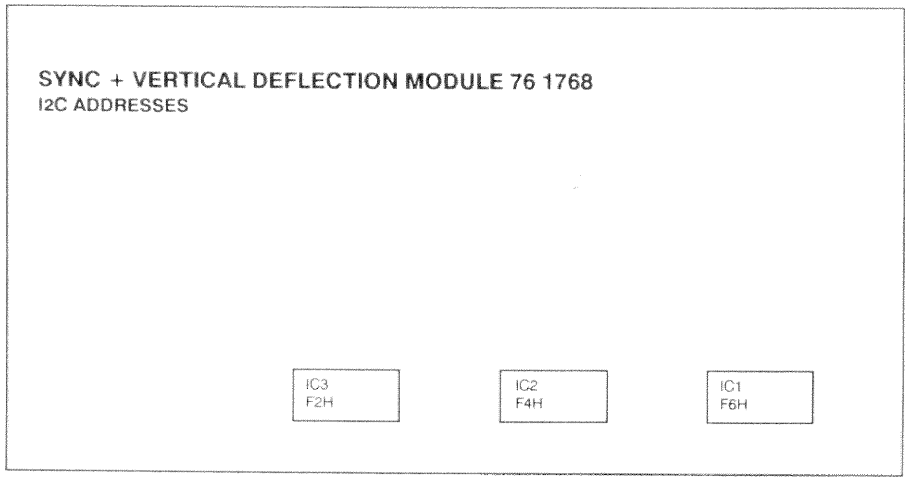


RGB INPUT + SWITCHING MODULE 76 1748
I2C ADDRESS




QUAD DECODER 76 1753
I2C ADDRESSES
QUAD DECODER+GAIN
CONTROL 76 1822
I2C ADDRESSES
IC1
5C
IC3
58H
IC5
5AH


N-S CORRECTIONS MODULE 76 1765
I2C ADDRESSES
IC200
F8H
IC201
FAH
IC202
FCH
IC203
FEH
IC400
F0H


SYNC + VERTICAL DEFLECTION MODULE 76 1768
I2C ADDRESSES
IC3
F2H
IC2
F4H
IC1
F6H

ADDITIONAL INFORMATION

BG-800 COMPONENT CLASS

SYNC-VERTICAL DEFLECTION
76-1768

INTRODUCTION

On this board and its sub-unit we find the sync separator, the autolock circuits, for driving the horizontal line and vertical oscillators, the vertical power output stages for all three vertical yoke circuits, and the preparation for the waveforms for the east-west correction signals.

The horizontal drive pulses for the MOSFET switchers on the Horizontal Deflection board are also prepared on this board.

A Barco designed IC called a " **BELLA**" , comprising four (4) digitally controlled potentiometers, is utilized for the adjustment of the amplitude of the waveforms, or for some DC control voltage adjustments. These Bella IC's are used throughout the BG 800 for digital control of voltages and signals. This IC, custom made for BARCO, is driven by a I2C (serial data) bus from the microprocessor on the controller board.

1. THE VERTICAL OSCILLATOR

a) Sawtooth Oscillator

The vertical sawtooth relaxation oscillator is built around Q3 and Q8 on the main Vertical deflection board. The 28VDC from the SMPS is regulated to 24V by IC8 and charges C13 and C14. As soon as the emitter voltage of Q3 reaches the voltage set by P1 (vertical hold 1) plus .6v , Q3 starts conducting and the collector of Q3 going in a positive direction, forward biases Q8 which also conducts. These two transistors form a discharge path for C13 and C14 to ground , and then the cycle can start all over again. This produces a Vertical Sawtooth waveform that free runs depending on the setting of P1.

b) SYNCHRONIZATION OF THE VERTICAL OSCILLATOR

1) By means of composite sync:

The composite video or composite sync is applied to pin 2 of IC 14 , a sync separator IC The composite sync output, from pin 1 of IC14 goes through emitter follower Q2 to pin

11 of Ic1. The composite sync also goes to Q1 base. The vertical positive going output pulses from IC1 pin 9 go to the base of Q7. The inverted vertical pulses from the collector of Q7 go through D7, C22 and then pull the base of PNP transistor Q3 negative, turning Q3 on. This action requires that Q6 is conducting at the time to form a emitter ground return for Q7.

The vertical oscillator can also be triggered by VS, separate vertical sync pulses injected into the projector at the VS BNC input, or the separate Vertical Sync that is used when the internal crosshatch or on screen display is selected. The separate vertical sync pulses enter the board at J4A-13, labeled VS on the schematic, then they are inverted by Q4 and trigger the vertical oscillator via D10 and D7. The negative sync pulses on the collector of Q4 also cause the gate of Q6 to be pulled low via D9, cutting off Q6. C23 keeps Q6 blocked as long as the negative pulses are on the gate of Q6. This keeps vertical sync pulses from passing through Q7 when separate vertical sync is utilized.

c) " BELLA", BARCO MADE IC: FOUR SECTION DIGITAL CONTROLLED POTENTIOMETER

The voltage or waveform, applied between VRP and VRN is adjustable in 128 steps and is available at the output V0. (refer to IC2, sub-unit , lower left of sub-unit schematic). The corresponding pins are :

VRP1 variable resistor positive 1
VRN1 variable resistor negative 1
VO1 variable out 1

There are four pots in each Bella IC ,and three of these IC's on the Vertical sub-unit. IC1, IC2, and IC3.

The control of these IC's is accomplished with a SCL (serial clock), and SDA, (serial data) which come from the controller board. The address of the IC, (Ic number) is determined by the address pins that are grounded on each IC. The address determines the IC number, such as IC1, IC2 etc... and the slave address determines which pot , VO1, VO2 etc....

The Ic is powered by VCC on pin 28, and VSS on pin 14. VCC is +5 volts DC measured from VSS.

d) Vertical Linearity Control

The shape of the vertical sawtooth determines the linearity of the vertical sweep. This can be changed by means of a feedback circuit, feeding a sawtooth to C14 via R33. (coordinate I-1 main schematic). This sawtooth is adjusted in IC2 on the sub-unit, via

VRP1/VRN1/ VO1. This sawtooth comes from the main vertical board , transistor Q10 (J3-1 marked VST) , goes to pin 19 of IC2 on the sub-unit, and comes out of IC2 on pin 25. It now goes through a buffer stage IC8, and returns to the main vertical board on J3-3 (marked Vlin on the main board), and through R33 to the junction of the vertical oscillator capacitors. This influences the charging behavior of C14, through R33, and therefore acts to change the linearity.

e) The Vertical Autolock Circuit

This circuit is built around Q19 , IC7 (pins 12, 13 and 14) and IC9 (pins 5, 6 and 7). The vertical sync pulses are picked up at the collector of Q7 and differentiated by C9 and R16. This would form a negative and positive pulse, and the positive pulse is used to trigger Q19. The negative pulse is grounded by D37. The output of the op-amp (IC7 pins 12,13, and 14) acting as a comparator, is fed back to the base of Q19 in order to keep it from retriggering after a trigger. R103, C30 determines the time constant of the circuit, before it can accept another trigger pulse.(negative in pin 12 of IC7 = negative pin 14, D38 clamps input)

The non-inverting input of IC7 is pulled up to 12 volts by R108 and a capacitor C31 is connected to ground. When no trigger pulses are applied to the base of Q19, pin 12 is at + 12 volts and the output is at +12 volts. When a vertical trigger pulse is applied at the base of Q19, C31 is discharged via Q19 and the output of IC7 pin 14 switches to -12 volts. This negative voltage is slightly delayed by C30, and this keeps the base low via D38 to prevent re-triggering. The capacitor C31 charges up to the 12 volts and when the voltage on the inverting and non-inverting inputs of IC7 are equal, the output switches high again. IC7 is then ready to accept the next trigger input, and the cycle starts over again.

The time between two consecutive vertical pulses determines the time the output is high, as the time the output is low is invariable and is set by the time constant C31/R108. The duty cycle of this squared waveform depends on the time between two consecutive pulses. This squared waveform is now clamped at ground by D35, so that only the positive portion of the waveform will charge the capacitors C62/C61. D34 and D36 provide a path for discharge of the capacitors in both directions for rapid equalization when changing vertical frequencies. This circuit acts as a variable chopper power supply, with the vertical frequency determining the output DC level. The C62, C61 network, acts as a double integrator, to change the pulsating DC to a varying DC voltage, **inversely proportional to the vertical frequency.** This voltage is sent to pin 5 of IC9 (a buffer). When the vertical frequency increases, the voltage on C61 decreases due to the shorter duty cycle, and Q11 conduction decreases, and causes an increase in the charging current of C14 through Q12. This is due to the fact that when Q11 conduction decreases, there is a higher DC level at the emitter of Q12, causing Q12 to increase conduction. This causes a higher DC level at the collector of Q12. Basically Q12 and R23 are in

parallel from the 24 volt line to the vertical oscillator capacitors. When Q12 conduction increases, it's internal resistance is lowered and since the time constant of the vertical circuit is R23 times C13 and C14, a lowering of the parallel resistance of R23 and Q12 will decrease the time constant and cause the vertical sawtooth frequency to increase. The Vertical Hold 2, P2, allows an adjustment of the gain and thus the highest frequency that must be locked by the circuit.

f) Vertical output stages, vertical shift, vertical amplitude.

The vertical sawtooth at the emitter of Q10 leaves the main vertical board from J3(1) and goes to the sub-unit to IC2 (VRN0 and VRP0 Vertical Amp Adjust) and the output leaves at VO0 (pin24), and returns to the main board through Q5 at J4 (4). It is now capacitively coupled to the inverting inputs of the power amplifiers IC11, IC12, and IC13 together with a DC voltage (vertical shift voltage). The vertical shift voltages are controlled by IC3 on the vertical sub-unit. (outputs 25, 26 and 27). The red and blue beam will follow the green shift, because a portion of the green shift voltage is fed to the red and blue shift lines. The shift voltages vary between +3V and - 1.7V. The sub-unit on the main board (coor. G-5) is used to fine tune the vertical blue and red shift, so that accurate center shift can be attained. The shift in terminal J4B12 is used, when the vertical scan is changed from ceiling mount to table mount. These two analog shift voltages are coupled with the voltages from IC3. (This sub-unit may not be present in older 800 Series projectors, however it can be added). This sub-board also contains 2 pots, P4 and P3. These pots can be used to adjust the red and blue vertical raster size to match the green raster. This adjustment should be done in the **North South Geometry** mode only.

The amplified sawtooth output currents flow in the respective scan coils and the ground return for these waveforms are the feedback resistors R44, R97 and R79. The amplitude of the waveforms across these resistors is proportional to the vertical amplitude and thus, these voltages can be used for a feedback stabilization of the vertical output circuits.

The TDA 8172 allows for a short vertical retrace time by doubling the supply voltage during retrace. During the flyback the voltage across capacitors C35, C55 and C52 is switched in series with the supply voltage of +8v. As a result, the voltage during flyback is 8+ (8+17)= 33 volts. This increased voltage allows for a shorter flyback time.

g) Vertical scan fail detection.

The flyback pulses at the pins 6 of the output amplifiers are AC coupled to a parallel detector. The diodes rectify the negative pulses and generate a negative 21 volts at the anode of the three diodes, (D24, D22 and D28) when a flyback pulse is present. As soon as one of the output stages fail, the voltage on the corresponding capacitor looses it's negative charge and via the diode, the base of Q14 gets a supply voltage from the +17 volt supply through one of the resistors (R88, R83 or R85) and Q14 turns on pulling

the scan fail line low, through D17. Diode D16 and the saturated Q14 cause a permanent conduction of transistor Q15, and the high generated at J4B (26) blanks the CRTs.

Vertical retrace blanking pulses are derived from the vertical flyback pulse at pin 6 of the red output stage (IC11) and fed to the base of Q20 , and then to Q15. The Vertical Blanking pulse leaves the board at J4B (26).

2. EAST-WEST CORRECTION.

a) Trapezoidal distortion correction.

The sawtooth waveform (VST) is applied to the buffer IC7 on the sub-unit via C14 (pin 10 of IC7). This signal is inverted by an invertor in IC7 (pin 12, 13 and 14) , and the two opposite phase sawtooth's are fed into IC1 pins 16, 17, or VRN0 and VRP0. The corresponding VO0 output goes through R45 to the adder amplifier IC7 pins 5,6, and 7. R 43 also couples a parabolic waveform into this same adder.

b) Parabolic or pincushion distortion correction.

The parabolic waveform is obtained by means of the multiplier IC11. The waveform at pin 8 of IC7 goes to pins 10 and 1 through capacitors C1 and C2. The opposite phase signal outputs of pins 6 and 12 are then capacitively coupled to the pins VRN2 and VRP2 of IC1. The adjusted output VO2 is now applied, together with the previously discussed sawtooth output to the adder IC7 pin 5. Part of the parabolic waveform also goes through Q3 and Q2, and exits Q2 emitter via R29 to J4 -10. This VPAR then goes to the focus board for electronic focus correction from top to bottom of the raster.

c) Frequency dependent correction.

The gain of the Op-amp in IC7 pins 5, 6, and 7 is variable and depends on the divider R31/Q1. The FET Q1 is biased by the output of an Op-amp IC7 (pin 1). The integrated output of the E-W correction, pin 7 , is applied to the Miller integrator input , pin 2 and the other input receives a portion of the HTHD voltage. The HTHD voltage is proportional to the line frequency. An increase of the line frequency , results in an increase of the voltage on pin 3 (+HTHD'). This results in an increase of the gain of the op-amp because the fet Q1 conducts more. This shunts the negative feedback to ground and increases the gain of the op-amp. Pin 2 follows this increase up to the point where both pins 2 and 3 have equal voltage. Through his method , we have a frequency gain correction for higher frequencies since we would need a larger signal at the higher frequencies.

d) Power Amplifier.

The sum of the corrections are sent back to the motherboard to be amplified by IC10 pins 1,2, and 4. It is then sent to the horizontal deflection board to modulate the HTHD supply Via Q13 on the horizontal deflection board.

3. MIDLINE CORRECTION (bow and skew)

The midline bow and skew corrections are added to the phase control of the picture. These corrections are a dynamic correction of the phase at a vertical rate, in order to adjust the center vertical line. The sum of the sawtooth and parabolic waveforms, are added via R44 and R42 on the sub-unit, and are then sent to the op-amp in IC8 (pin 24 and pin 25 of IC1 to IC8 pin 2). From IC8 pin 1 they go to pin 15 of the monoflop in IC12. This monoflop is triggered by the horizontal pulse from IC12 pin 12. Depending on the waveform on IC12 pin 15 and HTHD on this same pin, Ic12 output on pin 4 will have a variable width pulse. The width of the pulse is dependant on pin 15's voltage. If we use the trailing edge of the pulse to key the next stage, it can be seen that we have a way of varying the phase. The time constant of the monoflop is dependant on:

1. The corrections sent via D16, the dynamic correction of the phase.
2. The scan voltage +HTHD'; in order to decrease the correction at higher frequencies. At the higher frequencies, the phase correction as related to time would have to be less, because the line period would be less, and the percentage of correction would have to remain the same.

4. PHASE ALIGNMENT.

The phase of the picture is adjusted by introducing a variable delay of the horizontal drive pulses.
The adjustment range over the entire frequency range must be proportional with the line period.
If we have for example, a 6 microsecond range of phase shift at 15kHz, this would represent 64/6= 10% phase shift. The same 6 microsecond shift at 90 kHz would be 11/6= %50 phase shift, or half the picture. Consequently, the range must be much lower for 90 kHz compared with 15 kHz, or the range must be "tracked" with the line frequency. The DC voltage at VO2 (pin 26 of IC2) is the DC phase shift voltage and is sent to comparator Q7. The other transistor in Q7 receives the integrated drive pulses, thus a DC voltage related to the line period.(left side of Q7). The difference in voltage between the two collectors of Q7 becomes the base emitter voltage of Q6, or Q6 bias. Q6 is a current generator and part of the time constant of the monoflop in IC12. The width of the output pulse is controlled by the current generator Q6 and the monoflop, as long as the DC voltages at the bases of Q7 are not the same.This means that the width of the pulse (=

phase shift) becomes smaller at higher frequencies, in order to decrease the phase shift at these higher frequencies.

The pulse train that inputs to pin 10 of IC12 comes from J3-5 (HP In). This Hp In horizontal pulse comes from the main board, IC1 pin 4(J4 pin2 labeled HP out on main board). The horizontal pulse enters IC12 pin 10, and the variable width pulse exits IC12 pin 12 and goes to IC12 pin 2. Between IC12 pin 2 and Ic12 pin 4, the Vertical centerline skew and bow are adjusted, and that variable width pulse exits IC12 pin 4. Next, the signal goes through Q8 at pin 12 of IC12 and is then sent to the main board of the unit and then to IC5, pin 11(marked J4-2 HP In). IC5 monostable now produces a horizontal drive pulse with a constant (2uS) width, that will drive the MOSFETS on the UN Deflection Board (HDR).

5. HORIZONTAL OSCILLATOR- HORIZONTAL AUTOLOCK

a) Horizontal autolock

The sync separator IC14, (which is really a sync stripper) on the main board sends Q1 a composite sync signal (both horizontal and vertical sync). The amplified signal is then split to the PLL (IC6) and transistor Q17. The oscillator in the TDA 2595 is locked to the exact frequency by a PLL, but the latter has only a limited lock range of approximately 1.2 kHz. Therefore it serves as a fine lock for the frequency. An additional PLL, IC6 is used to coarse lock the frequency range from 15 to 90 kHz.

IC6 consists of two phase comparators and a VCO (voltage controlled oscillator). For this application, only the second phase comparator is used. The signal input, (pin 14 of IC6) is the line oscillator of the TDA 2595 (IC1), and the comparator input (pin 3) is the sync pulses buffered by Q1. The corresponding output is pin 13.

Note that it is a three level output and thus a pulsed information source. If the output is "open", (in the locked state) the voltage is set at 6 VDC with R92/R89. On the other hand, pin 6 of IC7 is set at 7.7 VDC with R94/R90.

In the locked state, the FET(behaving as a switcher) Q9 is blocked, because the output pin 7 of the voltage comparator IC7 is "low". Indeed the PLL output is 6 volts, thus pin 5 is lower than pin 6 and the output is "low". When Q9 is blocked, the coarse frequency correction circuit is in effect disconnected from IC1.

b) Line oscillator lower than the horizontal sync frequency.

If we assume that the horizontal frequency is lower than the horizontal sync pulse frequency , then the voltage on C8 decreases(pull down state). **The output voltage on IC6 pin 13 will track the line frequency versus the sync frequency. If the line oscillator is at 15kHz and the sync is at 33 kHz, pin 13 will go low.** This voltage is

now buffered and sent to pin 5 of IC7. Because of the Zener Z3, this voltage cannot decrease and stays at approximately 6V. The other pin, pin 6 is initially at 7.7v (divider R90/R94). This voltage now decreases because transistor Q17 discharges the capacitor C50 as follows:

The squared horizontal drive of pin 4 of the TDA 2595 switches Q18 on and off . When the frequency of the line oscillator is different from the horizontal sync (as we assume), these pulses arrive on the base of Q17 at the moment Q18 is off. These horizontal sync pulses switch on Q17 and C50 is discharged. The voltage at pin 6 drops and becomes lower than the other input on pin 5. The output on pin 7 of IC7 switches "high".
The gate of the MOSFET Q9 is now positive and Q9 conducts and connects the output pin 8 of the PLL (IC7) to the inverting input, pin 2, of the next integrating op-amp (IC7 pins 1,2,and 3). The decreasing voltage output of the PLL is inverted and transistor Q21 draws more current out of pin 14 of IC1 (TDA 2595). This increases the frequency of the line oscillator. **(IC1 pin 14 voltage is inversely proportional to the frequency. I.E., if Q21 turns on hard, it's collector goes low, and the oscillator frequency in IC1 will increase).**

As the frequency of the line oscillator increases, the PLL output also increases equally. This continues until there is coincidence between the horizontal drive and the horizontal sync at the base of Q17. Once coincidence is reached, the voltage at pin 6 is again 7.7 volts and the Mosfet Q9 changes to a blocked condition.

From this point on, the fine frequency lock in the TDA 2595 takes over and adjust the line oscillator until the exact frequency and phase is reached. The output line of the TDA 2595 ,pin 17, then feeds IC7 pin 2, and the fine frequency loop is established. In the locked state this PLL output is 6 volts. Since pin 3 of the op-amp is biased at 6 volts, the action of the op-amp continues up to the moment the oscillator is locked. Any small change in frequency after it is locked, is handled internally by the TDA 2595.

c) Line oscillator higher than the horizontal sync.

In this case the PLL output is increasing, Z3 cannot perform it's zener function,and pin 5 of IC7 follows the PLL output voltage, or goes in a positive direction. Again, because there is no coincidence, the voltage at pin 6 is decreasing because the sync pulses are triggering Q17, and pulling it's collector low. This again turns on the FET Q9, so the coarse loop is connected. Now the "high" on IC7 pin 8 is coupled through Q9 to Ic7 pin2, inverted to a low and used to reduce the forward bias on Q21. This causes Q21's collector to go high, and thus, lower the horizontal frequency.

6. ADJUSTABLE TOP AND BOTTOM BLANKING

The sub-unit generates blanking pulses for an adjustable blanking of the top and bottom

of the picture. To achieve a high accuracy, or , in other words, to dispose of a steep ramp, the sawtooth is sent into a "dead band response amplifier", built around the Op-amp in IC8. The sawtooth enters pin 9 of IC8 on the sub-unit. The output is inverted and the ramp is steeper at the start and at the end. The two clipping levels are set by clamping circuits in order to obtain a complete feedback between these levels. As soon as the first clipping level is reached, the output is steady, and no output signal change is noted.

The resulting waveform is now sent to two level detectors in IC9(IC9 pin's 6 and 3). The clipping levels are regulated by the potentiometers in the Bellas, IC2 and IC3. The resulting top and bottom blanking exits IC9 pins 7 and 1, is added and then goes to IC10 pin 5. In IC10 it is mixed with a horizontal line pulse and exits pin 2. The signal now goes to the main board, to the base of Q20.

7. SIMULATION OF THE FLYBACK PULSE FOR THE PLL OF THE TDA2595.

A " simulated" line flyback pulse is generated from the monoflop IC4. The first monoflop introduces a small delay for the pulse and the second monoflop standardizes the width of the pulse. The delay from the first monoflop is used to mislead the PLL IC and allow for a "negative" phase shift.

8. BLANKING- COINCIDENCE.

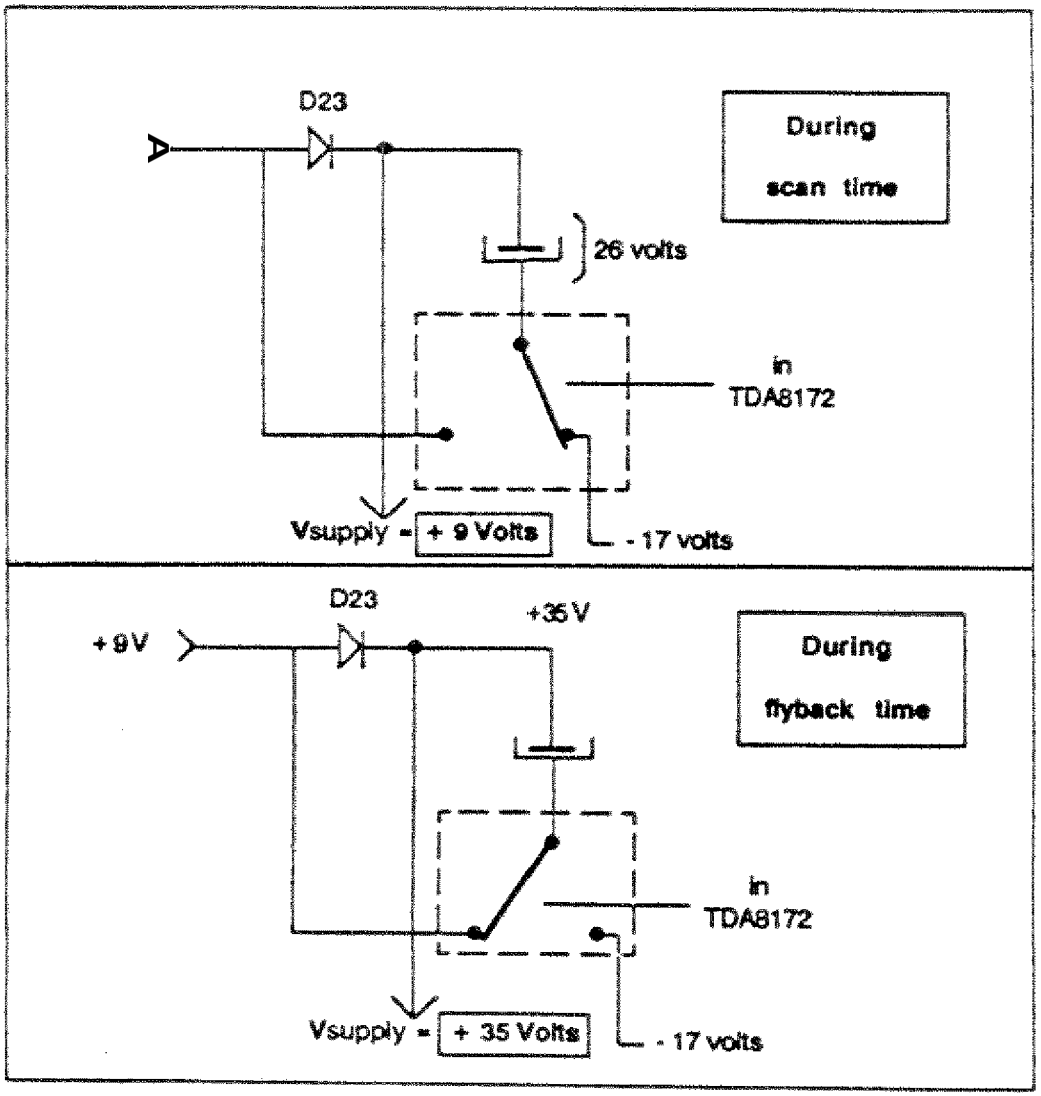
In the event of **non-coincidence of the sync and horizontal line pulse, or the absence of any Vertical Sync Signal** transistor Q16 on the main board is completely saturated. This signal comes from IC7 pin 7, which is only low, when the line pulse and sync are locked to each other. In an unlocked condition, pin 7 is "high" and this turns on Q16 via R310. This results in :

-Led D20 is illuminated to show the non-coincidence condition.
- If the blanking strap is in position, transistor Q15 is also saturated, and causes blanking of the three CRT's.

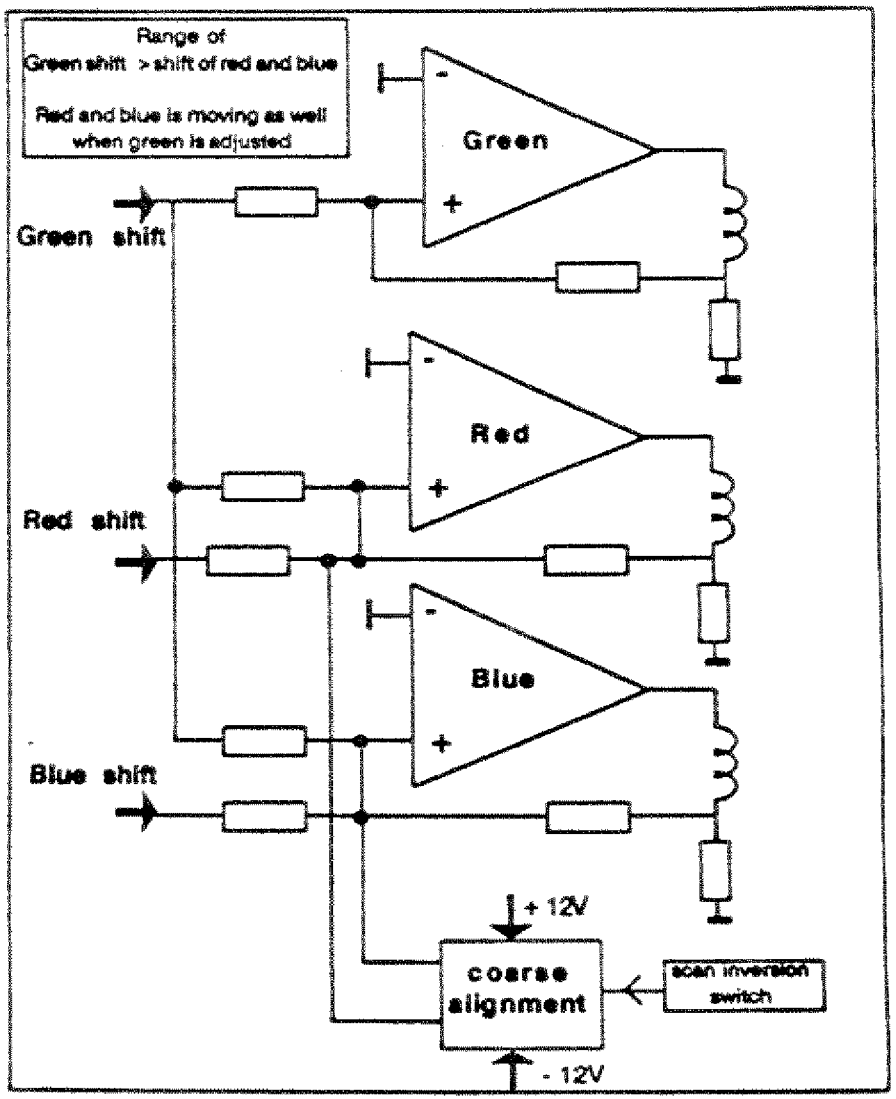
By removing the "blanking strap", the picture will not be blanked during non- coincidence.

If there is no Vertical sync, transistor Q5's base will be "high", causing Q5 to conduct, and via D5, the blanking and non-coincidence circuits will be activated.
Note: Blanking and non-coincidence are activated by horizontal unlock, or absence of vertical sync only. Therefore, if the vertical hold controls are maladjusted, and the picture rolls vertically, it will not blank out. This " non-coincidence " signal is used by the controller board, to determine if the projector has an active source. In non-coincidence, the controller will display a message " no source, check input".

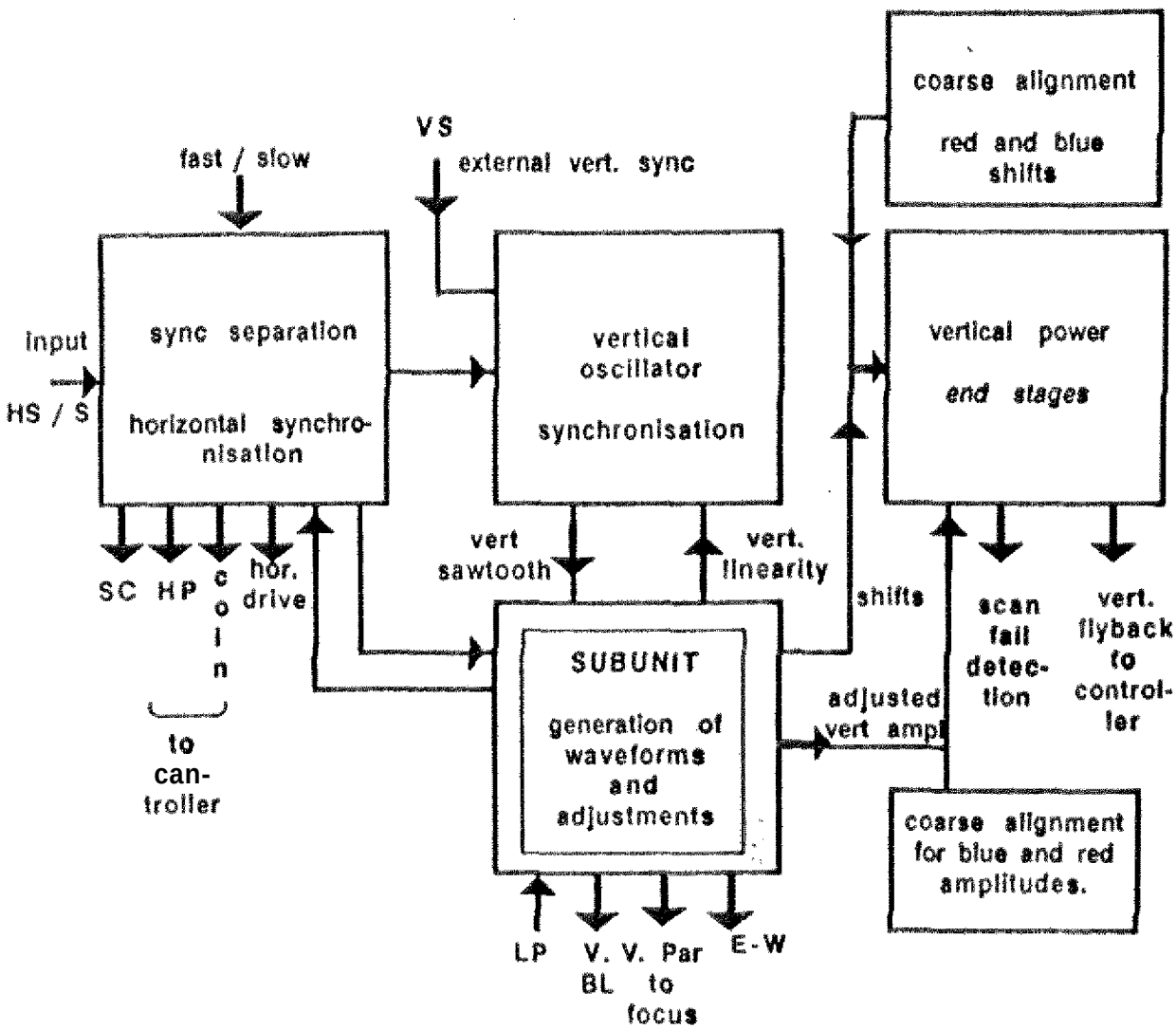
VOLTAGE DOUBLER DURING FLYBACK



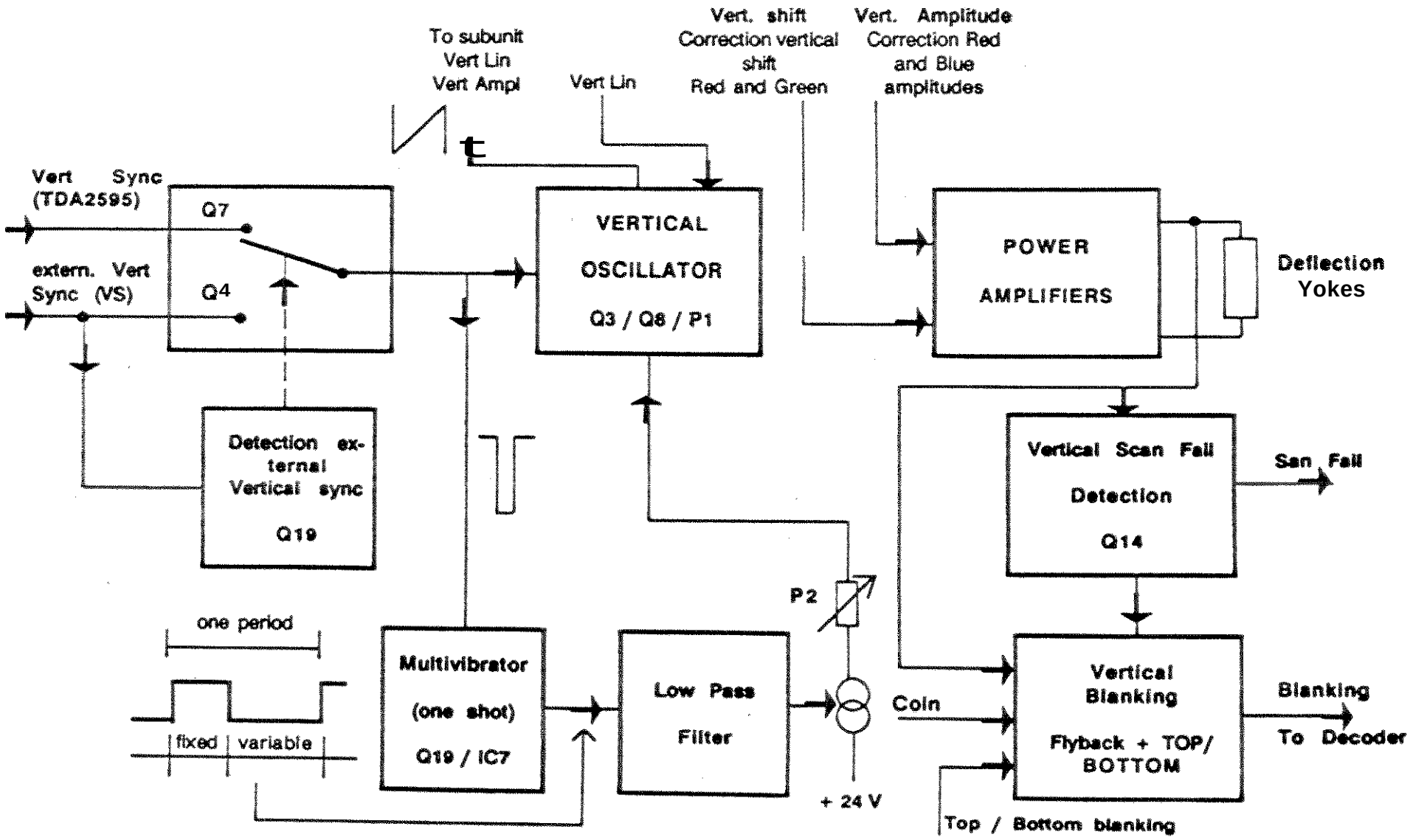
VERTICAL SHIFT



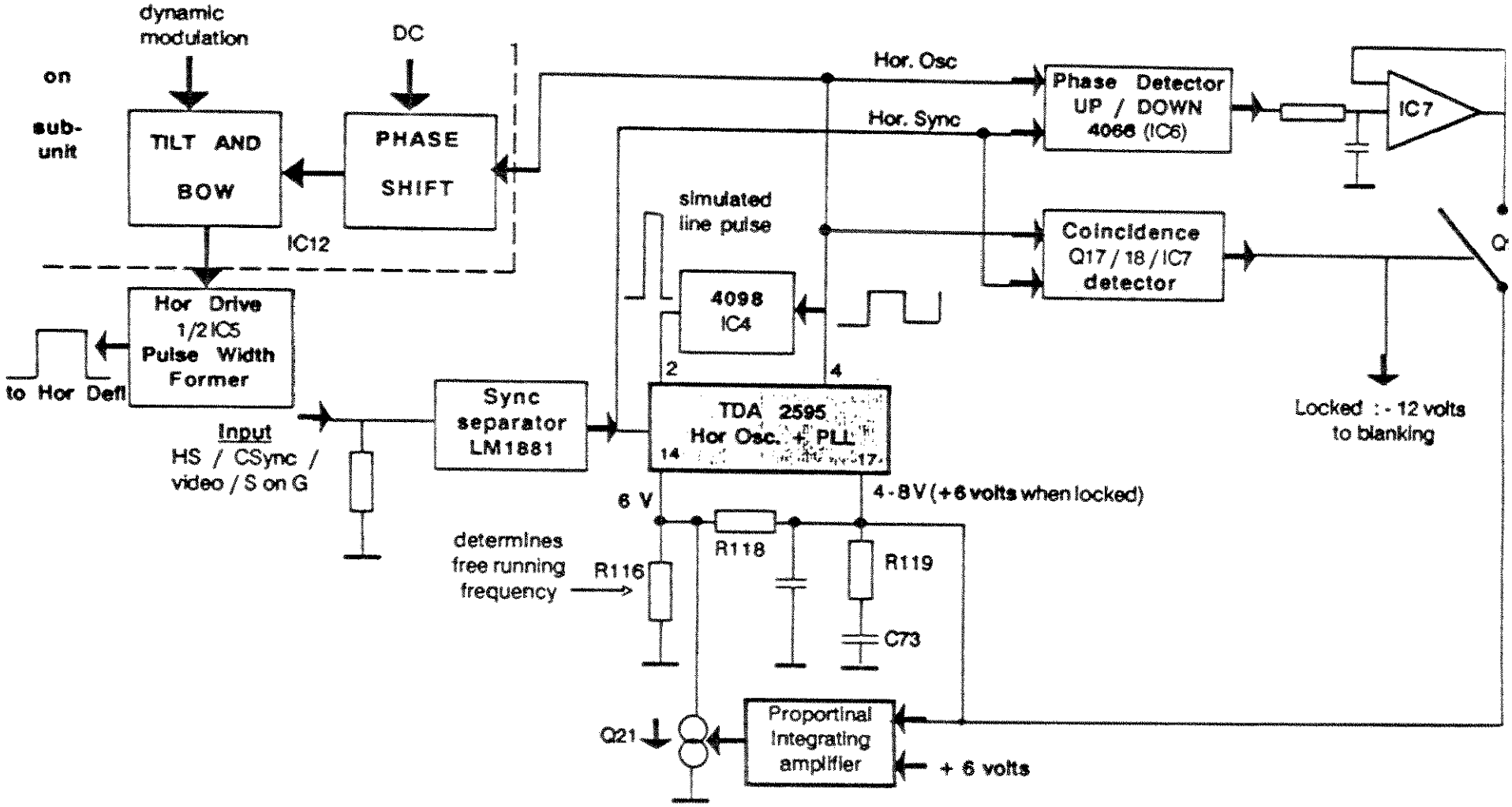
VERTICAL DEFLECTION UNIT



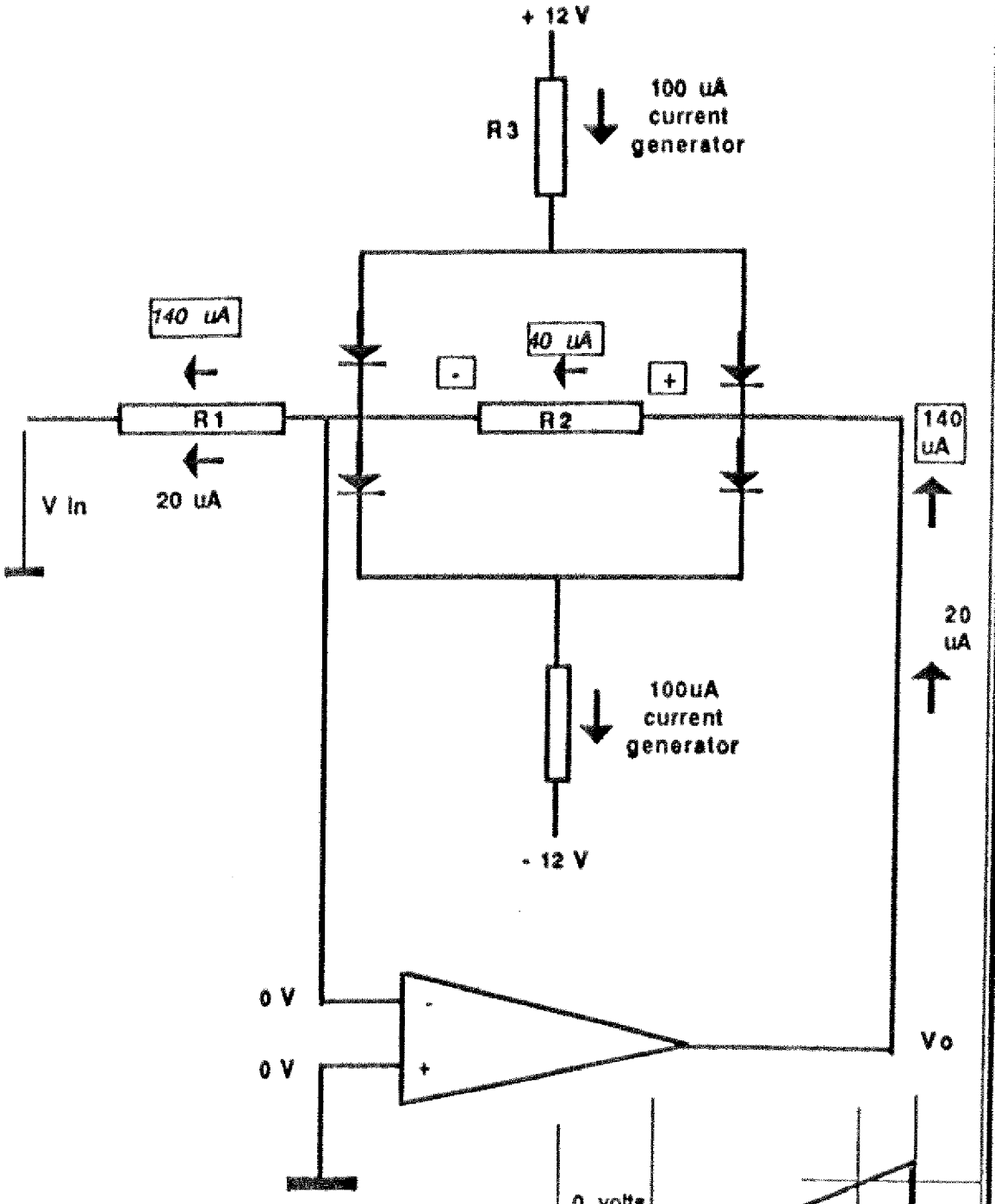
VERTICA t OSCILLATOR AND SYNCHRONISATION

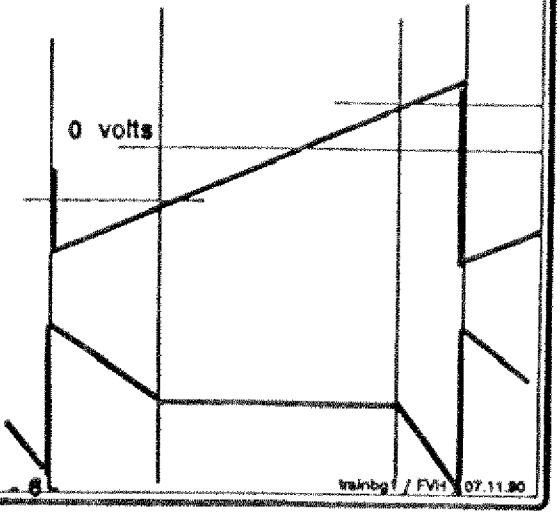


SYNC SPARATION AND HORIZONTAL AUTOLOCK



DEAD BAND AMPLIFIER



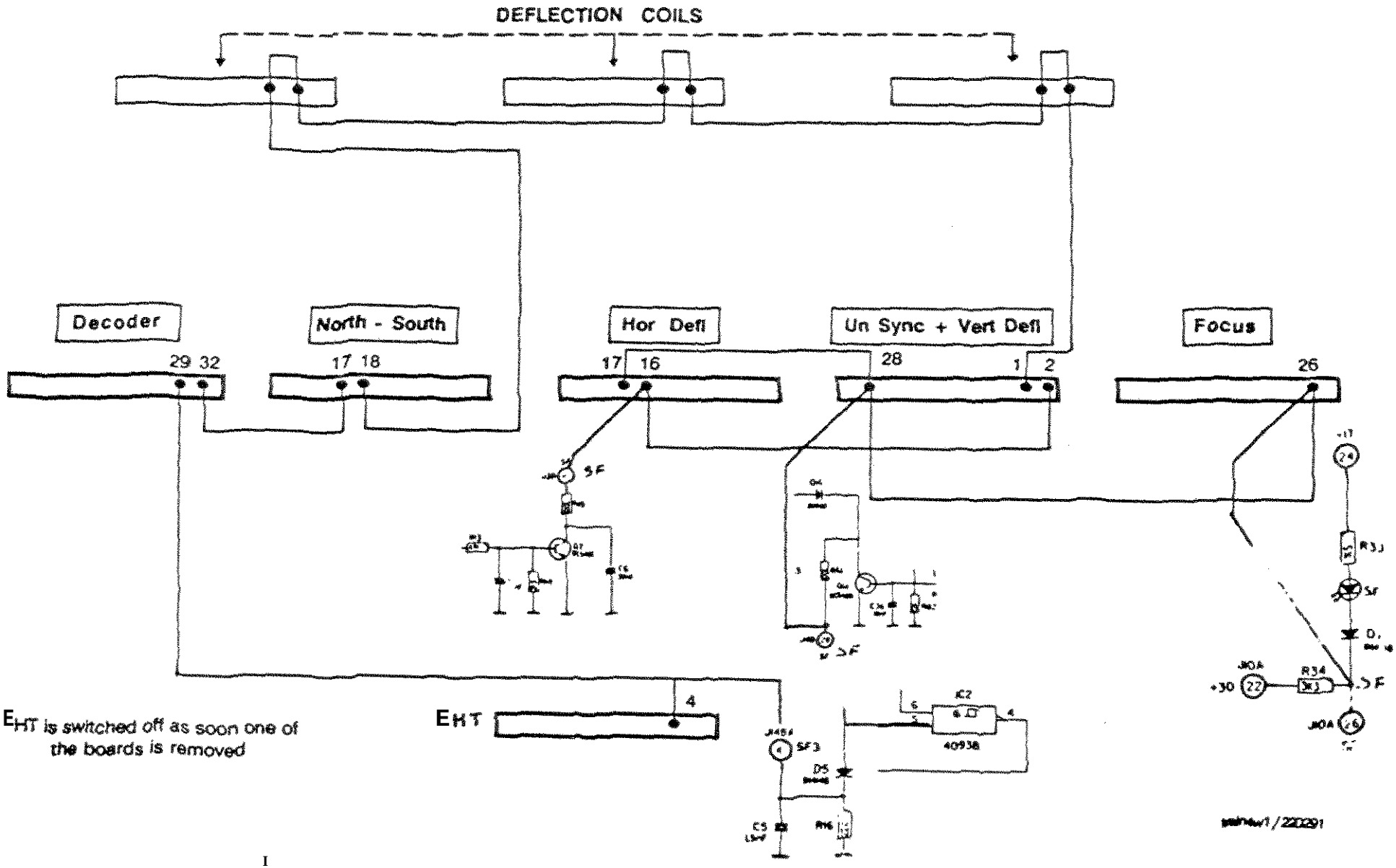


Dead zone start when I (R1) = I (R3)

Input : $V_I = R1 / R3 (12 - Vd)$

Output : $V_o = R2 \left(\frac{12 - Vd}{R3} - \frac{V_I}{R1} \right)$

SCAN FAIL LOOP / PROTECTION OF THE CRT



E_{HT} is switched off as soon one of the boards is removed

BG-800 COMPONENT CLASS

EHT BOARD

76-1742

INTRODUCTION

On this board, the EHT drive pulses for the EHT power supply are generated. The primary circuit for the EHT power supply receives it's 300VDC supply from the Mains. In the event of failure, either because the EHT is too high, too much current in the EHT circuit or a horizontal or vertical scan fail condition exists, the EHT voltage is discontinued. We will discuss the generation of the EHT pulses, the EHT regulation, and the different protection circuits.

DC controlled multivibrator.

The EHT multivibrator is configured around two Schmidt Trigger NAND gates in IC2. Two time constants are involved in this circuit; C7/R11 and C8/ R10 +Q2.

The first time constant is fixed, (C7/R11), whereas the second time constant is variable, depending on the current flow through Q2. Transistor Q2 acts like a variable resistor in parallel with R10. By varying the bias on Q2, and therefore it's resistance, the time constant can be varied (T= R x C)). Q2 is driven by the comparator transistor Q1. Q1 receives it's base bias voltage from FBHV (feedback high voltage from the divide by 1,000 circuit in the Splitter). The emitter of Q1 is set at +33 volts by zener Z1.
The duty cycle or the on/off time of the power switcher Q7 , is regulated by the voltage difference detected by Q1, between the fixed emitter and the FBHV from the splitter. The frequency of this oscillator is typically 80kHz. This circuit keeps FBHV within a 1 to 2 volts of Z1 reference voltage.

The squared waveform at pin 3 of the NAND gate is , via a fast switching FET Q3, sent to the opto-coupler IC1. This opto-coupler is necessary because the remainder of the circuit is supplied with a +17M voltage and + 300 VDC Main which is not isolated from the Mains. The + 17M voltage DC is obtained from a special winding on the SMPS and the 300 Volts DC is the main bridge rectified mains voltage (GNDM is " mains or hot ground ").

Caution : Any servicing on a board that uses both a Mains Ground and a Chassis Ground, should involve the use of an Isolation Transformer, especially when using a " Scope ", or other equipment connect to the main AC source. Do not connect

the Main and Chassis Ground together at any time.

FET Q6 drives the push-pull stage Q4/Q5 and the pulses are capacitively coupled to the gate of Q7. The zener diode Z3 has two purposes. The negative level of the pulses are clamped at - 0.6 volts , and on the other hand limited to + 20 volts DC , in order to protect the switcher Q7. The transformer and the quadrupler are one in the same unit. The +300 volts DC from the main bridge, enters the board at J148A pin 22, and passes a filter L1/C19 and a fuse before it goes to the Quad at J148A pin 32 (+300HV).

Protections

a) EHT hold down:

The slider voltage of P2 (hold down adjust pot) is sent to the base of Q8 and Q8's emitter is set at 5.6 Volts by Z4. As soon as the EHT rises beyond 36.0 kV , the transistor Q8 starts conducting, turning on Q9. The schmidt trigger pins 8 and 9 of IC2 go high, and it's output pin 10 , goes low. Diode D6 pulls the EHT multivibrator pin 5 on Ic2 low, and the multivibrator stops, halting the EHT. The output of IC2 , pin 11 goes high at the same time and forward biases LED D8, to indicate a EHT hold down condition. The feedback resistor R30 keeps the hold down condition on (lock-down), until the projector is powered off to reset the circuit.

The EHT hold down must equally operate when there is an " open loop " situation , or no EHT feedback voltage from the splitter. If that were the condition, there would be no way for the circuit to monitor the EHT, and it could go higher than the 36.0 kV. The detection for " open loop " is built around the EHT "flyback" pulses on the drain of Q7. These pulses are rectified by D42 and the resulting pulsating DC is filtered by the PI-filter C30 and C12, and sent to Q10 base. As the EHT gets higher, the flyback pulses will increase in amplitude, and therefore the voltage to Q10 base will increase. From 5.6V and above Q10 conducts and via the opto-coupler Ic3, the output pin 6 of the opto-coupler is switched low. This condition would exist if the amplitude of the pulses were excessive, or in other words, the high voltage was too high. This output is connected to Q8 collector, and pulls it low, turning on Q9, and the multivibrator is stopped as explained above.

Note that Q10 is supplied by the +17M voltage (not Isolated from main or hot ground)

Finally, in the event of an excessive amount of CRT beam current, with a long duration, the duration determined by the time constant R102/C39 , the collector of Q8 is pulled low via Q27, resulting in EHT hold down. The base of Q27 is connected to ground, and HVL is in the ground return of the Quadrupler, (see 76 1743 for HVL schematic), so as the emitter of Q27 goes more negative as the total beam current increases, Q27 is more forward biased and starts to conduct, pulling the collector low and activating the EHT hold

down. If any 1 CRT begins to draw too much current i.e. shorted CRT, through the "BCL" input,(coor. E6), Q27 again turns on causing HV holddown.

In conclusion, the EHT HOLD DOWN LED is " **on** " for :

-too high EHT, information via the feedback FBHV
-too high EHT in open loop via Q10 and opto-coupler IC3
-too high total beam current lasting for some time via HVL
-too high beam current in any one CRT via BCL

b) Horizontal and Vertical Scan Failures:

In the event of a horizontal or vertical scan failure detected on the horizontal or vertical boards, the EHT multivibrator is stopped via D5. Scan fail is a "low" from the scan fail detect circuits. Via D5, the EHT is halted.

c) Overcurrent protection:

The drain-source current of Q7 is measured by the resistor R21 in series with the source. This voltage is applied to transistor Q14 via a divider R40/R15. When this voltage exceeds 0.6 volts, Q14 starts to conduct and stops the EHT drive pulses by removing enable to IC1 pin 7, preventing damage to Q7 (pin 7 of IC1 is the enable pin , and must be "high" for the Ic to pass a signal). In this case , we have no illumination of the EHT hold down LED.

Slow startup of the EHT.

When the projector is switched on, a slow startup of the EHT voltage is provided. This is accomplished by the circuit around transistor Q11. The voltage for the reference zener Z1 is taken from the + 230 volt line through R7. When the unit is switched on, capacitor C4 charges up via R7 and C40 charges through R43. Until C40 fully charges, PNP transistor Q11 will be forward biased and inhibit C4 from charging. This gives a slow rise to the voltage for Z1, and this is the voltage that the FBHV is referenced to, so therefore the EHT will also have a slow rise.

When the unit is switched off, C40 is rapidly discharged via D9 because the 230VDC line drops quickly, taking the EHT reference voltage on Z1 quickly down, and therefore the EHT itself goes down. C40 discharging turns on Q11 because it's base is pulled in a negative direction. If a scan fail signal is present, Q13 sees a (**low**) causing Q13 which is normally biased on to go off. The base of Q12 then goes " High " and C40 is discharged, pulling down the reference voltage, through the conduction of PNP transistor Q11.

The EHT is stopped during scan fail by J148A pin 4 going low, and through D5, stopping the EHT multivibrator. If the scan fail is removed, we are back to a slow start condition because Q13 base would go High, saturating Q12, and thereby discharging C40 and C40 and C4.

FET Q30 is used to keep a drive pulse from driving Q7, until the drive voltage from the preceding pulse is zero. The EHT pulse is coupled to the gate of Q30 and removes the high on the enable pin (pin 7) of Ic1 until the drive pulse is zero, turning off Q30. Then the next pulse can pass.

To adjust either the High Voltage P1 or HV holdown P2, an accurate high voltage probe must be used. A probe is available from Barco, complete with a connector that will safely connect to the splitter. Failure to use the correct type of probe can cause the following:

1. Inaccurate high voltage settings causing; poor picture, abnormal CRT wear, arcing potential, excessive tube radiation.

2. A SHOCK HAZARD. the EHT is set at 34.7kv, AND THIS VOLTAGE IS WELL REGULATED. A shock from this supply, due to an improperly designed, hand held HV probe, could result in severe injury to the technician.

When adjusting either P1 or P2, these components must be replaced with new parts, and after setting the pots, they must be glued and white safety covers attached.

BG-800 COMPONENT CLASS

SM POWER SUPPLY
76 1770

The switch mode power supply:

The switched mode power supply derives all the necessary DC voltages and isolates them from the incoming main voltage from the AC line.

The first section of the power supply to start up is the plus and minus 9 volt standby power supply. It provides the controller board with the necessary voltages to operate the controller board circuitry so that the control IC's on the controller board will be active to read the information from the RCU or the built in controller.

The second section of the power supply delivers all the stable or fixed DC voltages and it is built around IC102, Q101, and T2.

The third part of the power supply produces the HTHD which is the frequency dependant voltage that is fed to the Horizontal sweep circuitry. This is built around IC100, Q100, and T1.

1. Principle of the switched mode power supply:

The principle of the switched mode power supply is as follows

When a positive pulse is applied at the base of switching transistor Q101, a current flows through the primary winding of transformer T2, supplied by the 300 Volt DC input bridge rectifier, through F100 to P19. When the switching transistor is cut off, the energy stored in the primary field is transferred to the secondary winding of the transformer, rectified by the diode D201, in case of the + 17V, and filtered by C202 and C203. The filter has a low reactance at the operating frequency and in effect shunts the AC ripple to ground and leaves the DC component. By adjusting the duty cycle of the on versus off time of the switching transistor, we can adjust the amount of energy that is stored in the primary field and transferred to the secondary, thus controlling the secondary output voltage. The IC used to regulate the DC voltage and the duty cycle is a specially designed IC, a TDA 4601.

One of the principle advantages of a SMPS is that the frequency of operation is much higher than a power line frequency type of power supply which permits the use of much

smaller transformers and filter capacitors.

2. Start Up.

When the projector is switched on with the main power switch, the 110VAC is connected to a input doubler circuit which in effect doubles the 110VAC to 220 VAC. This voltage then goes to the fullwave bridge rectifier (D100-D103), and the rectifier delivers +300 VDC to the power supply transformer primaries. This 300 VDC starts a free running oscillator, composed of Q1 and Q2 and T1, on the subunit (coor.B 1-2) Pins 11 and 12. The grounds of the secondary of T1 are connected to **Cold ground** , so that should be corrected if necessary in the service manual. The + and -9 volts are developed from D1 and D2 and C4 and C5 and zeners Z1 and Z2 are used to regulate the output to + and - 9 volts DC.

The plus and minus 9 volts is sent to the controller board for standby power.

When the on/off signal (J4 pin 3 sub-unit coordinate B-4) produced by the orange standby button on the control unit , becomes "low" , the LED of the opto-coupler Ic1 will light up and Q3 will be cut off because the base of Q3 is pulled to ground. This will allow the gate of Thyristor THYR1 to go positive and turn on the Thyristor (gate controlled diode), causing 11 volts DC to be connected through D104 to IC100 and IC 102 pins 9, turning on the both IC's. Once Ic102 is operational, the voltage on the secondary winding of T2 (P22, P24) will provide the operational voltages for the two IC's. Once this happens, D104 sees 13 volts DC on its cathode, and it becomes reversed biased. At this point the cathode voltage of THYR1 is equal to the gate voltage, and THYR1 turns off.

The time constant of R113-C113 on IC100 is longer than the time constant of R130-C121 on IC102. The IC will not start until pin 1, the reference pin reaches 4.4 VDC. C121 delays this charging of pin 1, and therefore this causes a **slow start** of the IC. The C113 connected to pin 1 of Ic100 is much larger than C121. This results in a slower startup of IC100 to make sure that the HTHD voltage is only available after the supplies controlled by IC102 and T2 are already on and stable.

When the projector is turned to the standby condition, the on/off (J4 pin 3) signal becomes " **High** " turning off Ic1, and Q3 on the subunit turns on. This pulls down pin 5 of IC102 (external blocking pin) which shuts off IC102 through D105. Pin 5 is the input on the TDA 4601 that monitors the main voltage and if it goes too low (below 5.5VDC), the IC will shut off. The monitoring of the 300Volts DC is through the divider R123, R122. If IC 102 shuts off, the supply to pin 9 of IC100 will also be turned off, disabling both IC's. This will leave only the standby power supply operating.

3. Control loop of the stable or fixed voltages.

All the stable or fixed voltages are delivered by the first part of the Switched Mode Power Supply, formed by IC102, Q101 and T2. The secondary winding P20-P22 of T2 provides a negative feedback voltage after rectification through D111-C118-C119. A reference voltage, coming out of pin 1 of IC102, comes up slowly through R130-C121, providing a slow start to the switch mode.

A simulation of the collector current of Q101 is made by charging C117 through R124 from IC102 pin 4. This creates a sawtooth ramp voltage and the switching point of the IC is determined by the control voltage on pin 3, the control pin. When the voltage on C117 reaches a certain level, the capacitor is discharged by the control logic of IC102.

The higher the control voltage on pin 3 of the TDA4601, the higher on the sawtooth ramp before the IC pulses Q101. Therefore the feedback voltage from pin 3 , will modify the the **pulse width** of the driving pulses.

The negative feedback voltage developed by D111 is compared with the reference voltage in the voltage divider network through R131-R125 and P100, the 17 volt adjust pot. This combined voltage is fed into pin 3 of IC102 and by adjusting P100, we can adjust all the secondary voltages developed by T2.

A feedback signal is fed through R127 to IC102 to provide a zero passage identification for making the SMPS more efficient. This zero passage insures that the only time the transistor is switched is when there is no energy in the field in the transformer. From this AC voltage sent to pin 2 of the TDA4601, the IC can determine when the current in the transformer is crossing the Zero point.

Divider network R122-R123 provides an input voltage to pin 5 of the TDA 4601, which is relative to the 300VDC main supply, to turn the IC off in case of the Main input voltage dropping too low. Pin 5 must be at least 5.5 VDC for the IC to operate. If pin 5 drops below 5.5VDC, pin 7 goes to ground and grounds the drive pulses from pin 8 , thereby turning off the supply.

Diode D112 is connected to winding P18 and produces 17V DC referenced to Main or HOT ground. This supply is only used by the EHT generator board because that board also is connected to the Main 300V DC input. .

Control loop of the HTHD (Horizontal Deflection High Voltage).

The supply voltage for the horizontal deflection circuit has to change , when the horizontal frequency of the projector changes. A separate power supply is provided to deliver this voltage. This supply is formed around IC100, Q100, and T1.

The reference voltage of IC100 pin 1 is also integrated by means of R113, C113 , to provide a delayed start. The width of the driving pulses produced by IC100 can be varied by modulating the voltage on pin 3 of that IC. When the voltage on pin 3 is lowered the duty cycle will be shorter and less energy will be sent to the transformer to regulate the voltage. The (FBHD) feedback voltage is used for this purpose. The **FBHD** is the feedback Horizontal Deflection voltage from a transformer on the Horizontal Deflection board. This primary of this transformer is connected across one of the horizontal deflection yokes, and the secondary output voltage is rectified and is proportional to the width of the raster on the CRT.

The secondary winding P13-P17 provides the zero passage identification through R109-R110-R111 and over voltage protection through D108-C108-Z101. As soon as the rectified negative voltage across C108 passes (51+5) 56 volts, pin 5 is pulled low and IC100 switches off.

5. Feedback control of HTHD.

The feedback loop consists of a 5mA current source (Q7), Z7, and a controlled reference voltage (Z8, R28 ,R29) and a opto coupler IC5. This is located on the sub-unit schematic.
The current source supplies Z8 with 5 mA to achieve a HTHD independent reference voltage. Z7 is connected between the collector and emitter of Q6, and limits the C-E voltage across Q6 to 7.5 V DC., minus the drop across Ic5, D10, the Green LED, and R37.

FBHD (Feedback Horizontal Deflection J4 pin 7 sub-unit) is a rectified positive DC voltage proportional to the current flowing through the deflection coils. This voltage modulates the current through Q6 which in turn controls the current through the opto-coupler LED, pins 1 and 2 of IC5. When the FBHD increases, due to a higher deflection current, the current in Q6 increases. This causes an increase in IC5 LED current which causes the transistor in IC5 (pins 4 and 5) to increase it's conduction, and in turn the FB2 voltage to IC100 pin 3 is pulled towards ground. This results in shorter driving pulses for Q100 and a lower secondary voltage output voltage.

E (FBHD)	increases
I Q6	increases
I IC5	increases
E IC100 pin 3	decreases
E HTHD	decreases

1. Protection against a disconnected FBHD loop

The problem with an open feedback loop is that the control voltage is lost and the IC may think that the output voltage of the circuit is much too low and try to increase it, when in fact the voltage may be actually too high. When the FBHD voltage is not connected to IC4 pin 5 , the non-inverting input of IC4 goes low, causing the output of IC4, pin 7 to go low. This low voltage forward biases Q8, and pulls the emitter of Q8 to ground, which turns on the LED in IC5. This will lower the voltage on pin 3 of IC100 and lower the HTHD voltage to about one-half it's normal value. This low voltage will be insufficient to produce horizontal scan, and the projector will go into "scan fail".

2. Protection against undervoltage of the +17 volt supply.

To prevent damage to the Power-Mosfets of the Horizontal Deflection circuit, the + 17V supply must not drop below 14 volts. The Power-Mosfets are driven by circuitry supplied by the 17V supply. If the 17 volts is too low, the Mosfets are not fully turned on, due to insufficient drive, and the internal resistance will be too high , causing them to overheat. When this happens, the HTHD must be switched off immediately.
The + 17v supply is compared with a reference voltage in IC3, (pins 5, 6, and 7). This reference voltage is derived from the +30v supply and clamped by adjustable zener Z6. Pot P1 is set for 14V , and when the 17 volt supply goes below 14 volts, pin 7 of IC3 goes low and turns on Q8 through D7 and the HTHD goes to about one half it's normal value. R17 and D6 prevents oscillations in the circuit. The 30V DC line is used for the reference voltage, since it would have to drop almost in half, to make the reference voltage inaccurate for circuit operation.

3. Overvoltage protection.

A high voltage protection is provided around pins 1-2-3 of IC4 and transistor Q9. The HTHD voltage is divided across resistors R38 and R39, and compared to a reference voltage formed by R40 and zener diode Z10 from the 30 volt line. When the HTHD becomes too high, the output of IC5 (pin 1) will go high, and trigger Q9. Q9 causes the LED in the Ic5 to turn on, and pull pin 3 of Ic100 low, and greatly reduce HTHD. The HTHD goes to about one half it's normal value in this condition. The unit has to be powered off, to reset the circuit, because the diode D8 locks this condition on by holding pin 3 of Ic4 high, until the unit is powered off.

4. Overcurrent protection.

To protect Q100 and Q101 on the main board against excessive current flow, the voltage across R106 and R121 are compared with the internal reference voltage of IC100 and IC102 in the Op-Amp IC101. When the current becomes too high, causing a higher voltage across either R121 or R106, which are in series with the emitters of Q101 and Q100, IC101 pin 1 or pin 7 goes low and pulls down pin 3 of IC100 or IC102. This shuts

down the supply that has the excessive emitter current flow.

5. The horizontal amplitude regulation.

The Horizontal Amplitude voltage which is adjusted by means of the projectors remote control, controls the reference of Z8 through IC3 (pins 1, 2, and 3) on the sub-unit. When the amplitude of the voltage increases on inverting input pin 2 of IC3, the control voltage to Z8 will decrease and the reference voltage on Z8 will rise, which decreases the conduction of Q6 by setting the emitter to ground voltage of Q6. This will cause the LED in IC5 to conduct less, and pin 3 of IC100 will rise. The driving pulses for Q100 will be extended, and the output voltage HTHD will rise, causing a wider horizontal deflection.

We can limit the maximum amount of current that will flow through the horizontal deflection coils by adjusting P2. This will determine the conduction point of Q6, and therefore the maximum amplitude of the Horizontal Width. The HTHD voltage should be set using composite video. After checking to make sure the throw distance is accurate, display composite video on the screen, adjust the horizontal size to 99 on the bar scale, and with the blanking fully open, adjust P2 on the sub unit, until the video slightly over-scans the screen. HTHD should then read between 47VDC to 52 VDC.

BG-800 COMPONENT CLASS

QUAD DECODER

76 1753 76-1822

Introduction.

The composite video signal is split up into a luminance signal and a chrominance signal, and processed separately. The S-VHS signal is already separated at the source and processed the same as the composite signal.

The luminance goes through a enhancing or sharpness circuit, and the chroma information is blocked. The luminance then goes to IC4, containing the luminance delay line. (TDA 4565)

The chrominance information passes the correct bandpass filter and reaches pin 15 of the quad decoder IC2 (TDA 4557).

The **NTSC 3.58Mhz** passes the comb filter (DL1) before entering pin 15 of IC2

The color difference signals are then regulated in amplitude by two potentiometers in IC3 (Bella) , and then go to IC4.

The Y signal, the R-Y and B-Y signals are processed and the RGB signals are matrixed and leave the decoder board, and go back to the RGB Analog and Switching Board for text insertion.

The brightness and contrast control is accomplished on this board. Then the signals are ready for the RGB power drivers.

In case of the 76-1822 Quad Decoder with Gain control, the Red and Blue black level and gain is adjusted on the sub-board, as well as brightness and contrast.

The CP clamping pulse is formed to be utilized in the brightness control circuit and on the RGB switching board.

The blanking pulses for the horizontal retrace time, and the adjusted left/right blanking (user adjusted), are combined with the vertical blanking pulses produced on the UN SYNC + VERT deflection board in order to get a total blanking pulse train which is then sent to the RGB driver output boards.

We will now cover these items in more detail.

1. Video Composite Signal Flow.

Enhancing;

The composite video arrives at the base of the buffer Q1 and feeds the delay line DL3. The middle tap of this delay line supplies the base of the buffer Q2.

The signal then goes from Q2 emitter to the chrominance bandpass filters PAL/N4 and SECAM , and to a buffer in IC1 (Pins 12, 13 and 14).

The output, pin 13 of DL3 is delayed twice as much as the pin 8 output, and obviously at the node C3/C4, we obtain the sum of the delayed and non-delayed signals.

The signal is now sent to the base (pin 12) of a transistor in IC1. At the emitter of the same transistor we apply the half delayed video and since this transistor is the common emitter resistor of the differential pair , we get the difference signal at the collector of the differential pair (pin 5 of IC1).

Finally, this signal needs to be added to the delayed signal, and this happens in the third transistor of IC1 (pins 6, 7 and 8). The fourth transistor (pins 9, 10 and 11) of IC1 is a buffer for the signal, and the output goes to the comb filter DL750 via Q3 and Q4. The amount of enhancing is made adjustable by the DC voltage applied to the base of the differential pair (pins 2 and 4 of IC1). The left base of IC1, pin 2 is connected to a fixed DC divider, R25 and R26. The voltage on the right base, pin 4 of IC1 has a variable voltage which comes from BELLA IC3, VO3, pin 27. This variable voltage is the voltage that changes when you activate the sharpness control of the projector. By adding the delayed and non-delayed signals, the transient response can be augmented, causing the sharpness of the image to change. (This will be explained in by the Instructor).

NTSC 3.58 Mhz comb filter.

This comb filter is based on the principle that the phase of the color subcarrier is phase shifted 180 degrees, each horizontal line. The reason for using the COMB filter is mainly to eliminate the need for a Chroma Bandpass Amplifier and a method for removing high frequency video content from the chroma signal. Before the use of a comb filter, the high frequency response of the video amplifier chain was limited to about 3 Mhz out of a possible response of 4.2 Mhz. As a result, fine detail in the picture was limited. The reason that the limiting was necessary was ;

1. High frequency (Y) luminance signals between 3.08 and 4.08 Mhz can simulate color information and can be processed by the color circuits. This results in false colors that appear as swirls of color on such things as striped clothing, or striped ties.
2. The overlapping chrominance and luminance signals tend to produce beats that add a grainy appearance to the picture. The comb filter eliminates both of these defects.

The comb filter is based on four important characteristics of the NTSC signal:

1. The harmonic components of the luminance signal are spaced at intervals equal to the scanning rate.
2. The color harmonic components fill the space between the luminance harmonics by being an odd multiple of half of **the** horizontal scanning rate. This results in the chrominace signal reversing phase from one horizontal line to the next. It is this comb-like relationship that gives the comb filter it's name.
3. Adjacent successive horizontal lines of luminance are almost identical.
4. All components of the composite video signal have definite phase or timing relationships at the start of each horizontal line.

The comb filter is able to separate the luminance and chrominance signals by delaying the composite video signal by one horizontal line, and then adding and subtracting this signal from the composite video signal. When the signals are in phase, they add, and when they are out of phase they cancel. By configuring the circuits, we can have twice as much chroma, and no luminance, or twice as much luminance and no chroma. Buffer Q7 provides only chrominace and Q8 provides only luminance. P1 is used for Chroma Null adjustment.

The luminance signal then goes through Q8, Q9 and Q10 to C20 and then to IC4 pin 17.

2. CHROMINANCE FLOW.

The multi-standard decoder IC2 sequentially scans the information on the backporch of the horizontal sync from the signal on pin 15 of IC2. As soon as the correct signal is identified by IC2, the appropriate output PAL/SECAM/N4/N3 goes high (IC2 pins 25-28). This output activates the correct chrominace bandpass filter and oscillator (crystal).

The tint control from the Bella IC3 (pin 26 of IC3) is sent to pin 17 of IC2, hence the tint can be adjusted.

The SC (sandcastle pulse) is supplied to pin 24 of IC2.

The chrominace delay line DL2 is only used for Secam and PAL, and for the latter, the phase and amplitude of the delayed and non-delayed signals are aligned with L8 and P4

respectively.

In SECAM, the (R-Y) amplitude and the zero point of the frequency discriminators are aligned with P3 and L7. B-Y is aligned with P2 and L6.

Finally the -(R-Y) and -(B-Y) signals exit IC2 on pins 1 and 3 and proceed to the digital pots in IC3, where the amplitudes are adjusted via the I2C bus signals from the controller board. Adjusting the amplitude of the R-Y and B-Y signals adjust the color saturation of the picture.

The chroma then goes to IC4 , where the color transitions are improved, and then the signals leave at pins 7 and 8 of IC4.

3. COLOR MATRIXING.

The (B-Y) and (R-Y) are added at the base of Q16. The ratio of addition is fixed in order to get the (G-Y) at the collector of Q16. After the signal is buffered by Q26, it is fed to the base of Q17. The R-Y and B-Y signals are added to the Y signal from IC4 pin 11 to produce R and B. The R-Y and B-Y plus Y at Q17 produces G.

All three signals, red, blue and green are sent to the RGB switch board where the INS and pixel information is added.

The R, G and B signals then come back to contacts 2, 4, and 6 of the J4 connector and are introduced to IC7, the LM1203, the RGB video amplifier IC on pins 4,6, and 9

4. BRIGHTNESS AND CONTRAST CONTROLS.

A) CONTRAST:

The contrast voltage is adjusted in IC5 (exits pin 24 of IC 5) and delivered to the base of Q37 (pins 1 and 2 of switch S1 are shorted together at the factory). For service reasons, pins 2 and 3 of S1 may be shorted together to put a fixed bias on Q37 for troubleshooting purposes.

The contrast control voltage that is applied to pin 12 of IC 7 can be limited by the following :

- the IBCL information, that comes from the RGB output boards, and is relative to the CRT beam current.
- the BCL information, which is a negative voltage that comes from the EHT transformer via the EHT board (HVL). This voltage is a result of the sum of the three CRT currents and is proportional to the current generated by the EHT.

- the presence of D30 (schematic coordinates H-6),
means that the voltage cannot drop below the node voltage R146/R147.

B) BRIGHTNESS :

The brightness control voltage at the VO1 output of Bella IC5 goes to pins 15, 19 and 24 of IC7, the RGB video amp.

Pins 3 and 2 on S2 are shorted at the factory (schematic coordinates I-8) and for servicing, 1 and 2 can be shorted to apply a fixed voltage to pins 15, 19 and 24 of IC7.

The CP (clamping pulse), available from the collector of Q32, is also applied to pin 14 of IC7 through buffer Q40, and is used for brightness control.

5. CLAMPING PULSE CP.

The clamping pulse, CP, utilized by the brightness control and the DC restoration on the green of the RGB Switching board , is formed as follows:

1) In the VID, S-VHS and RGsB mode (sync pulses in the blanking time)
" Note that in the S-VHS mode, the + VID lines is high (See RGB switching Board Schematic)

In this mode, the original sandcastle pulse (SC), may be used to clamp on the backporch of the blanking. In the + Video mode, Q29 is turned on and through C81, the pulse is integrated for video only.

In either case, transistor Q30 (schematic coordinates H 5-6) is saturated, eliminating the lines pulses from J7A pin 27, from driving transistor Q31. (correct schematic, coordinate C-7 , J7B pin 11 should be marked J7A pin 11 and labeled **SC** for sandcastle rather than G1).

The SC arriving on J7A pin 11 is coupled through Q55, when Q55 is biased on by either +VID or +RGSB and because of the threshold set on Q31 emitter by R164, only the small top pulse of the SC is found on the collector of Q31.

2) In the TTL and RGBS mode:

The line pulse from J7B-27 is applied to the base of Q31, because Q30 is biased off. Now This Line Pulse now becomes the clamping pulse in TTL and RGBS mode.

A small pulse, coinciding with the start of the blanking time is available on the collector of Q32.

6. LEFT / RIGHT BLANKING.

Capacitor C88 (schematic coordinates D8), is charged up from the HTHD line through R175/R174 and discharged through Q33 each time a line pulse is sent to it's base.

The horizontal sawtooth waveform generated by Q33 and C88, is the input for 2 level detectors in IC6 (IC6 pins 2 and 5).

Two digital pots in IC5 (IC5 pins 26 and 26) feed the other inputs in IC6 and determine the duration of the blanking pulses at the parallel connected outputs. The pulses are buffered by Q41 and leave the board from the emitter of Q41 to J7B pin 19 (BL).

7. COMPOSITE BLANKING.

The VBL pulses, sum of the top/bottom and vertical retrace blanking pulses and the scan fail blanking from the Sync Vertical Deflection Board, are mixed with the LP pulses taken from the node D8/D9, and both are applied to the base of Q34 via a zener diode Z4 and the divider R176/R177, where they are amplified and mixed with the previous left/right blanking.

The total composite blanking then leaves the decoder board and goes to the RGB output boards.

8. SPOT SUPPRESSION AT SWITCHING OFF.

When the projector is operating normally Q35 is on, and C111 charges to 15VDC, and C110 charges to 150VDC due to the voltage divider from the 230V line and zeners Z5 and Z1.

When the projector is switched off, the +17volts drops faster than the +230 volt line. **(correct in schematic coor E-8 the lower transistor marked C23 should be C35. The transistor higher and to the right should be marked C36)** The sudden voltage drop at the collector of Q36 caused by Q35, which is normally on, turning off, puts Q36 into saturation because of the bias from R221. This causes:

- the base of Q41 (schematic coordinate F-7) via D40 and C111 to blank the cathodes (RGB Outputs) . (note: this voltage is limited to 15 volts by Z5)

- the G1 via capacitor C110, to go to a negative 165 volts.
  this voltage is limited to (150 + 15 volts) with Z1 and Z5.This voltage would be a negative voltage on the G1 grid of the CRTs cutting off any beam current.

76-1822 Decoder board with Gain Control

Much of the circuitry of this board is the same as the 76-1753 board previously discussed. The main difference is this board has a sub-unit that includes IC3. The RGB signal goes into IC3, from the RGB Switching Board, on J1 on the sub-unit. The Green signal exits IC3 on pin 16, and goes IC50 to J3 and eventually to the CRT Output Board. The contrast control voltage enters IC3 on pin 12. The brightness control voltage enters IC3 on pin's 15, 19 and 24. RGB sharpness, which is really a high-frequency roll-off circuit is located at coordinate C-6 on the sub unit. It consists of 3 varicaps D1,D2 and D3 to ground on each color input line (R,B and G). The capacitance of these varicaps can be adjusted by a DC voltage via Z3 adjustable Zener and Z1. Changing this DC voltage changes the capacity, and therefore the reactance to ground. The higher the capacitance, the more high frequencies are attenuated. This is adjusted by the sharpness control on the RCU.

The Red signal from IC3 pins 24 and 25 is applied to Q2. Q2 also receives a Line Pulse via IC4, and during blanking , a fixed DC level is then applied for IC111 to utilize for brightness level reference. The Blue signal exits IC3 pins 20 and 21, and through Q1 and Q3 arrives at IC81 pin 16 (video in). IC81 and IC111 have adjustable gain and this gain is controlled by the voltage on pin 4 of either IC. This is the **White Level** or contrast for either Red or Blue, set at the brightest bar on the video grey scale pattern. The black level is adjusted on IC81 and IC111 on pin 6 (clamp+) of either IC. Both of these adjustments, while level and black level, are adjusted in the **COLOR BALANCE portion of the Random Access Menu. Bella IC1, controls the voltages to IC81 and IC111.**

The Red signal from IC111 pin 8, then goes to IC110 and then back to the main board and to the Red CRT Driver Board. The Blue signal from IC81 pin 8, goes through IC80 to the main board and to the Blue CRT Driver Board.

BG-800 COMPONENT CLASS

RGB ANALOG INPUT & SWITCHING BOARD

76 1748

INTRODUCTION:

The projector can operate in five different modes.

1). Video
2). Super VHS
3). RGB TTL
4). RGsB
5). RGBS

These different signals are selected on this board by means of 5 different current generators. When one of these current generators is selected, it activates a differential amplifier associated with it, and this differential amplifier passes the desired signal.

The selection voltage is obtained from a BCD/ Decimal decoder, which is directed by a BCD coded signal from the I2C bus.

The text pixels from the TXT block on the control panel are added and the video is blanked with the **INS** (insert) signal whenever it is required.

In order to maintain the insert level for the green text, the G-signal undergoes a black level clamping.

The turning off of different colors in the adjust mode takes place on this board

A. Mode Selection.

The signal from the I2C bus enters IC2 (8574 interface IC), and the output ports P4 through P6 are connected to the BCD/Decimal Decoder IC3 input. The output of the Decoder IC drives the base's of the switching transistors Q151 to Q155. The collectors of these transistors supply the 5 switching voltages (+ Video, +SVHS , +TTL , +RGsB, +RGBS) needed to drive the 5 different current generators. These voltages also are connected to the 5 green LED's on the board (D157 - D161) to supply a visual indication of which input is selected.

B. Composite Video Input:

The + video voltage from Q151 activates the current generator Q10 of the differential amplifier input stage Q11-Q12. The video is now applied to Q121 and Q122 via D14. Q122's output feeds the decoder (J6B pin 3) and Q121 feeds the sync separator on the UN SYNC+ Vert Defl Bd (J6B pin 4).

After the video is decoded into RGB on the decoder, it returns to the RGB Analog board on Q200, Q300 and Q400. These transistors are turned on by the + video voltage via D152, D154 and D164.

The Y-input from J6B pin 7 does not effect this circuit when composite video is used, because the collector of Q21 is clamped by D25 to the +12 volt supply because D25 is forward biased by the +17v' supply through R29. This prohibits any S-VHS luminance signal from reaching the decoder, when in composite video mode.

C. S-VHS Input

The Y (or luminance) and Chrominance inputs are now active with the +SVHS voltage through Q20 and Q30. The Y signal proceeds to the decoder and to the sync separator, whereas the chrominance is sent to the decoder only.

Diode D15 clamps the collector of the video input to AC ground as in the above example of composite video, through the +17v' line and R19.

The decoded S-VHS returns from the decoder back to the RGB Analog board, to the bases of Q200, Q300 and Q400. At the same time D159, the S-VHS LED is illuminated via D151, and Q152.

D. TTL Input.

The + TTL voltage leaves the board at J2B (26) for the TTL input board, to supply the board with voltage for the regulators on the TTL input board.

The same +TTL voltage supplies the bases of the emitter followers Q200, Q300 and Q400 via D156.

The TTL signals enter the bases via gating diodes, D200, D300, and D400

The +TTL voltage supplies D161, the TTL LED.

E.RGB Analog Inputs.

Depending on the selection of either RGsB or RGBS, three or five inputs are

activated , and the appropriate sync is guided to the sync separator.

The three current sources, Q201, Q301 and Q401, in the open collector configuration (the 75 ohm collector resistors are located on the decoder board), are directly supplied with these signals via Q61-d64, Q81-D84 and Q101-D104. Sync on green is added via Q82, Q125 and Q124.

F. DC Clamping of the Green Black Level.

The Green signal at the emitter of Q301 is applied to the base of a differential amplifier in IC4 (IC4 pin 4), the other base (IC4 pin 2) is fixed at a voltage set by R315/R314. This differential pair is only turned on when a clamp pulse from the decoder board (**CP**), is applied on the base of the internal transistor in IC4, pins 6, 7, and 8. Thus, the circuit samples the blanking level, due to it's timing relationship to the clamping pulse used to gate the circuit. The differential between the two collectors in IC4 is amplified by Q 304 and Q305, and the charge across C303 changes with the black level. This C303 voltage, effects the bias of Q402, and the black level through the changing bias of Q301. The changing bias on Q301, changes the gain of that stage. This circuit works in the same fashion as an "KEYED AGC" circuit, for the Green signal.

G. Cut-off of one or more Guns.

When the strap (J7 coordinate H 4-5) is in place, and Q500 is switched on (during the scan only), the output of current generators Q201, Q301 and Q401 are clamped at ground via a diode, when one of the FETS; Q203, Q303 or Q403 is fully saturated. Q500 is the ground return for FET's Q203, Q303 and Q403 when the J7 strap is in place.
The **CP** (clamping pulse) is fed into the PNP transistor Q500, and this positive going pulse turns of Q500 during retrace. At the retrace time, Q500 then has a fixed bias determined by zener diode Z500. The video amplifiers on the Quad-Decoder board also have a black level clamping circuit, and if the Red, Blue or Green signals were grounded during the blanking interval, Black level clamping in the next stage would not work properly. This is the reason that Q500 turns off during the Clamping Pulse, and a fixed bias is inserted from Q500 collector to ground. Then the Quad-decoder black level clamp and use this fixed voltage as a reference. The three FET's are driven by the P0- P2 signals from the I2C interface IC2. When one of these FET'S are on, the diodes D202/D207, D302/D307 or D402/D407 pull down the collectors of the R, G, B amps, as well as the RGB Pixel information.

H. Insert

This signal, produced on the controller board (TXT Block), clamps the outputs of the R, G , and B drivers under black level to blank the video, so that a window will be created, in which the text can appear. This insert signal comes in on IC1 pins 11 or 13. The text

enters IC 1 ,pins 1, 3 and 5.

I. Fast/Slow.

The output P3 of IC2 drives transistor Q150, whose collector is connected to pin 13 of the TDA2595 on the UN SYNC + VERT DEFL.

J. Forced Video.

Jumper strap J8 is connected to force video operation, to bypass the I2C bus, as a troubleshooting aid.(schematic coordinate D-3) Actually, any of the inputs can be forced on by connecting the collector to emitter of any of the switching transistors, Q151 through Q155.

K. Enhanced Blue.

Transistors Q511 and Q510 form the enhanced blue circuit. The purpose of this circuit is to couple some of the Blue signal into the Green channel, in the event that you have Blue text from your source, and it is difficult to read.

Q511 is normally on. When "Enhanced Blue" is selected in the "Random Access" menu, Q511 is biased off by a voltage change from IC2 pin 12. When Q511 is biased off, it's collector goes "high", and allows Q510 to turn "on". Q510's base is connected to the Blue channel, and it's collector is connected to the Green channel. This allows some Blue signal to enter the Green channel, making the Blue text more readable.

BG-800 COMPONENT CLASS

N-S CORRECTION
76-1765

The North-South Board:

The North-South Board performs several functions.

1) This board develops the signals used in the vertical yoke circuits to correct for the geometry distortion cause by the horizontal shifting of the outboard CRT's to statically converge the image in the center of the screen. The blue and red CRT's will have a vertical error in the rasters on the screen due to the fact that the CRT's are not perpendicular to the screen in the horizontal plane. The North-South correction signal adjusts the vertical height of the raster along each horizontal period, to neutralize this error. The error appears as a stretching of the vertical portion of the raster, as the distance to the associated CRT is increased. In a floor mount front configuration, the red CRT is on the left side of the projector. The left edge of the red raster is closest to the red CRT, and the right edge of the red raster is further away from the CRT. This causes the right edge of the raster to be stretched vertically. The opposite effect would happen with the blue raster. The blue tube located on the right side of the projector would cause the blue raster to be vertically stretched on the left side. The North-South correction signals, are added in the Vertical Yoke circuits, to eliminate this error. The closer the projector is to the screen, the more the outboard tubes are angled in, and the more North -South correction is needed.

2) The North- South board also controls the Horizontal Shift voltages, which are used to horizontally shift the red, blue and green rasters. These shift voltages are sent from the BELLA IC400 on the N-S sub-unit, to IC110, IC120 and IC 130, and then to the three horizontal deflection coils.

North- South Correction:

The horizontal line pulse enters the North-South Board at J2A pin 23 (labeled LP on lower left of main board schematic). The line pulse goes through Q1, and Q2 is connected to HTHD. The horizontal line frequency determines the level of HTHD, and therefore the collector voltage of Q2. Q2 is the collector supply for Q1 and therefore the charging current for C2 is controlled by Q2 current. This causes the sawtooth generated on C2 by the horizontal rate firing of Q1 to have a steeper ramp at higher frequencies.

The horizontal sawtooth generated by Q1 and C2 goes through buffer IC5 pins 5, 6 and

7, and then becomes ST1 and goes to the sub-unit. (Sawtooth 1). The sawtooth from pin 7 on IC5 then goes to IC5 pin 9 and is inverted at the output, pin 8 and becomes ST2 (sawtooth 2 or the inverted sawtooth). ST1 also goes to IC6, a multiplier, where a parabolic waveform is formed. The parabolic waveform exits IC6 pin 6 and goes to buffer IC5 pins 2, 3, and 1 and then to J3 pin 6, and to the sub-unit. This line is marked "PAR". The parabolic waveform on IC5 pin 1 feeds IC5 pin 13, and is inverted on IC5 pin 14. This is the HPAR waveform which connects to the focus board for left-right electronic focus correction.

IC4 on the main board (coor. B-1, 3, 5,) receives a vertical sawtooth from the vertical output circuit on J2B pin 32 (VDLB), and this connects to pins 6, 8 and 11 of IC4. The outputs of IC4, pins 1 ,14 ,and 13 have a vertical rate square wave (top- bottom switch) that is used for the top-bottom circuits on the sub-unit. These signals are on the lines labeled BCOMP, RCOMP and GCOMP. These top- bottom square waves feed the multiplex IC's on the sub-unit, IC204, IC205 and IC206.

The multiplex IC's switch the ST1 and ST2 and PAR signal to the Bellas, IC'S 200, 201 and 202, depending on whether the vertical is at the top half or bottom half of the screen. The "comp" signals enter the multiplex IC's on pins 11,10 and 9. When the comp signal is high, pin 14 connects to pin 13. When the signal goes low, pin 14 connects to pin 12 on IC's 204, 205 and 206. The other 2 sections of the multiplex IC work in a similar fashion. These signals are sent to the Bellas, IC 200,201 and 202. The outputs of the Bella's are matrixed in the resistor network and the total of all these waveforms are labeled STPAR. These signals then leave the sub unit at J5 pin3 (ST Par R), J5 pin 2, (St Par G) and J5 pin 1 (ST Par B). These three signals are the combination of sawtooth and parabolic correction signals for the three vertical yoke circuits, and are sent back to the main board to IC20, IC40 and IC 60, pin 1. Due to the switching of the Multiplex IC's, different adjustments can be made for the top half of the raster, and the bottom half of the raster. At the same time three DC voltages from Bella IC 203 on the sub-unit, pins 24, 25 and 26 (MB G, MB R, and MB B, refer to midline bow), connect to IC's 20, 40 and 60 pins 8, and IC4 pins 7, 9 and 11. These voltages effect the Mid-line bow by effecting the switching point on the vertical sawtooth with IC4, and by effecting the gain of IC's 20, 40 and 60. The output signals from IC's 20, 40 and 60 go to transistors Q31 to Q35 for the Blue circuit. Q34 and Q35 are configured to give a high slew rate and minimize hooking. The output of the discrete transistor circuit is connected to T30, and the center taps on the transformer VDLB and VDHB are connected to the vertical blue deflection coil. The other two circuits for Red and Blue are identical.

Horizontal Amplitude:
The horizontal amplitude control voltage is developed on IC203 on the N-S sub-unit and exits pin 27 of IC203. This voltage is sent to the SMPS, IC3 pin 2 on the SMPS sub-board, to vary the HTHD for control of the Horizontal Size of the raster.

Horizontal Shift:
The horizontal shift control voltages are developed on the N-S sub-unit, IC400, and exit the IC on pins 24, 25 and 26. Then they go to the main board IC's 110, 120 and 130 pin 1. IC 400 is also **"powered"** by the + and - Shift voltages from the SMPS. These shift voltages are from a floating winding in the SMPS, and the ground reference from these voltages is HTHD. From the plus shift to the minus shift , a voltage reading of 5 VDC will be measured. This 5 Volts can be measured on IC400 pins 28 and 14. If there is a failure in the shift voltage from the SMPS, such as a open fuse, IC400 will not have any VCC and VSS, and trying to control this Bella, will result in a "I2C communication error" displayed on screen. The current from IC's 110, 120 and 130 depending on the control voltage input on pin 1 of each IC, horizontally shifts the three rasters by creating a DC current flow in the horizontal yoke circuits. In addition, a sub-unit on the N-S board (coor. I-7) provides an ability to fine tune the center horizontal shift, to attain exact center convergence. The output of the sub-unit connects to the red and blue shift IC's.

T111, T121 and T131 are the width coils for Red, Blue and Green. The yokes are connected from **HDH** to **HDL** for each horizontal yoke.

Serial Clock and Serial Data Isolation.

The FET's Q400, 401, 402 and 403, and the two opto-couplers IC401 and IC402 are used to isolate the serial clock and data lines, referenced to chassis ground from the shift circuits in IC 400 which are supplied with a DC shift voltage referenced to a floating ground which is tied to HTHD. The HTHD voltage as we know, can vary from approximately 48VDC at 15kHz to 250VDC at 90 kHz. Because of the two different ground potentials, isolation is required to keep from damaging IC 400, or the serial clock and Data lines from the controller. Opto-coupler IC 401 and Q400 sends the SCL (serial clock) signal into IC400 pin 1. The SCL signal pulses Q400, the LED in IC401 pins 1 and 2, and the transistor in IC401 pins 7, couples this signal to IC400, pin 1. Since this is a one-way conversation, the SCL only requires one opto-coupler for isolation.

The SDA (serial Data), however is a two-way communication with the controller board. Therefore a "push to talk" type circuit is used. To receive a signal from the controller board, Q402 is normally "on", since it's gate is connected to the +5V via R407. The serial Data then goes through Q401, the opto-coupler LED pins 4 and 3 and pulses the collector of the transistor feeding pin 6 of IC 401. The SDA pulses then go through D400 to J5 and up to pin 2 of IC400. Pulses at the node of D400, and D401 turn off Q404, disabling the transmit circuit when IC400 is receiving SDA.

When IC400 sends Data back to the controller, the SDA exits IC400 pin 2, and pulses Q403 and IC402. These outgoing pulse via D402 go to SDA and back to the controller board. At the same time these outgoing pulses, turn off Q402, so that no receive can

occur, while IC400 is transmitting SDA.

Summary:

IC400 receiving SDA	Q402 On	Q404 Off
IC400 transmitting SDA	Q402 Off	Q404 On

BG-800 COMPONENT CLASS

HORIZONTAL DEFLECTION
76-1766

INTRODUCTION

On this board we find the MOSFET switching transistors, which act as switches to start and stop the current through the deflection coils. In order to obtain a very short retrace time with a relatively low scan voltage, and, as a MOSFET only may have 1,000 volts across it's drain-source , we have the switchers in series. In order to accomplish this, we have a separate DC supply that supplies IC302 with 5 volts DC across pins 5 and 8 Vcc and ground). The ground on IC302 is also the ground reference for Q14-Q19, and is marked 1,000V. The 1,000 volts refers to the maximum flyback pulse present at this point.

Because of the series configuration, and the 1,000 volt pulse on Q14-Q19, the drive signal for the MOSFETs Q14-Q19 must be isolated from chassis ground. An isolation circuit utilizing an optocoupler must be used for this purpose.

Furthermore, on this board, we find the required protection circuits such as " scan hold down", and " "horizontal scan failure detect".

Preparation of the drive pusses.

The horizontal deflection circuit uses two MOSFETS in series in order to be capable of handling the 2,000 volt flyback pulses. Therefore, two drive pulses, on different ground reference levels are required. The " bottom" MOSFET is driven by a pulse train referenced to ground level, whereas the " top" Mosfets are driven by a pulse train referenced to the mid-point of the two series connected MOSFETS. The Vcc of each optocoupler must therefore have a different ground reference.

The horizontal drive pulses developed on the " UN SYNC + VERTICAL DEFL " board, are sent to the amplifier-shaper transistor Q10. At the collector of Q10, these pulses are buffered by Q302 and reach the opto-couplers IC302 and IC303, pins 2.
The 2 opto-couplers are powered via the 17 volt line through diodes D303 and D302. D303 feeds 17VDC through R 315 to pin 8 of Ic303, and this voltage is clamped to 5.1 volts by Z304. D302 feeds the 17VDC via R310 to pin 8 of Ic302. The VCC or power ground of IC302 is the mid-point of the Mosfet switchers, or the 1000V reference. When

the flyback pulse is present during retrace, D302 becomes reversed bias and acts like an open circuit to the 17VDC line. At that time, IC302 receives its voltage from the charge stored in C307 (470mfd cap). Z302 clamps the IC302 voltage between pin 5 and 8 to 5.1 volts.
The " high" drive pulses reach the gate-source of the top Mosfets, and the " low " drive pulses, drive the " bottom " Mosfet switches. The 20 volts zenerdiodes, Z303 and Z305, prevent the gate-sources voltages from exceeding the maximum tolerable voltages of the Mosfets . These zener diodes (Z303 and Z305) also act as a negative clamp, to shift the pulse in a positive direction, after it is AC coupled through C310 and C312. Because of the floating ground, these 2 zeners become a good diagnosing aid for checking circuit operation. Connecting a DMM across Z303 or Z305, should produce a low value DC voltage when the projector is operating. If a DMM produces zero volts DC across these zeners, then either no drive signal is present, or the zener is open. This is an efficient way to check the circuit, if no isolation transformer is available. The output of Ic 302 and Ic303 is approximately 17V p-p.

Modulation of the scan voltage.

The +HTHD voltage from the main Switched Mode Power Supply is modulated in Q13 by the East-West correction signal from the Sync-Vertical Deflection board. Q26 is used to discharge the HTHD, every vertical period, by a vertical flyback pulse sent to it's gate. This eliminates any keystone problem at the top of the raster in a table mount configuration, or at the bottom of the raster in a ceiling mount configuration, due to a charge on C39, between vertical frames. This causes the charge on C39, to always start from the same place after each vertical scan, regardless of the voltage that it had across it at the end of vertical trace.

Horizontal linearity control.

The problem that arises here is the frequency dependant characteristic of the linearity coil. At a higher frequency, the impedance of the linearity coil would increase. In order to overcome this, a second coil T1, is magnetically coupled to the linearity coil, T3, and the latter is modulated by a current delivered by a Mosfet, Q1. The Mosfet, Q1 receives a voltage determined by the HTHD scan voltage and the zeners Z1 , Z2, and Z3. By choosing the voltage values of the zeners, the current flow of Q1 can be made exponential. The higher the HTHD, the more zeners conduct, and when the zeners conduct, they in effect, short out the control that are in parallel with them.(i.e., if Z3 conducts, P2 is bypassed). In that way, the pots can be set so that at different HTHD voltages, different controls are bypassed, and the gate of Q1 will see different bias voltages. This current through Q1, is in series with T1, and the coupling of T1 with T3 controls the impedance of T3, and therefore the linearity.

Protection Circuits.

a) Overcurrent protection;

If for some reason, the current in the sum of the horizontal scan coils exceeds a pre-determined level, the drive is inhibited as follows:
The wire J1-J3 (just below linearity coil on schematic), in series with the three scan coils, acts as a low value resistor and it is connected across the base-emitter junction of Q201. When a 0.6 volt or greater voltage is dropped across the wire, by the deflection current times the resistance of the wire, Q201 starts to conduct and triggers the monoflop Q202/Q203. When Q202 is switched on, it grounds the drive pulses via D202, and the deflection is interrupted by the time constant of the monoflop circuit. The voltage on the base of Q203 then begins to build via R204/ D203, and when that voltage on the base exceeds 0.6 volts, Q203 starts to conduct, the collector of Q203 goes to ground, and resets Q202 base.

b) Overvoltage protection;(scan hold down)

The flyback pulses on each of the series connected Mosfets are checked by a rectifier network consisting of a diodes D10, D11, and D12, and common decoupling capacitors. The resulting voltage is divided by R67/P3 , and sent to the voltage comparator IC1. The threshold level is set by zener Z6 at 6.2 volts DC. At the moment pin 6 exceeds this threshold, the output pin 7 switches " low ", and consequently:

1. The drive is inhibited through D14.
2. The input is kept "high " as transistor Q27 is blocked and D13 conducts via R89, too keep pin 6 of IC 1 high. This requires that the set be powered off, to reset this circuit.
3. The red LED D23 is illuminated in order to show that " hold down " has occurred.
4. As the deflection is stopped, there is horizontal scan fail, and as a result, the appropriate circuit (see further) will drop the EHT voltage and blank the three CRT's to prevent damage to the CRT phosphors.

C) Too low drive protection:

It is imperative that the Mosfets are fully switched on, so that the internal resistance will be as low as possible. Due to the large deflection current, even a small amount of excess resistance, will cause the Mosfets to generate too much heat.
This Mosfet drive pulse amplitude, depends in part on the +17 volt supply, and the voltage supplied from the 17vDC line via R319. This is at the cathode of D303 and is called the "safe" voltage. The drive signals are developed from the 17VDC and to prevent damage, due to insufficient drive, if this voltage becomes too low, Ic1 pin 1 goes low and inhibits the drive signal Via D18. At the same time via D20, the scan fail circuit is

immediately triggered. In this situation, the red " hold down " LED does not light.

D) FEEDBACK TO THE SMPS.

The scan voltage +HTHD has to track the line frequency in order to regulate the horizontal width of the picture. The amplitude of the line " flyback pulses " is a direct result of the horizontal width and can consequently taken as a reference. These pulses are rectified by D16 (coordinate C-1) and the FBHD voltage is sent to the SMPS, to regulate the HTHD. This voltage is proportional to the width of the raster on the CRT face. At normal width, at the cathode of D16, it reads approximately 475VDC. This voltage is then sent to the SMPS for feedback to regulate HTHD.

E) Horizontal Scan Fail.

Horizontal pulses are fed into transistors Q4, Q5 and Q6. As long as there are horizontal pulses on the base of these transistors, they are conducting for each horizontal period, and the collectors are held " Low " by C3, C4 and C5. If a horizontal pulse is missing, that collector will go to +17v' , and through D2, D3 and D4, Q7 will be turned on and when it's collector goes " low", the SF terminal will be pulled low and the scan fail signal condition will be met.