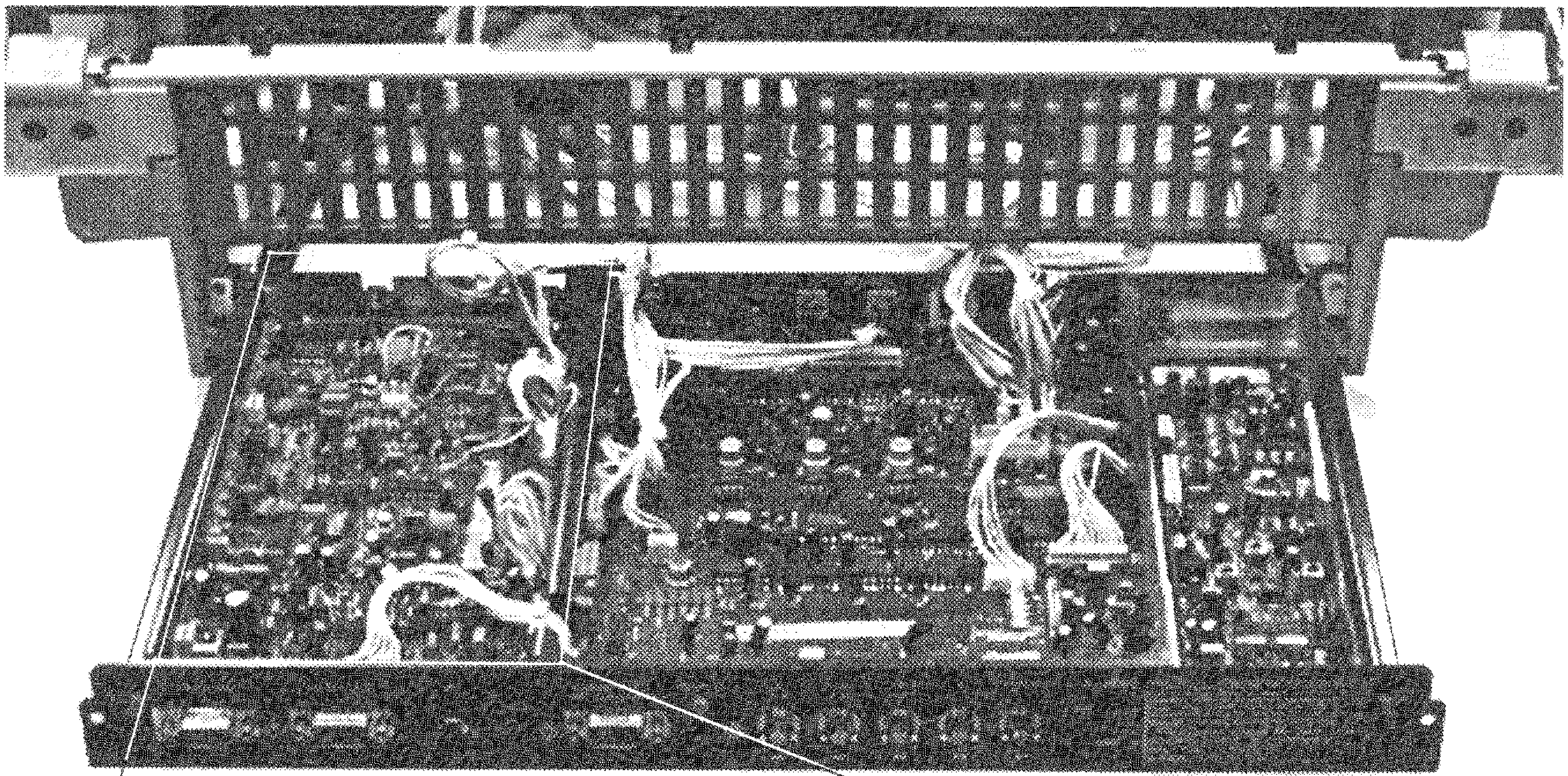
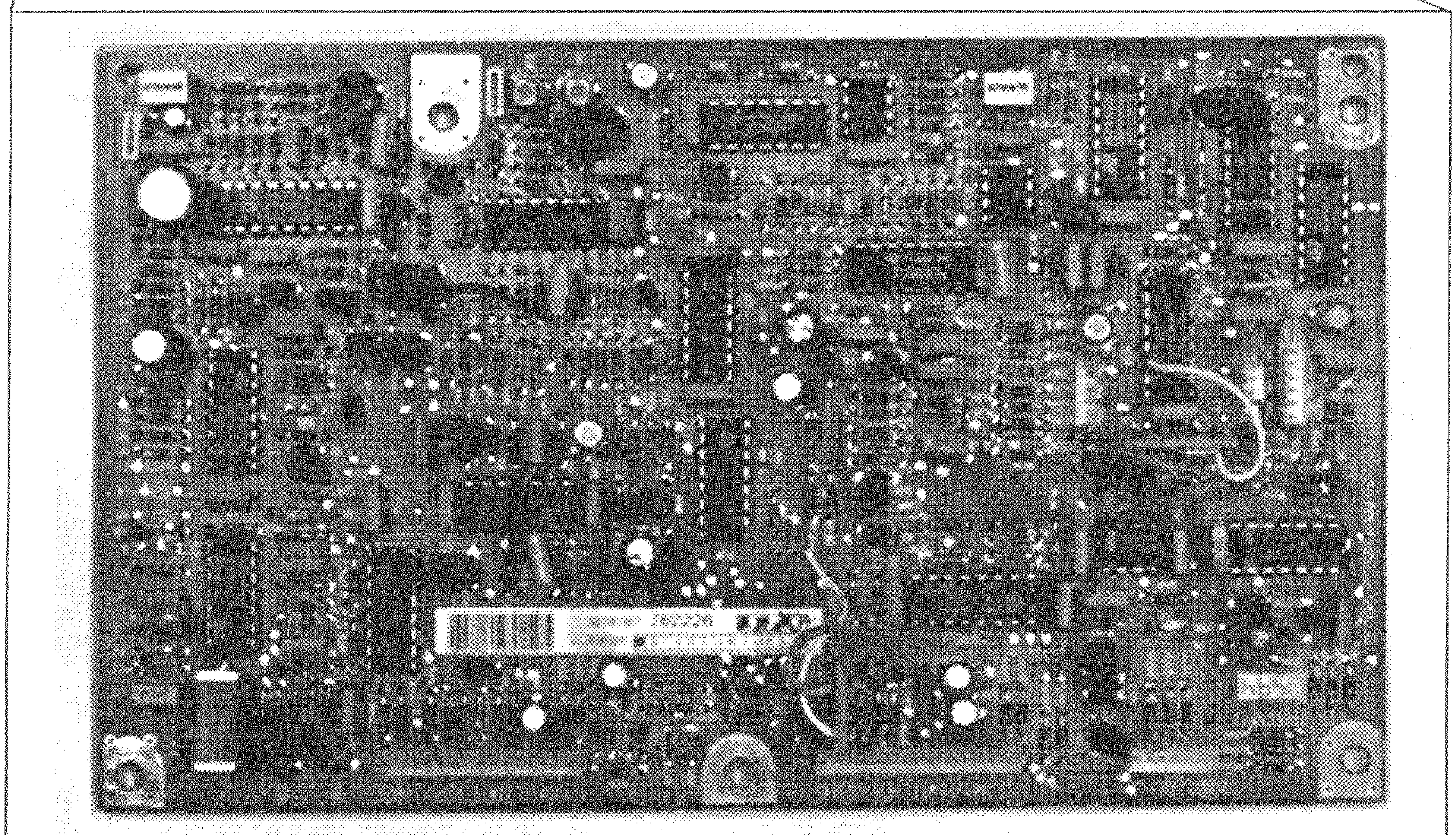
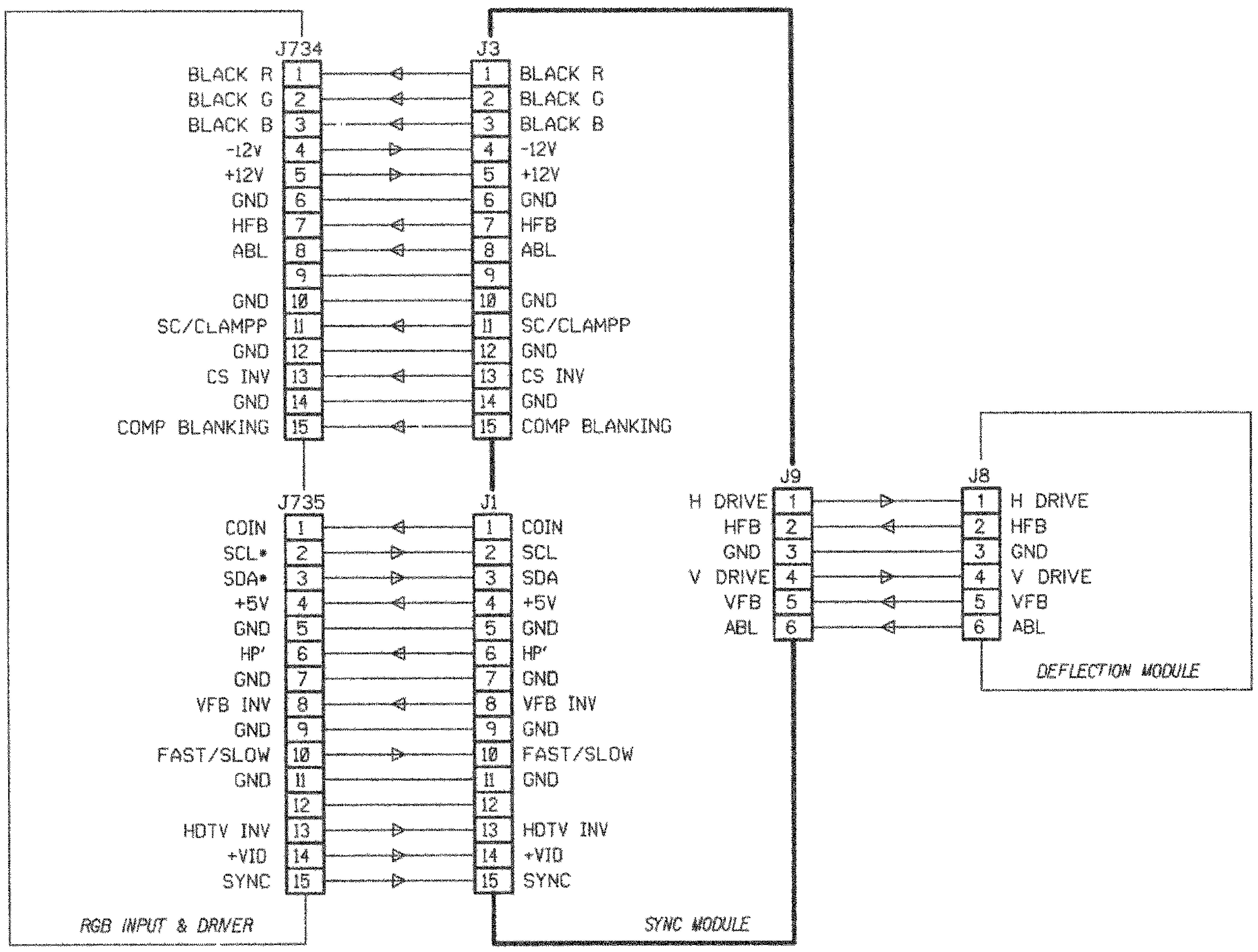




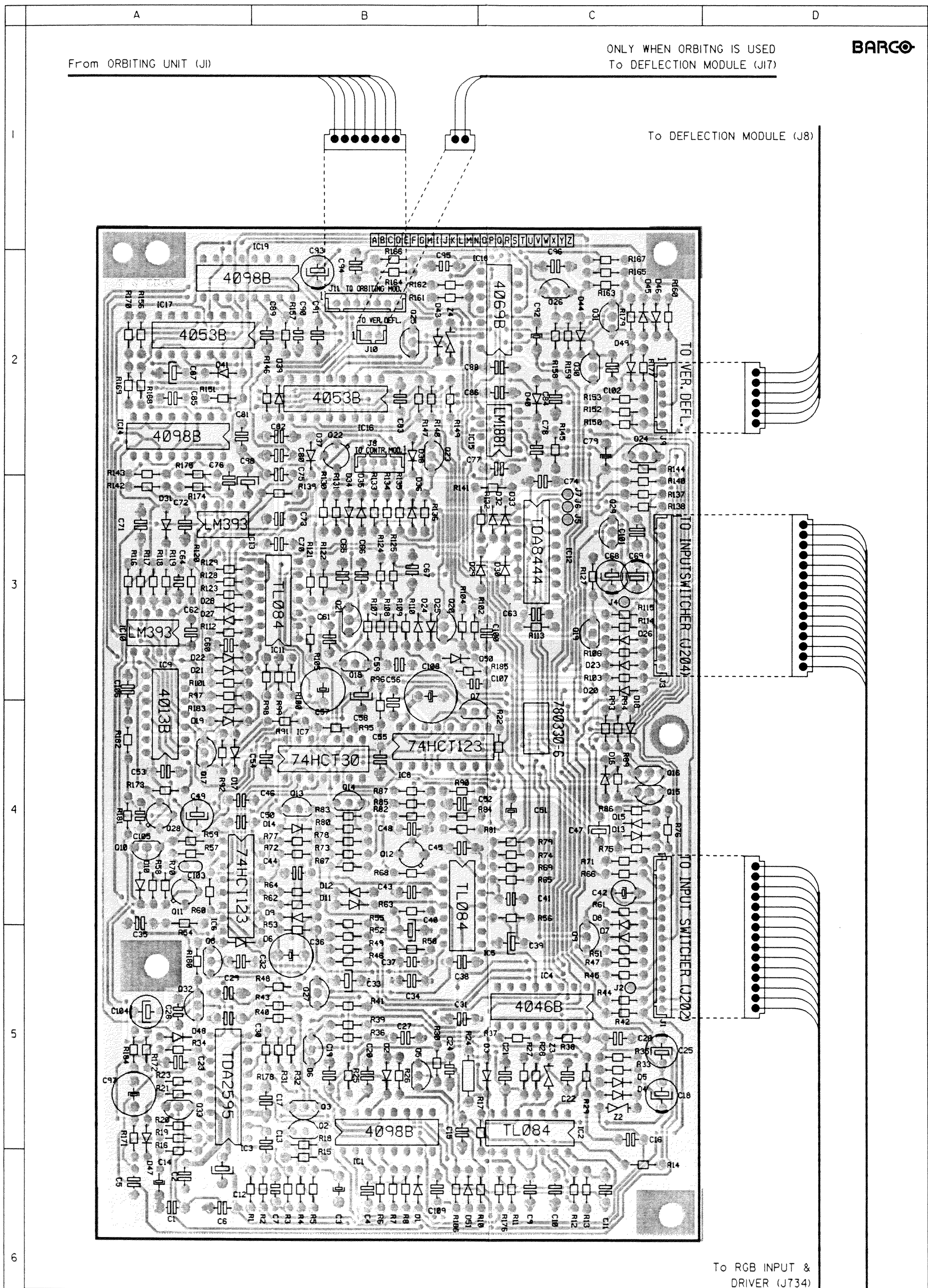


Name Interconnection SYNC MODULE		Article nr. 76 2489
Date 20-04-1995	Drawn JVDY	Checked CHT

BARCO PROJECTION SYSTEMS

Modification reserved

Sheet 1



Name	Article nr.
SYNCHRONISATION	76 2489-6

Date	Drawn	Checked
26-04-1995	JVDY	CHT

BARCO PROJECTION SYSTEMS

Modifications reserved

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C4	B 6	D28	A 3	R46	B 5	R183	A 4
C5	A 6	D29	C 3	R47	C 5	R184	A 5
C6	A 6	D30	C 3	R48	B 5	R185	C 3
C7	B 6	D31	A 3	R49	B 5	R186	B 6
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COMP.	LOC.	SHEET
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COMP.	LOC.	SHEET
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COMP.	LOC.	SHEET
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Name		Article nr.
COMP. LOC. SYNC.		76 2489-6
Date	Drawn	Checked
28-04-1995	JVDY	PDG

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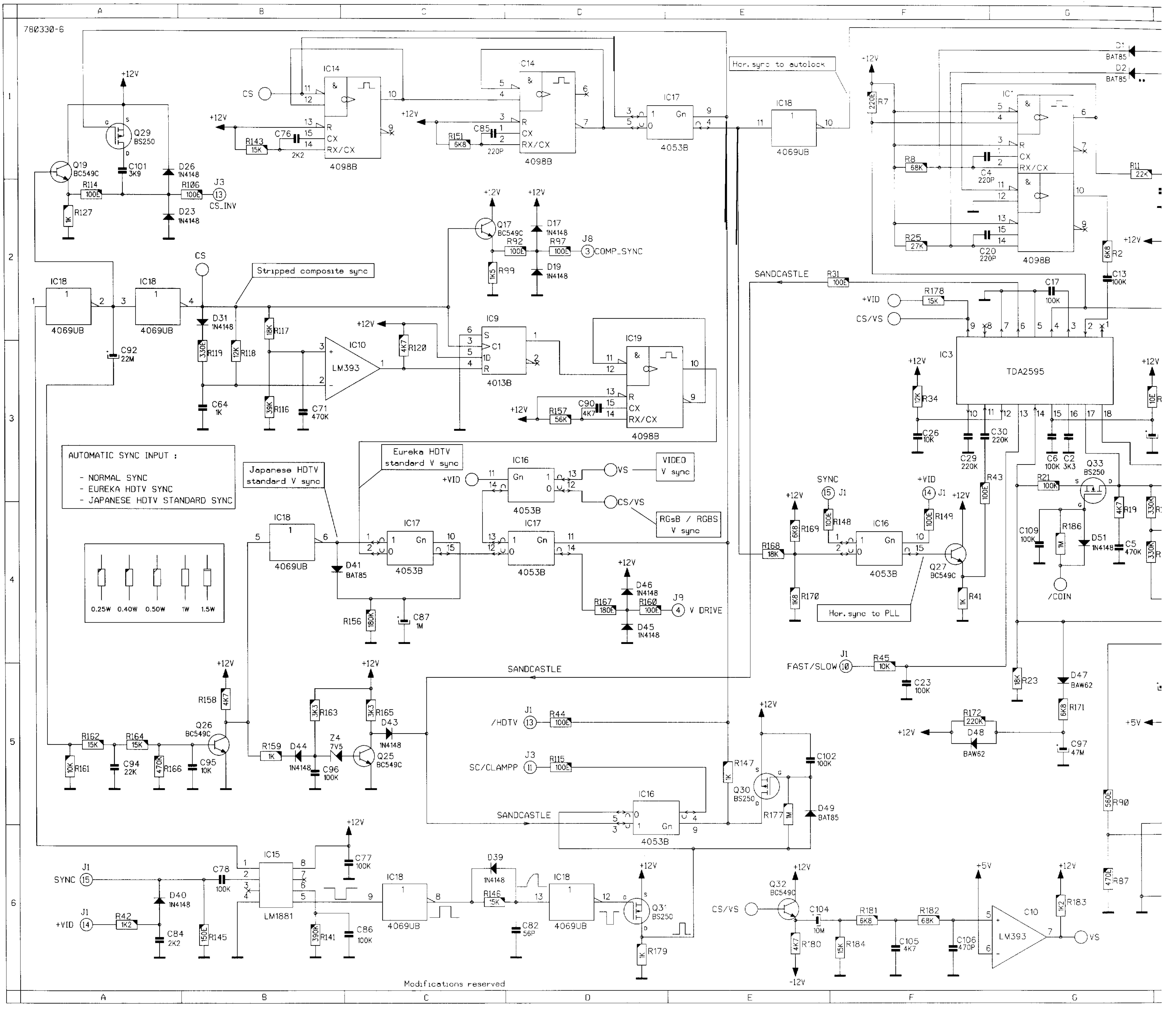
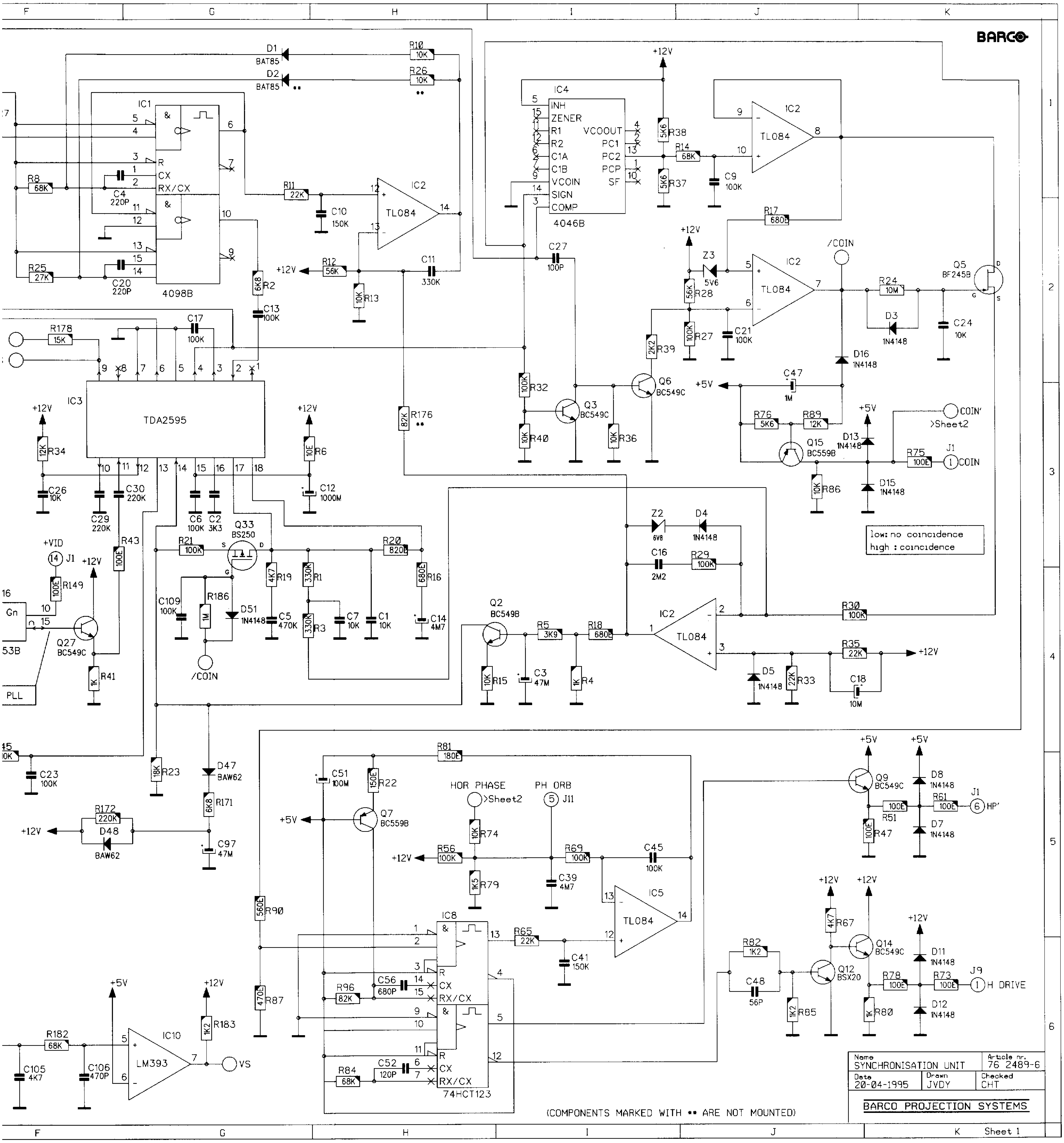
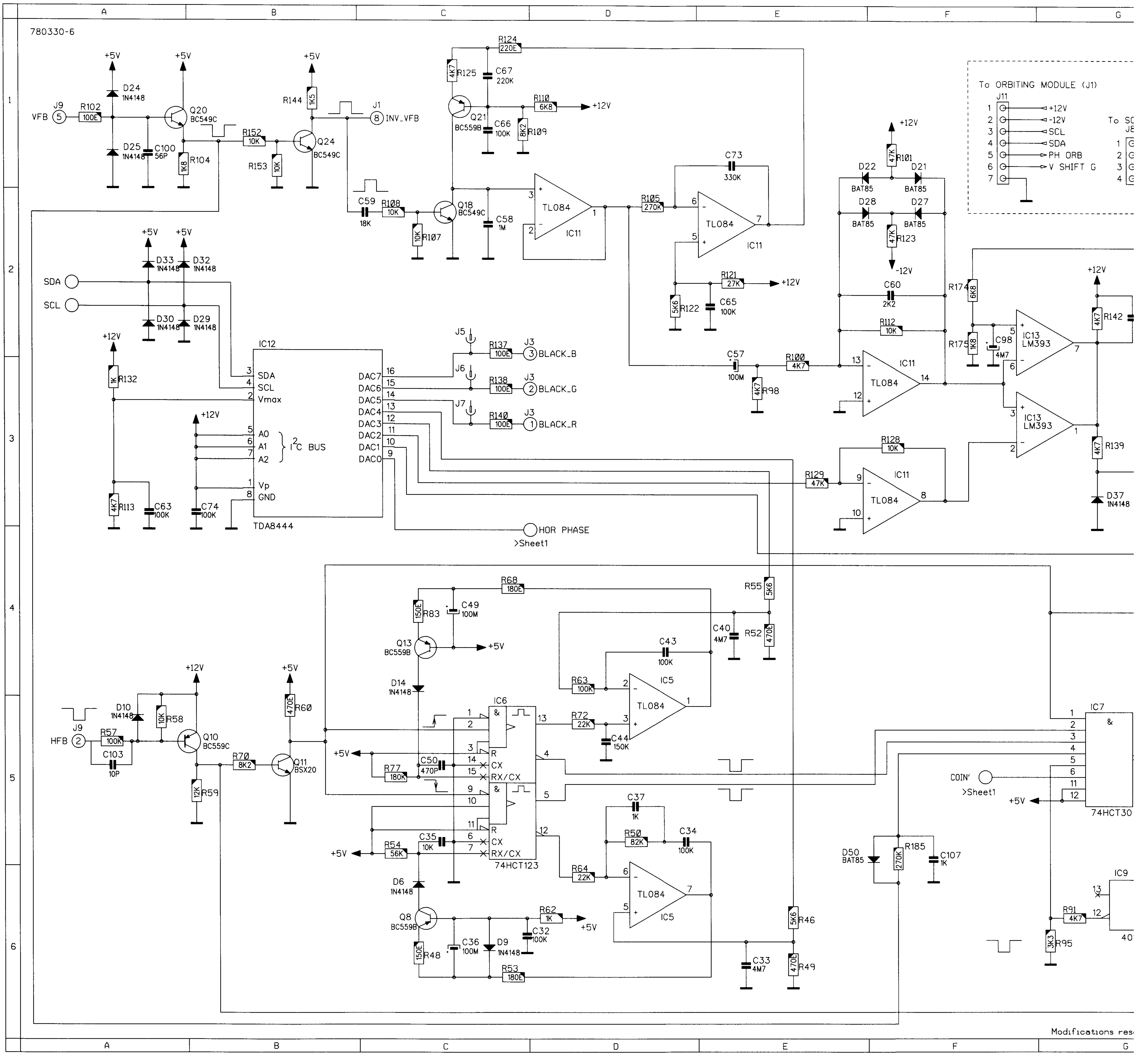
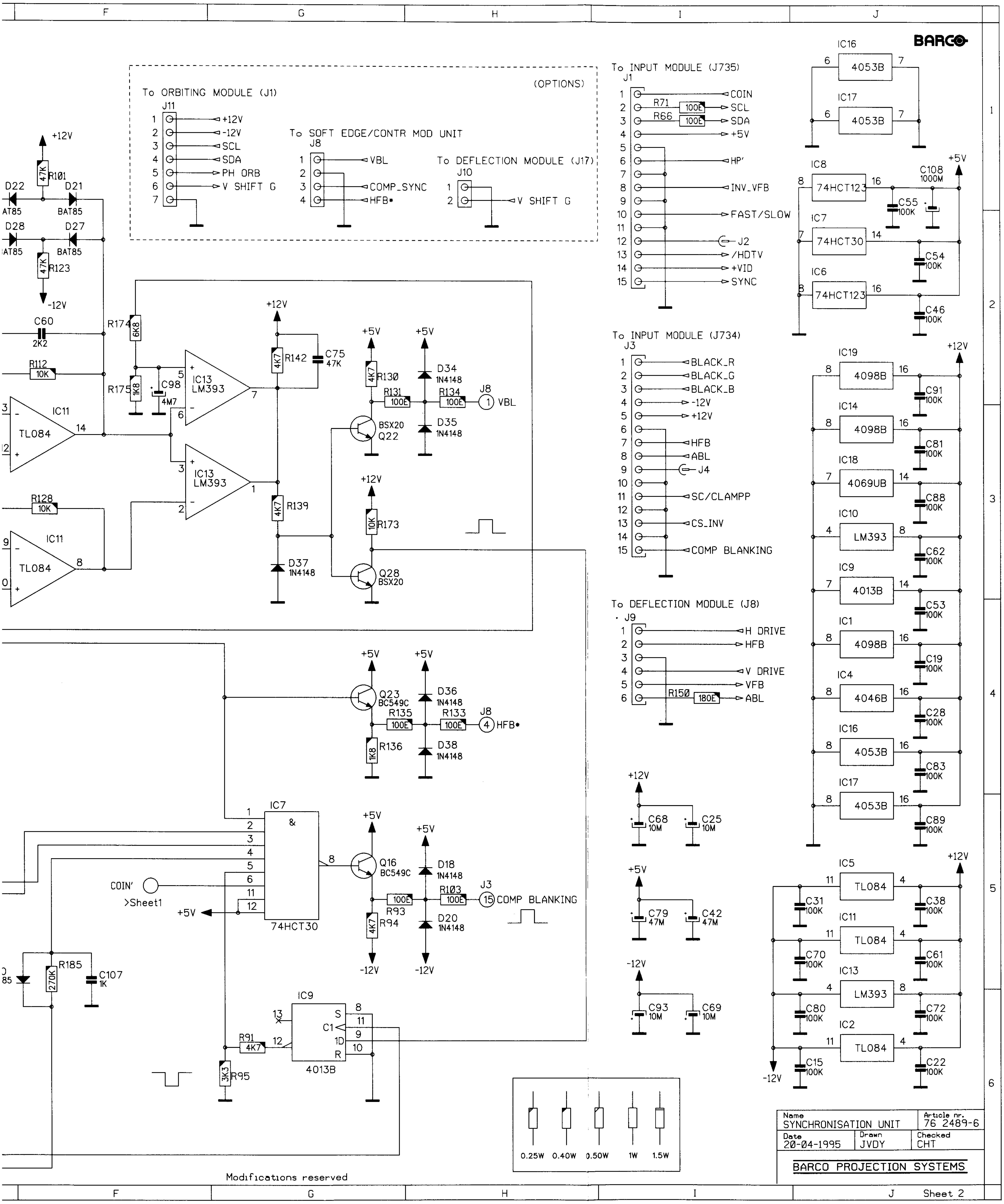
Sheet 1



Modifications reserved


BARCO
low: no coincidence
high : coincidence
(COMPONENTS MARKED WITH •• ARE NOT MOUNTED)
Name
SYNCHRONISATION UNIT
Article nr.
76 2489-6
Date
20-04-1995
Drawn
JVDY
Checked
CHT
BARCO PROJECTION SYSTEMS
Sheet 1


780330-6
VFB
R102 100E
D24 1N4148
D25 1N4148
C100 56P
Q20 BC549C
R104 1K8
R152 10K
R153 10K
R144 1K5
Q24 BC549C
J1 INV_VFB
R124 220E
R125 4K7
C67 220K
Q21 BC559B
R110 6K8
C66 100K
R109 8K2
C59 18K
R108 10K
R107 10K
Q18 BC549C
C58 1M
TL084
IC11
C73 330K
R105 270K
R121 27K
R122 5K6
C65 100K
To ORBITING MODULE (J1)
J11
+12V
-12V
SCL
SDA
PH ORB
V SHIFT G
D22 BAT85
D21 BAT85
D28 BAT85
D27 BAT85
R101 47K
R123 47K
C60 2K2
R112 10K
R174 6K8
R175 1K8
C98 4M7
IC13 LM393
R142 4K7
R139 4K7
D37 1N4148
SDA
SCL
D33 1N4148
D32 1N4148
D30 1N4148
D29 1N4148
R132 1K
R113 4K7
C63 100K
C74 100K
IC12
TDA8444
SDA SCL Vmax A0 A1 A2 Vp GND
I2C BUS
DAC7 DAC6 DAC5 DAC4 DAC3 DAC2 DAC1 DAC0
J5 J6 J7
R137 100E BLACK_B
R138 100E BLACK_G
R140 100E BLACK_R
HOR PHASE >Sheet1
C57 100M
R100 4K7
R98 4K7
R128 10K
R129 47K
R55 5K6
R68 180E
R83 150E
C49 100M
Q13 BC559B
C40 4M7
R52 470E
C43 100K
R63 100K
IC5
D14 1N4148
IC6 74HCT123
R72 22K
C44 150K
R77 180K
C50 470P
R54 56K
C35 10K
HFB
R57 100K
C103 10P
D10 1N4148
R58 10K
Q10 BC559C
R59 12K
R60 470E
R70 8K2
Q11 BSX20
D6 1N4148
Q8 BC559B
C36 100M
D9 1N4148
C32 100K
R62 1K
R48 150E
R53 180E
C37 1K
R50 82K
C34 100K
R64 22K
R46 5K6
C33 4M7
R49 470E
IC7 74HCT30
COIN' >Sheet1
D50 BAT85
R185 270K
C107 1K
IC9
R91 4K7
R95 3K3
Modifications res



F
G
H
I
J
BARCO
To ORBITING MODULE (J1)
(OPTIONS)
J11
+12V
-12V
SCL
SDA
PH ORB
V SHIFT G
To SOFT EDGE/CONTR MOD UNIT
J8
VBL
COMP_SYNC
HFB•
To DEFLECTION MODULE (J17)
J10
V SHIFT G
To INPUT MODULE (J735)
J1
COIN
R71 100E
SCL
R66 100E
SDA
+5V
HP'
INV_VFB
FAST/SLOW
J2
/HDTV
+VID
SYNC
To INPUT MODULE (J734)
J3
BLACK_R
BLACK_G
BLACK_B
-12V
+12V
HFB
ABL
J4
SC/CLAMPP
CS_INV
COMP BLANKING
To DEFLECTION MODULE (J8)
J9
H DRIVE
HFB
V DRIVE
VFB
R150 180E
ABL
IC16 4053B
IC17 4053B
IC8 74HCT123
IC7 74HCT30
IC6 74HCT123
C108 1000M
C55 100K
C54 100K
C46 100K
IC19 4098B
IC14 4098B
IC18 4069UB
IC10 LM393
IC9 4013B
IC1 4098B
IC4 4046B
IC16 4053B
IC17 4053B
C91 100K
C81 100K
C88 100K
C62 100K
C53 100K
C19 100K
C28 100K
C83 100K
C89 100K
IC5 TL084
IC11 TL084
IC13 LM393
IC2 TL084
C31 100K
C38 100K
C70 100K
C61 100K
C80 100K
C72 100K
C15 100K
C22 100K
C68 10M
C25 10M
C79 47M
C42 47M
C93 10M
C69 10M
R101 47K
D22
D21 BAT85
D28
D27 BAT85
R123 47K
C60 2K2
R174 6K8
R112 10K
R175 1K8
C98 4M7
IC13 LM393
IC11 TL084
R128 10K
R142 4K7
C75 47K
R139 4K7
D37 1N4148
R130 4K7
D34 1N4148
R131 100E
R134 100E
J8 VBL
D35 1N4148
BSX20 Q22
R173 10K
Q28 BSX20
Q23 BC549C
D36 1N4148
R135 100E
R133 100E
J8 HFB•
R136 1K8
D38 1N4148
IC7 74HCT30
COIN' >Sheet1
Q16 BC549C
D18 1N4148
R103 100E
J3 COMP BLANKING
R93 100E
R94 4K7
D20 1N4148
R185 270K
C107 1K
IC9 4013B
R91 4K7
R95 3K3
0.25W 0.40W 0.50W 1W 1.5W
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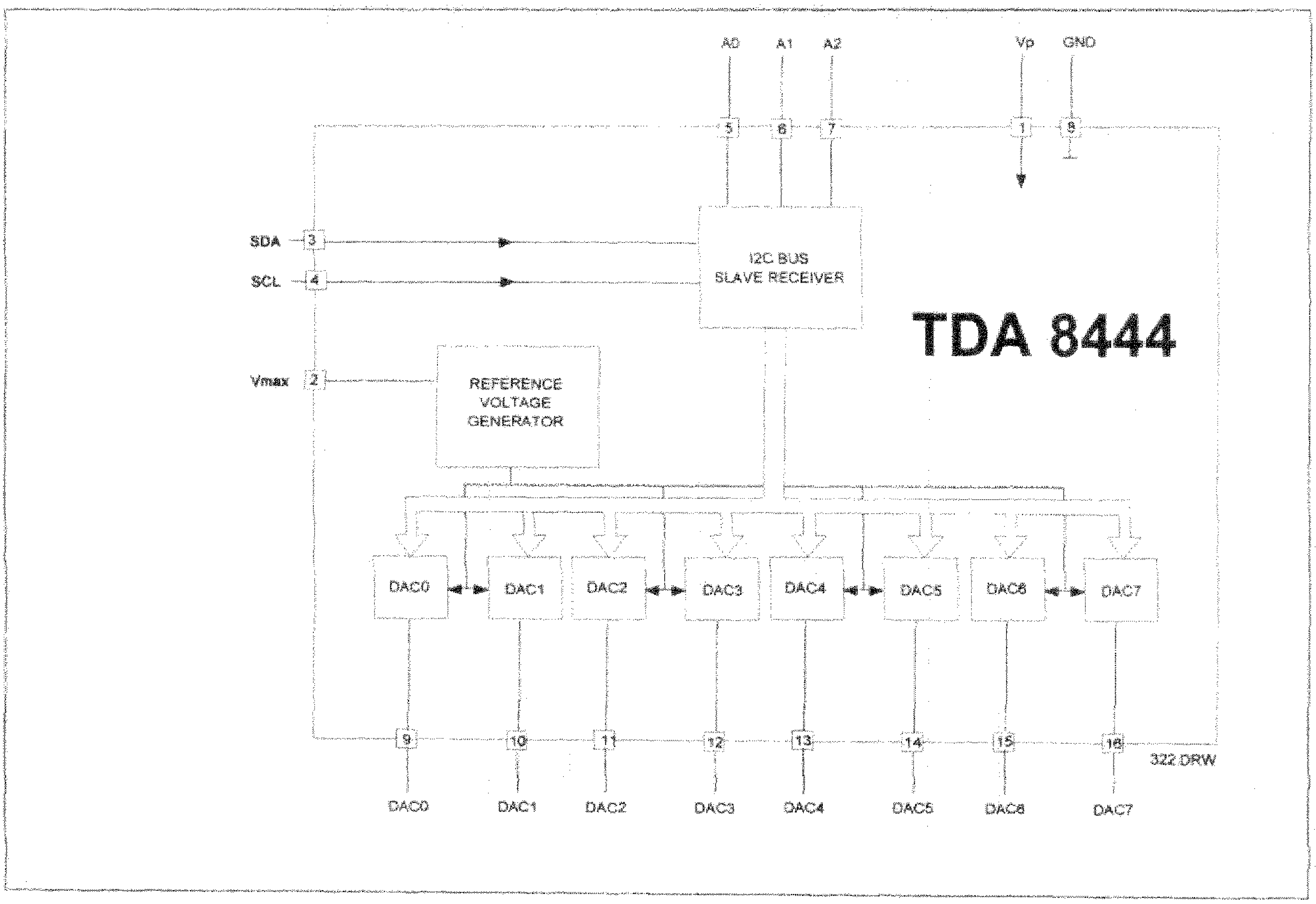
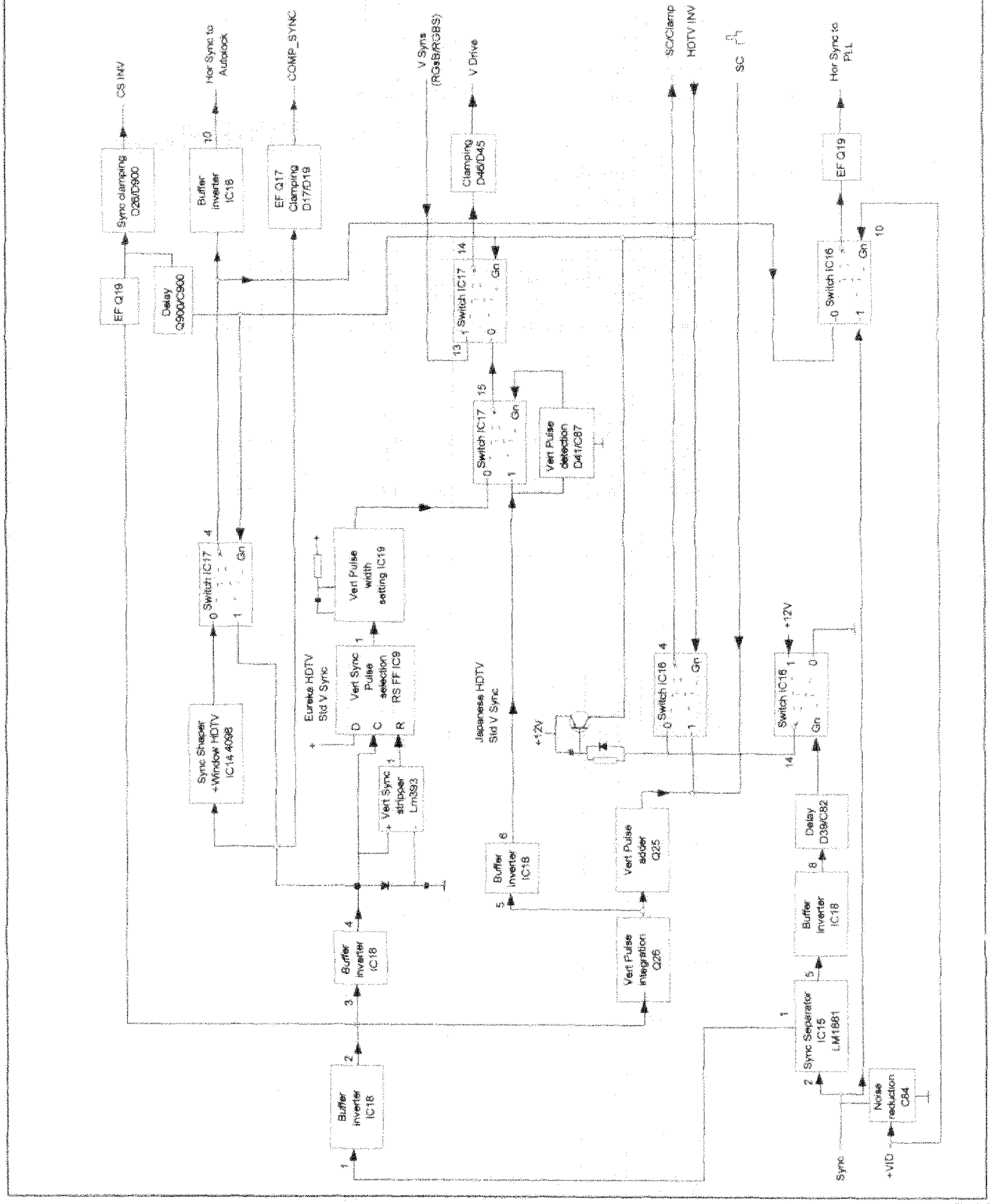
Modifications reserved
Sheet 2

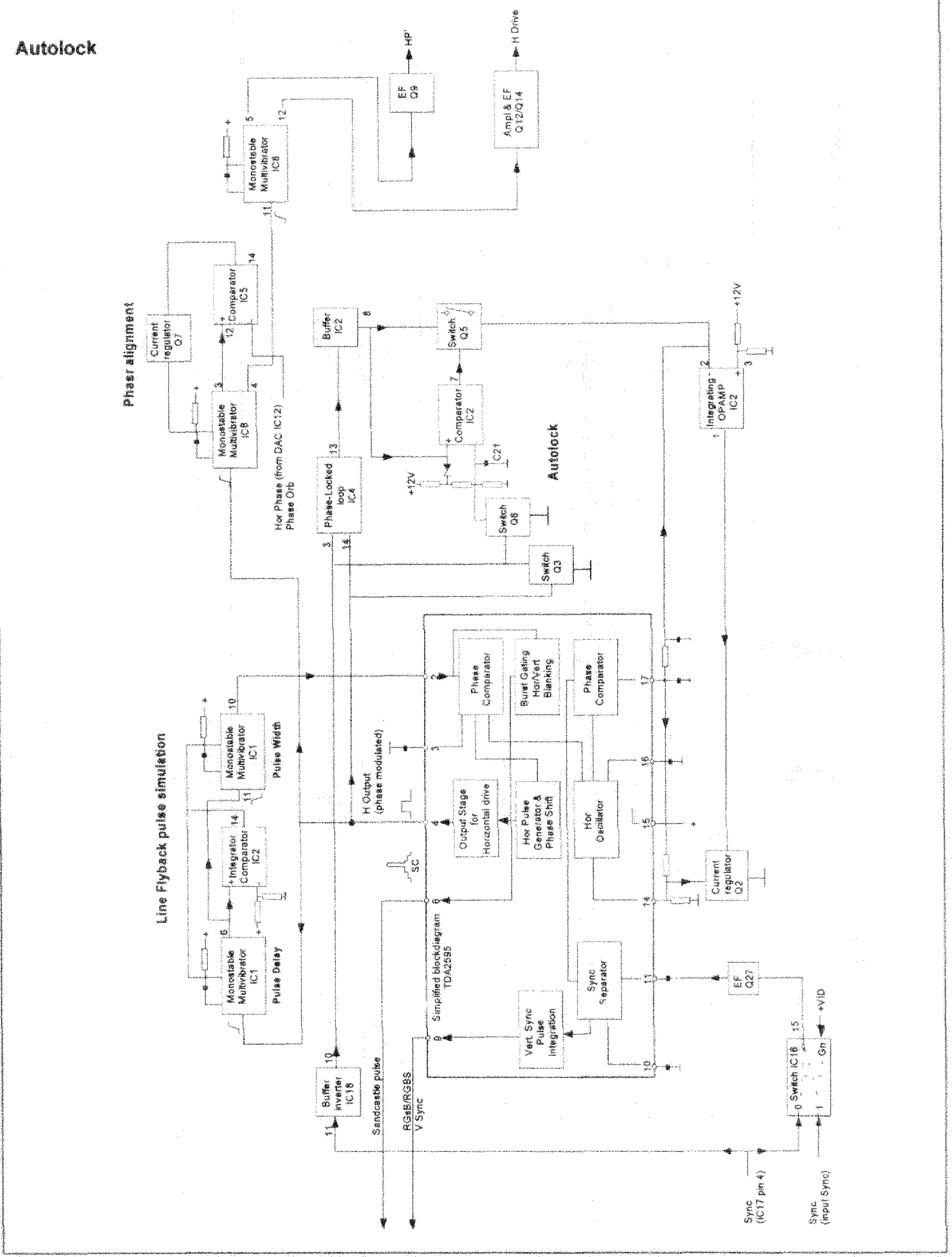

A0
A1
A2
Vp
GND
5
6
7
1
8
SDA
SCL
3
4
I2C BUS
SLAVE RECEIVER
TDA 8444
Vmax
2
REFERENCE
VOLTAGE
GENERATOR
DAC0
DAC1
DAC2
DAC3
DAC4
DAC5
DAC6
DAC7
9
10
11
12
13
14
15
16
322 DRW
DAC0
DAC1
DAC2
DAC3
DAC4
DAC5
DAC6
DAC7

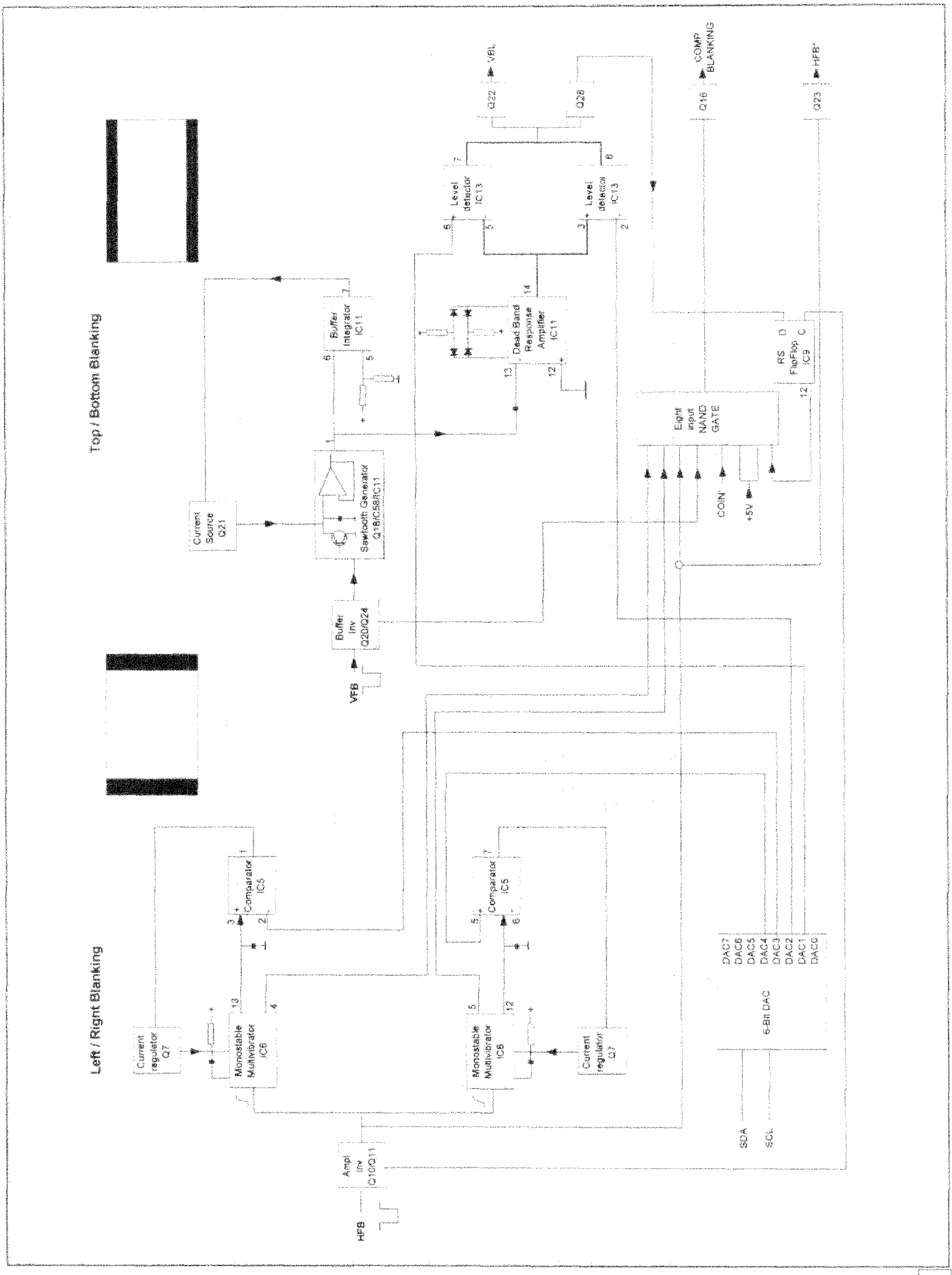
TECHNICAL DESCRIPTION "SYNCHRONISATION "

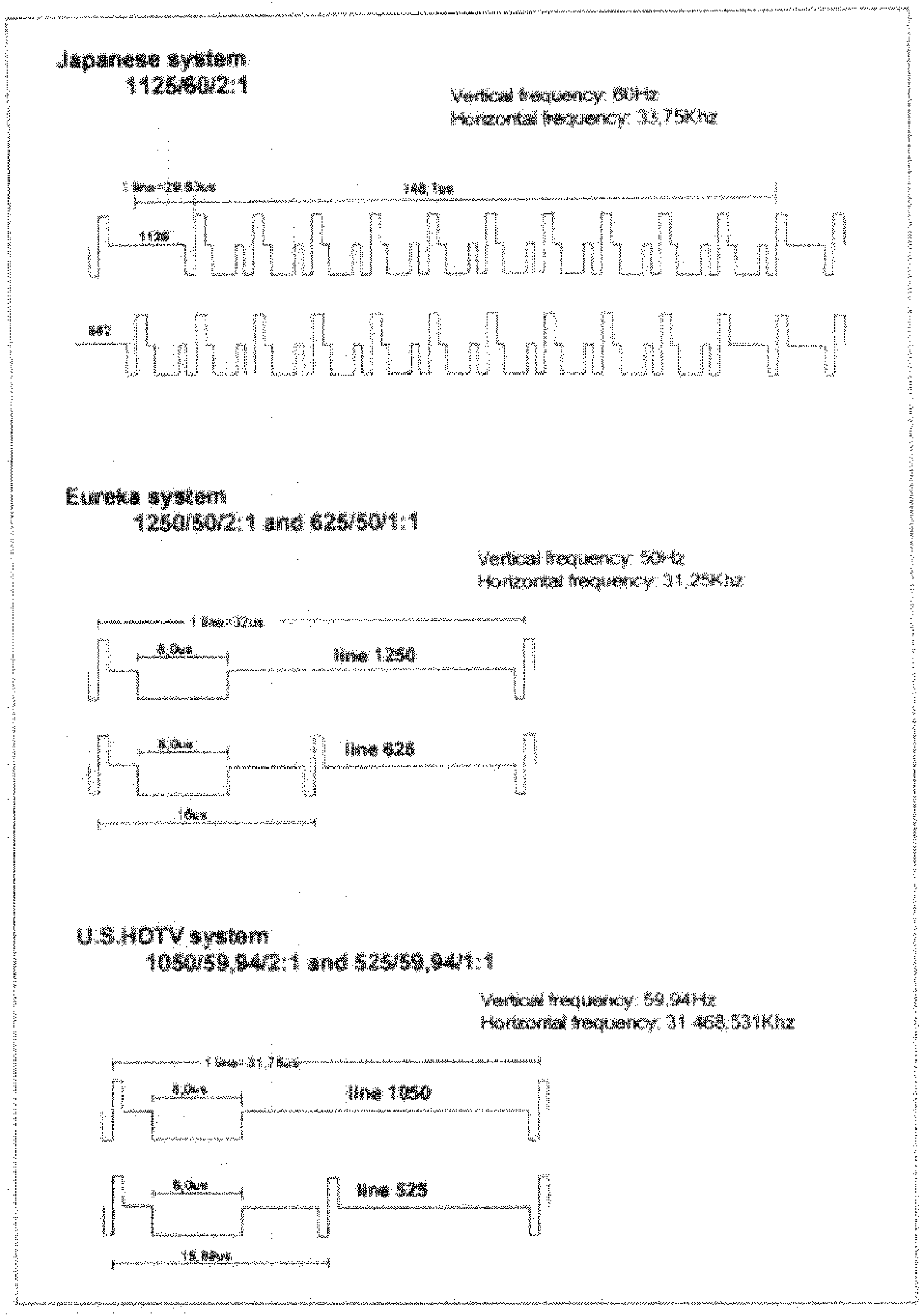
Synchronisation



Autolock


Phase alignment
Current regulator Q7
Comparator IC5
Monostable Multivibrator IC8
Monostable Multivibrator IC6
EF Q9
HP'
H Drive
Ampl & EF Q12/Q14
Hor Phase (from DAC IC12) Phase Orb
Buffer IC2
Switch Q5
Comparator IC2
C21
+12V
Phase-Locked loop IC4
Switch Q6
Switch Q3
Autolock
Integrating OPAMP IC2
Line Flyback pulse simulation
Monostable Multivibrator IC1
Pulse Width
Integrator Comparator IC2
Monostable Multivibrator IC1
Pulse Delay
H Output (phase modulated)
SC
Simplified blockdiagram TDA2595
Phase Comparator
Burst Gating Hor/Vert Blanking
Phase Comparator
Output Stage for Horizontal drive
Hor Pulse Generator & Phase Shift
Hor Oscillator
Current regulator Q2
Sync Separator
Vert. Sync Pulse Integration
EF Q27
Switch IC16
+VID
Buffer inverter IC18
Sandcastle pulse
RGsB/RGBS
V Sync
Sync (IC17 pin 4)
Sync (input Sync)


Top / Bottom Blanking
Left / Right Blanking
VBL
Q22
Q28
COMP BLANKING
Q16
HFB*
Q23
Level detector IC13
Dead Band Response Amplifier IC11
Buffer Integrator IC11
Current Source Q21
Sawtooth Generator Q18/C58/IC11
Buffer Inv Q20/Q24
VFB
Eight input NAND GATE
RS FlipFlop IC9
COIN
+5V
Comparator IC5
Monostable Multivibrator IC6
Current regulator Q7
6-Bit DAC
DAC7
DAC6
DAC5
DAC4
DAC3
DAC2
DAC1
DAC0
SDA
SCL
Ampl Inv Q10/Q11
HFB



The LM1881, sync stripper, separates the sync from the composite video which is applied to the input pin 2. In case of Video or SVHS a noise integrating capacitor C84 is added in parallel, by means of the forward biased diode D40.

Burst output, pin 5, is buffered in IC18 and feeds after been delayed the select input of the Multiplexer in IC16 (pin 11). The latter is used to force the SC pulse on SC/CLAMP out when no Sync signal is presence. The Composite Sync output, pin 1, buffered in IC18 and led out (pin 2) as composite sync "CS_INV" via EF Q19.

The flow of the Composite Sync depends on the selected mode: HDTV or not.

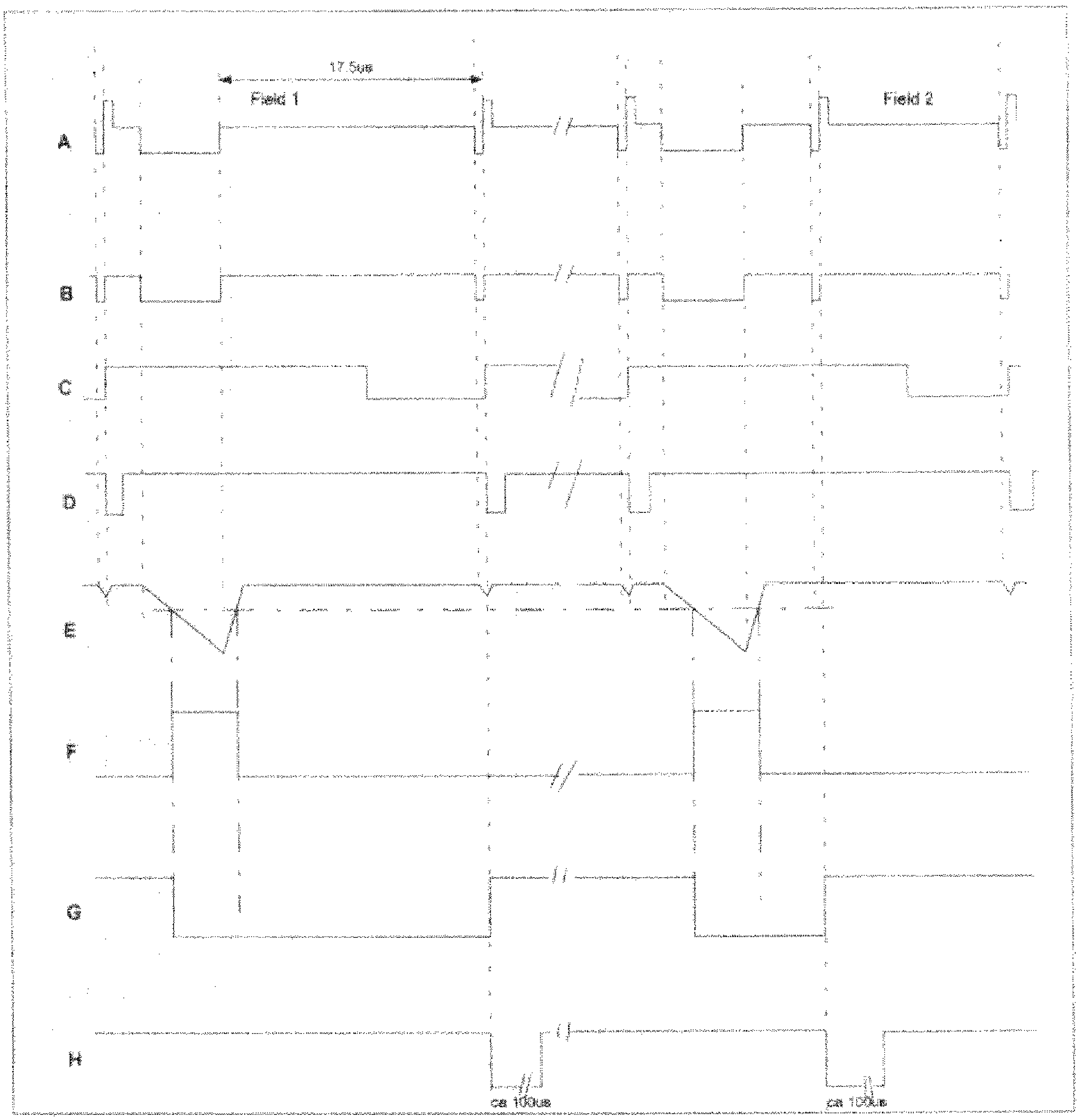
a) two-level sync (no HDTV) :

In this case, the ' HDTV INV' selection voltage is High, and the input pin 3 is selected by the multiplexer in IC17. The output pin 4 is split to the TDA2595 and to the PLL IC3. The TDA2595 produces the "H OSC"signal.

The vertical pulses at pin 9 of the TDA2595 are selected by another multiplexer in IC17, pin 13, and leave pin 14 as "V drive" to the vertical oscillator on the "deflection board" (76 2201).

b) Tri-level sync or HDTV:

In this case, the 'HDTV INV ' selection voltage is low. The signal available at pin 5 (Hor sync) and pin 12 (Vert sync) of the multiplexer in IC17 are selected.



1. Horizontal Sync:

The original sync pulses are represented in fig. as A. The sync separator output is represented in fig. as B, and we see that the positive part of the tri-level sync is cut by the sync separator.
The purpose of the tri-level sync is to trigger at any time the line oscillator at the 'sync trigger' time (trailing edge of the tri-level pulse).
As can be seen in signal A, in the first line of the second field there is an additional pulse halfway the line period (interlacing).
This pulse may be skipped as to get sync pulses with constant time periods. This is performed by means of two monoflops in IC14 as follows:

At each sync trigger (positive transition of the horizontal sync) the first monoflop IC14 is triggered. The output pulse at pin 10 of the latter comes high for a time smaller than a line period, but longer than half a line period (signal C).

At the start of the second field, the tri-level pulse (halfway the line) cannot trigger the monoflop as its output is still at high level. The resulting pulse train is presented as signal C in the diagram.

These pulses now trigger on the positive transitions the second monoflop in IC14. The monoflop delivers horizontal pulses with a fixed time and the leading edge is always in coincidence with the 'sync trigger' (signal D).

2. Vertical sync:

Detection Japanese HDTV system or Eureka/US HDTV system.

The integrated CS_INV pulses at the collector of the transistor Q26 are inverted by IC18 , out pin 6. These pulses are rectified by the diode D41/C87/R156. For the Japanese system, a DC voltage is built up across the capacitor C87. This voltage , applied at pin 10 of the multiplexer IC17, selects the integrated pulses at input 1 of the multiplexer. The integrated pulses are passed through the second multiplexer in IC17 (selected by /HDTV) and used as "V drive".

Note: the integrated pulses at the collector of Q26 are, with Q25, added to the SC pulses. This is needed for the decoder.

For the other systems, they are passing the RS FF (IC9) and the monoflop IC19 before being selected by the multiplexer.

Sync processing for Eureka/US HDTV system

Here again, the purpose of the tri-level sync is to determine undoubtedly that the vertical oscillator is triggered at the 'sync trigger' time.

As can be seen on signal A, the first field must start 17.5us after the trailing edge of the vertical pulse. Whereas the start of the second field is determined by the 'additional horizontal pulse' halfway the line period.

We need vertical pulses, starting at the mentioned 'sync trigger' time and the duration of which should be approximately 100us. This will be realized with the aid of a RS flip-flop IC9 and a monoflop in IC19.

The vertical pulses at the output pin4 of the inverter IC18 are first integrated with D31/R118/C64 (see signal E). The threshold of the level detector IC10 is set with R117/R116. The output pulses (signal F) are applied to the Reset input of the RS flipflop IC9. The clock of this flipflop is the combined sync.

The start of the vertical pulses resets the output to low level. The first positive transition of the clock input is the 'sync trigger' which sets the output high as the D-input is pulled up to the +12 Volts. The output remains high until the next vertical pulse appears (signal G).

This signal G is now triggering the trigger input of IC19, pin 12. The latter triggers on the positive transition; thus in coincidence with the 'sync trigger'. The time constant of this monoflop is providing pulses with a duration of approx. 100us.

The sync signal H is passed through the multiplexers in IC17 and used as "V drive"

Horizontal oscillator + Autolock.

The horizontal pulses from multiplexer IC17, out pin 4, serve the PLL in IC 3 TDA2595 via the multiplexers in IC16 in non Video mode, and the inverted pulses, IC18 out pin 10, serve the autolock circuit IC4. In the Video mode, +VID pin 10 IC16, the Sync pulses at pin 1 of IC16 serve the PLL in IC3

The oscillator in the TDA2595 is locked to the centre frequency by its own PLL system, but the latter has rather a limited range of approx. 1 khz. Therefore, it serves as a fine lock for the frequency. An additional PLL, IC4, is used to coarse lock the frequency first.

The 4046B consists of two digitally controlled phase comparators. For this application only the second one is used. The signal input, pin 14, is the line oscillator **"HOSC"** of the TDA2595, and the **COMP** input is the comp. sync. The corresponding output is **PC2**, pin 13, a three-level state output.

If the output is open, the voltage is set at 6 volts with R38/37. This voltage can be increased or decreased by the push-pull output of the IC. The voltage is buffered and reaches a voltage comparator, pin 5 and 6 of IC2. The output of the latter switches on or off the Fet Q5 which transfers the regulating voltage to the TDA2595. when shorted.

The gate voltage of Q5 is buffered with Q15 and then, out as ' COIN' .Low level output means no coincidence whereas Highlevel the opposite..

Coincidence detector

The HOSC (square wave with the line period) switches on and off the transistor Q3. When switched on, any pulse arriving at the base of Q6 is clamped at ground and cannot switch on the latter. When the frequency or phase of the line oscillator is different from the composite sync, these pulses arrive on the base of Q6 at the moment Q3 is off. These pulse switch on and off Q6 and discharge C21 decreasing the voltage at pin 6. The voltage at the other input cannot drop lower than 6 volts due to the zenerdiode Z3. Consequently, the output pin 7 switches "high" to forward biases Q5. The latter connects the buffer-output with the integrating OPAMP.

Locking of the oscillator

The regulating voltage at pin 1 of IC2 drives Q2. The efficiency of the circuit is thus automatically adapted to the line frequency. The current drawn by Q2 determines the frequency of the line oscillator of the TDA2595.
The line oscillator is corrected until it is locked to the comp. sync frequency. The PLL output is now switched off and the coincidence circuit turns off the fet Q5.
From this point on, the fine frequency lock in the TDA2595 takes over and adjusts the line oscillator until the exact frequency and phase is reached.
As the coarse tuning voltage is lost now, the PLL output pin 17 of the TDA2595, feeds now pin 2 of the integrating OPAMP IC2 to establish and maintain the fine tuning loop.
In the locked state, this PLL output is 6 volts. As pin 3 of the OPAMP is set at 6 volts with R35/R33, the action of the OPAMP continues up to the moment the oscillator is locked to the centre of the hold range of the PLL.

Line flyback pulse simulation.

The phase of the HOSC square wave output, pin 4 of the TDA2595, is determined by the position of the pulse applied at pin 2.
The width of this pulse also is the width of the SC (Sandcastle) which exits at pin 6.
This pulse is generated by means of two one shots in IC1. The first one introduces a delay between the end of the scan (=positive transition of the square wave) and the simulated pulse. The second monoflop sets the width of the pulse.

The trailing edge (negative transition) of the named pulse triggers now the next one shot.

Phase alignment

The HOSC square wave (pin 4 TDA2595) is not suitable for driving the MOSFETs in the horizontal deflection. Two one shots will derive a drive pulse with the correct width and an adjustable delay (=phase) with respect to the (reference) input sync signal.
The adjustment range over the entire frequency range must be proportional with the line period.
The range in *absolute* value must be much lower for the higher frequencies than for the lower frequencies. The *relative* value (percentage) must be the same. This

is obtained by tracking the phase range with the line frequency by means of an automatic system (feedback) as described hereafter.

The "phase control" voltage from the 6-Bit DAC IC12, out pin 9 'HOR PHASE', is sent to the comparator IC5, pin 13. The other input, pin 12, receives the integrated pulses of pin 13 IC8. This DC voltage is depending on the line period (line frequency) and the width of the pulses.
Assume we have set the phase voltage at 2 volts. The comparator will now adjusts the width of the output pulses at pin 13 IC8 until both inputs of IC5, pin 13 and 12, carry the same 2 volts. Therefore, the width of the pulses will be narrower when the line period decreases, thus for the higher frequencies. Note that the width of this pulse here is the phase delay, or phase alignment.
Indeed, the other one shot now is triggered with the negative pulse of pin4 on the positive transition.
The width of the horizontal drive pulse is set by C52/R84.

Adjustable blankings.

The positive drive pulses at pin 5 are sent to the controller via Q9 and board connector J1 (pin 6) to lock the PLL of the textgenerator. The negative going pulses at pin 12 are slightly amplified and buffered with Q5 and Q6 and sent to the Horizontal deflection circuit via board connector J9 (pin 1).

a) Left / right blanking .

The left/right Blanking pulses are generated by means of two one-shots in IC6, triggered with HFB (Horizontal FlyBack pulses).
The available range of the 6-Bit DAC's of IC12 is 0 -9 volts (Vmax pin 2=9 Volts). This range should allow the same relative blanking irrelevant the line period. Therefore, the absolute value must be smaller at higher frequencies.
A feedback system is used that automatically adapts the width of the pulse to the line period (compare this with the phase alignment where a similar problem is solved in a similar way).

Pulses, coinciding with the start of the flyback time, and, having a width set by C50/ Q13, exit at pin 13 of IC6. These pulses are integrated and the resulting voltage is sent to pin 3 of IC5 to be compared with the voltage at pin 2 (=left bl, from 6-Bit DAC IC12 pin12). The OPAMP's output, pin1, is fed back to the input pin 2 with a Miller capacitor. The current of Q13 is adapted until both voltages at the pins 2 and 3 are identical. The pulses **"inv L"** are applied to the NAND-gate input 3 of IC7.

To generate the blanking pulse for the end of the scan, the inverted output at pin 12 of the second one-shot in IC6 is integrated and compared with the DAC voltage 'right bl' from IC12. The pulses **"inv R"** are applied to the NAND-gate input 2 of IC7.

Top / Bottom blanking
To achieve a high accuracy, or, in other words, to dispose of a steep ramp, the sawtooth is sent into a "dead band response amplifier" built around the OPAMP 12-13-14 in IC11.

A sawtooth generator with stable amplitude is generated by means of a feedback system as described hereafter.
The capacitor C58 is charged through the current source around Q21 and discharged through Q18 at the moment a **"INV_VFB"** pulse is sent to its base. The sawtooth is buffered and integrated by the next OPAMP due to the feedback capacitor C73. The integrated voltage regulates the base-emitter current of the current source Q21 and

consequently adapts the charging current to stabilise the amplitude irrelevant the vertical frequency.
Note that the amplitude is set by the voltage at pin 5 by the divider R121/R122.

The sawtooth from IC11, pin1, enters pin 13 capacitively. The output is inverted and the clipping levels are set by clamping circuits : R101/D21/D22 and R123/D28/D27. The resulting waveform is now sent to two level detectors in IC13, on the inverting and the non inverting inputs. The respective outputs of the DAC IC12, pin 11 'bottom bl' and pin 10 'top bl', adjust the DC levels of the other inputs.

The combined output pulses '**VBL**' on the collector of the transistor Q28 are applied to the "Data" input of an RS-flipflop of IC9. The pulse is clocked to the output with flyback pulses HFB to guarantee a full line blanking for interlaced pictures.

The output pin 12 is added to the NAND-gate IC7 just like the left/right blanking. Blanking during the vertical retrace time is accomplished by applying a vertical pulse '**VFB**' at pin 4 of the NAND-gate.

Parts listing 76 2226

SIT.	ITEM NO.	DESCRIPTION	QUANTITY
C 1	R114068	C POMERA 10N M 63E2 85	1
C 2	R113819	C POMERA 3N3J250E2 85	1
C 3	R111465	C EL RA 47M M 16E2 85	1
C 4	R112366	C N750MI 220P G100E2	1
C 5	R114087	C POMERA 470N K 63E2 85	1
C 6	R113724	C POMERA 100N K 63E2 85	
C 7	R112763	C CE MI 10N U 63E2	1
C 9	R113724	C POMERA 100N K 63E2 85	
C 10	R113726	C POMERA 150N K 63E2 85	
C 11	R113730	C POMERA 330N K 63E2 85	
C 12	R111469	C EL RA1000M M 16E2 85	1
C 13	R113724	C POMERA 100N K 63E2 85	1
C 14	R1115915	C EL5 RA 4M7M 35E2 85	1
C 15	R113724	C POMERA 100N K 63E2 85	
C 16	V114098	C POMERA 2M2M 50E2 85	1
C 17	R113724	C POMERA 100N K 63E2 85	
C 18	R111531	C EL RA 10M M 35E2 85	
C 19	R113724	C POMERA 100N K 63E2 85	
C 20	R112366	C N750MI 220P G100E2	
C 21	R113724	C POMERA 100N K 63E2 85	
C 22	R113724	C POMERA 100N K 63E2 85	
C 23	R113724	C POMERA 100N K 63E2 85	1
C 24	R112763	C CE MI 10N U 63E2	
C 25	R111531	C EL RA 10M M 35E2 85	
C 26	R112763	C CE MI 10N U 63E2	1
C 27	R112242	C NP0 MI 100P G100E2	
C 28	R113724	C POMERA 100N K 63E2 85	
C 29	R113728	C POMERA 220N K 63E2 85	
C 30	R113728	C POMERA 220N K 63E2 85	
C 31	R113724	C POMERA 100N K 63E2 85	
C 32	R113724	C POMERA 100N K 63E2 85	
C 33	R111550	C EL RA 4M7M 50E2 85	
C 34	R113724	C POMERA 100N K 63E2 85	
C 35	R114068	C POMERA 10N M 63E2 85	1
C 36	R111466	C EL RA 100M Z 16E2 85	
C 37	R112739	C CE MI 1N K100E2	1
C 38	R113724	C POMERA 100N K 63E2 85	
C 39	R111550	C EL RA 4M7M 50E2 85	
C 40	R111550	C EL RA 4M7M 50E2 85	
C 41	R113726	C POMERA 150N K 63E2 85	1
C 42	R111500	C EL RA 47M M 10E2 85	
C 43	R113724	C POMERA 100N K 63E2 85	
C 44	R113726	C POMERA 150N K 63E2 85	1
C 45	R113724	C POMERA 100N K 63E2 85	
C 46	R113724	C POMERA 100N K 63E2 85	1
C 47	R111546	C EL RA 1M M 50E2 85	1
C 47	R111550	C EL RA 4M7M 50E2 85	1
C 48	R1122395	C NP0 MI 56P G100E2	1
C 49	R111466	C EL RA 100M Z 16E2 85	
C 50	R1159081	C PP RA 470P J100E2 85	
C 51	R111477	C EL RA 100M Z 25E2 85	
C 52	R112243	C NP0 MI 120P G100E2	1
C 53	R113724	C POMERA 100N K 63E2 85	
C 54	R113724	C POMERA 100N K 63E2 85	1
C 55	R113724	C POMERA 100N K 63E2 85	1
C 56	R112737	C CE MI 680P K100E2	1
C 57	R111477	C EL RA 100M Z 25E2 85	
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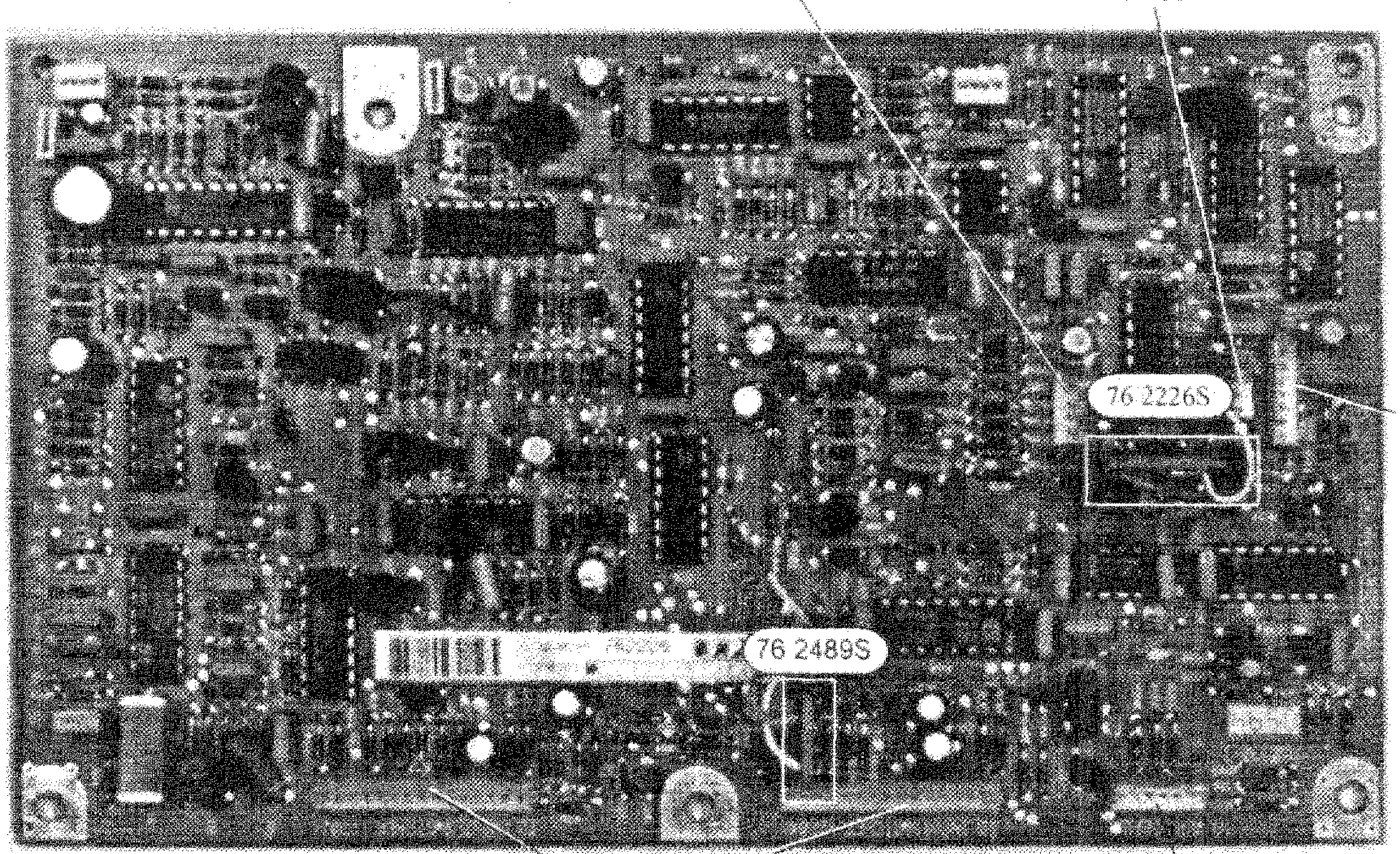

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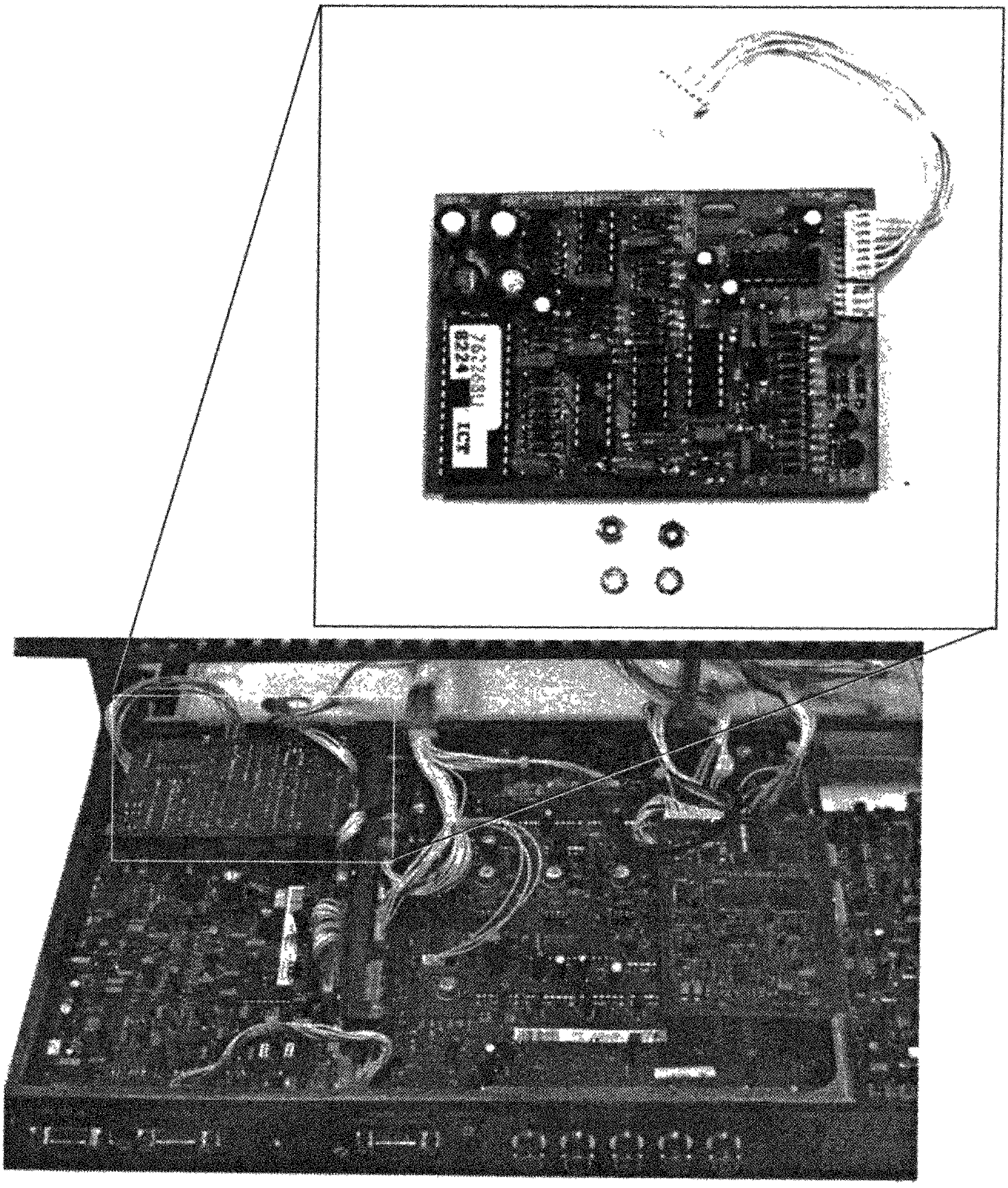
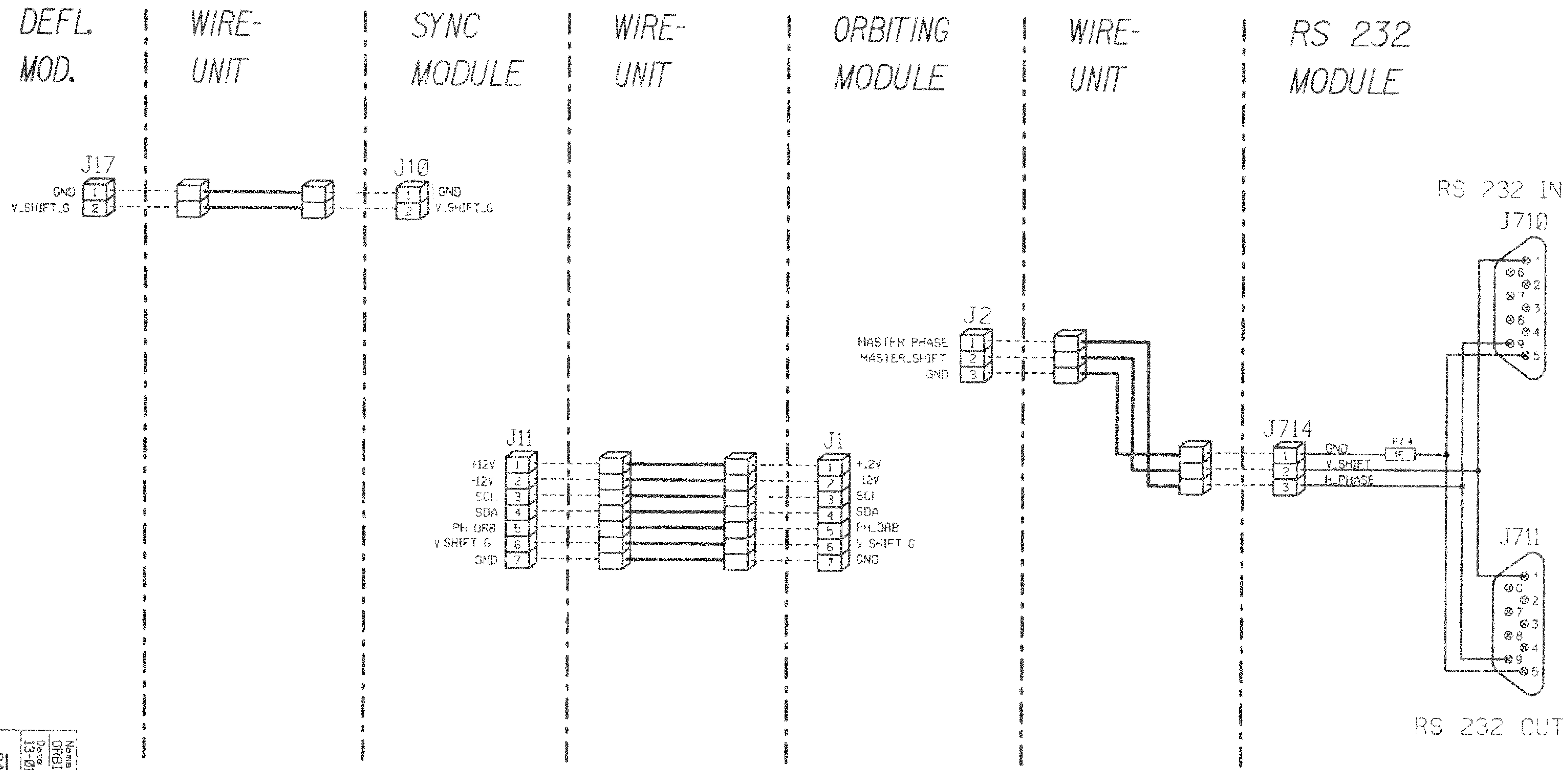
ORBITING KIT R762268U



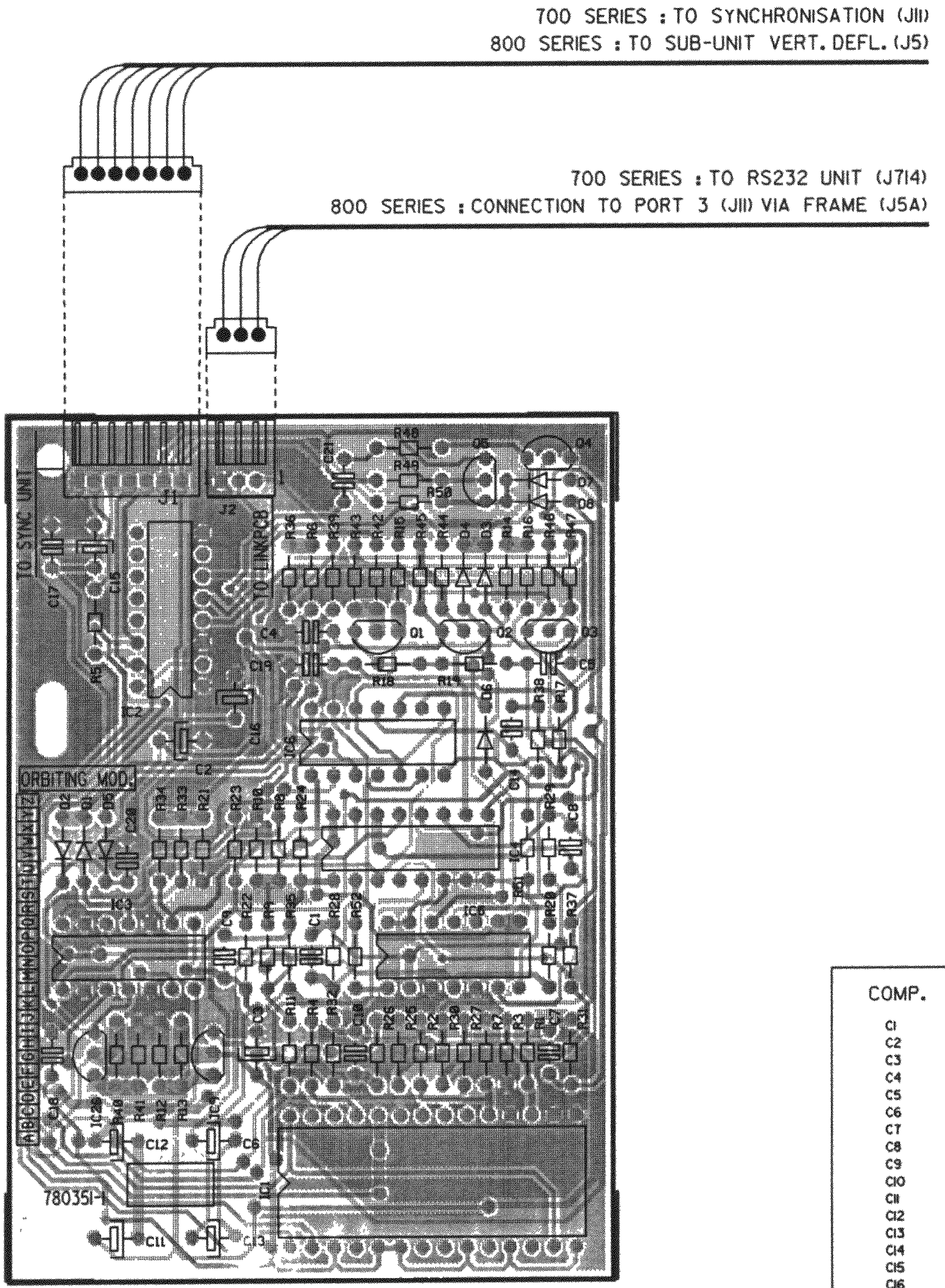


ORBITING LINK

BARCO

Name ORBITING LINK		Article nr. 700 series
Date 13-01-1995	Drawn JVDY	Checked CHT
BARCO PROJECTION SYSTEMS		
		Sheet 1

BARCO



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C7	C 4	R7	C 4
C8	C 3	R8	B 3
C9	B 4	R9	B 4
C10	B 4	R10	B 3
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D4	B 3	R26	B 4
D5	A 3	R27	B 4
D6	B 3	R28	B 4
D7	C 2	R29	C 3
D8	C 3	R30	B 4
		R31	C 4
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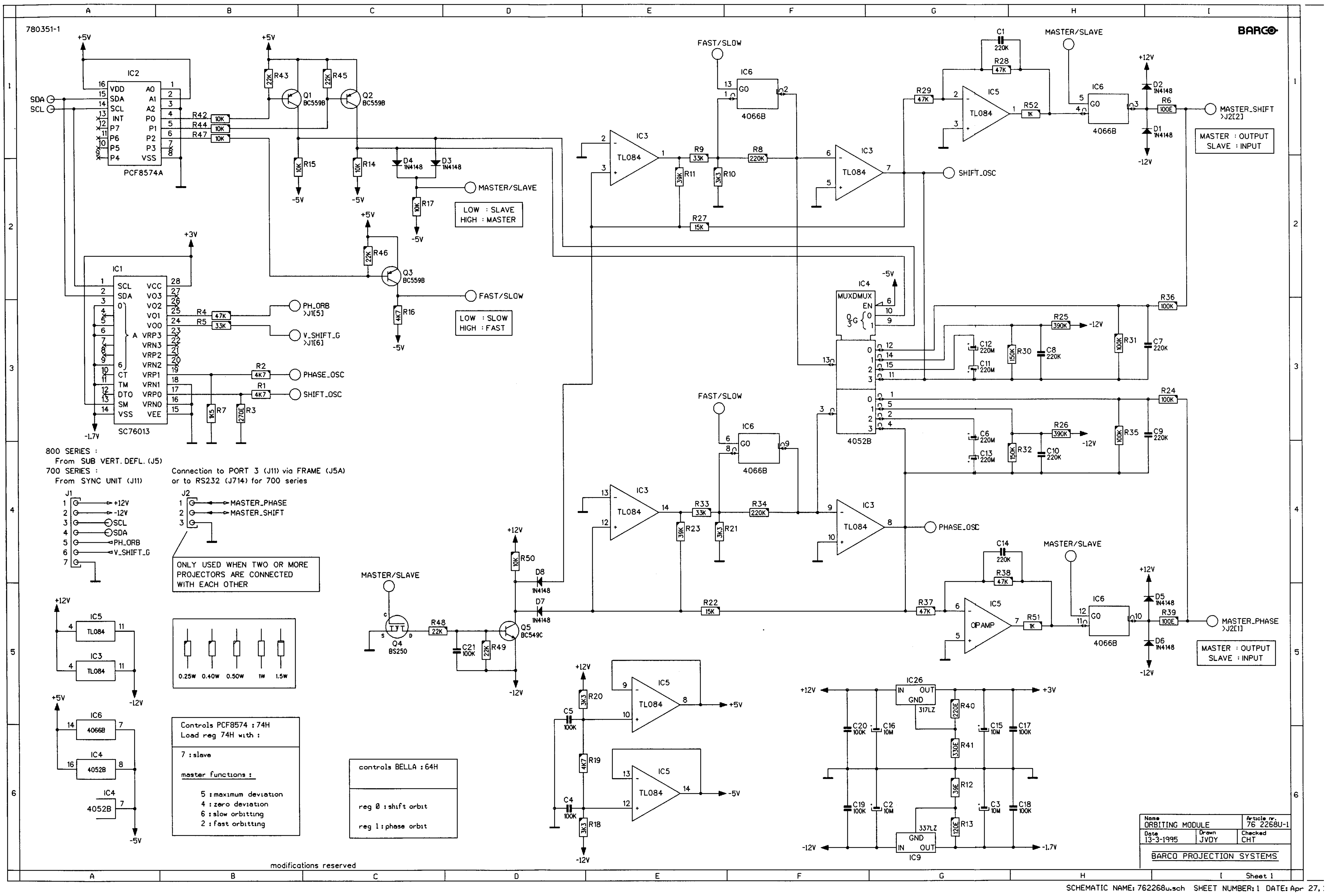
IC2	B 3	R33	B 3
IC3	A 4	R34	B 3
IC4	C 3	R35	B 4
IC5	B 4	R36	B 3
IC6	B 3	R37	C 4
IC9	B 4	R38	C 3
IC26	A 4	R39	B 3
		R40	B 4
J1	B 3	R41	B 4
J2	B 3	R42	B 3
		R43	B 3
Q1	B 3	R44	B 3
Q2	C 3	R45	B 3
Q3	C 3	R46	C 3
Q4	C 2	R47	C 3
Q5	B 2	R48	B 2
		R49	B 2
		R50	B 3
		R51	C 4
		R52	B 4

Name		Article nr.
ORBITING MODULE		76 2268U-1
Date 26-04-1995	Drawn JVDY	Checked CHT

BARCO PROJECTION SYSTEMS

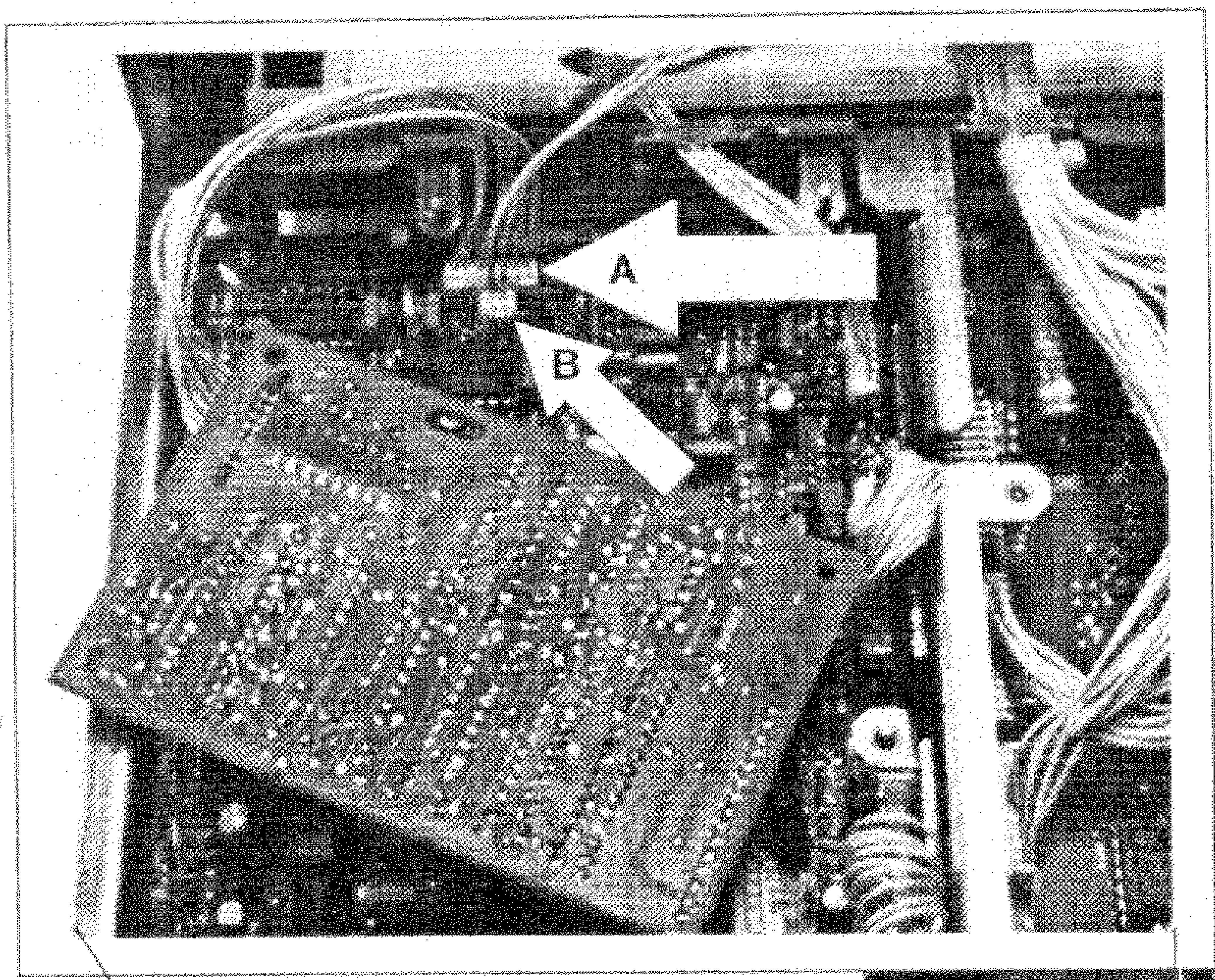
Modifications reserved

COMP.	LOC.
C1	G 1
C2	G 6
C3	G 6
C4	D 6
C5	D 5
C6	G 3
C7	I 3
C8	H 3
C9	I 3
C10	H 4
C11	G 3
C12	G 3
C13	G 4
C14	G 4
C15	G 5
C16	G 5
C17	H 5
C18	H 6
C19	F 6
C20	F 5
C21	D 5
D1	I 1
D2	I 1
D3	D 1
D4	C 1
D5	I 5
D6	I 5
D7	D 5
D8	D 4
IC1	A 2
IC2	A 1
IC3	E 1
IC3	E 4
IC3	A 5
IC3	F 1
IC3	F 4
IC4	A 6
IC4	A 6
IC4	F 2
IC5	E 5
IC5	E 6
IC5	A 5
IC5	G 1
IC5	G 5
IC6	F 3
IC6	A 5
IC6	H 1
IC6	F 1
IC6	H 5
IC9	G 6
IC26	G 5
J1	A 4
J2	B 4
Q1	C 1
Q2	C 1
Q3	C 2
Q4	C 5
Q5	D 5
R1	B 3
R2	B 3
R3	B 3
R4	B 3
R5	B 3
R6	I 1
R7	B 3
R8	F 1
R9	E 1
R10	F 2
R11	E 2
R12	G 6
R13	G 6
R14	C 2
R15	C 2
R16	C 3
R17	C 2
R18	E 6
R19	E 6
R20	E 5
R21	F 4
R22	E 5
R23	E 4
R24	I 3
R25	H 3
R26	H 3
R27	E 2
R28	G 1
R29	G 1
R30	H 3
R31	H 3
R32	H 4
R33	E 4
R34	F 4
R35	H 3
R36	I 2
R37	G 5
R38	G 4
R39	I 5
R40	G 5
R41	G 6
R42	B 1
R43	B 1
R44	B 1
R45	C 1
R46	C 2
R47	B 1
R48	C 5
R49	D 5
R50	D 4
R51	H 5
R52	H 1



SCHEMATIC NAME: 762268u.sch SHEET NUMBER: 1 DATE: Apr 27,

Electrical connection

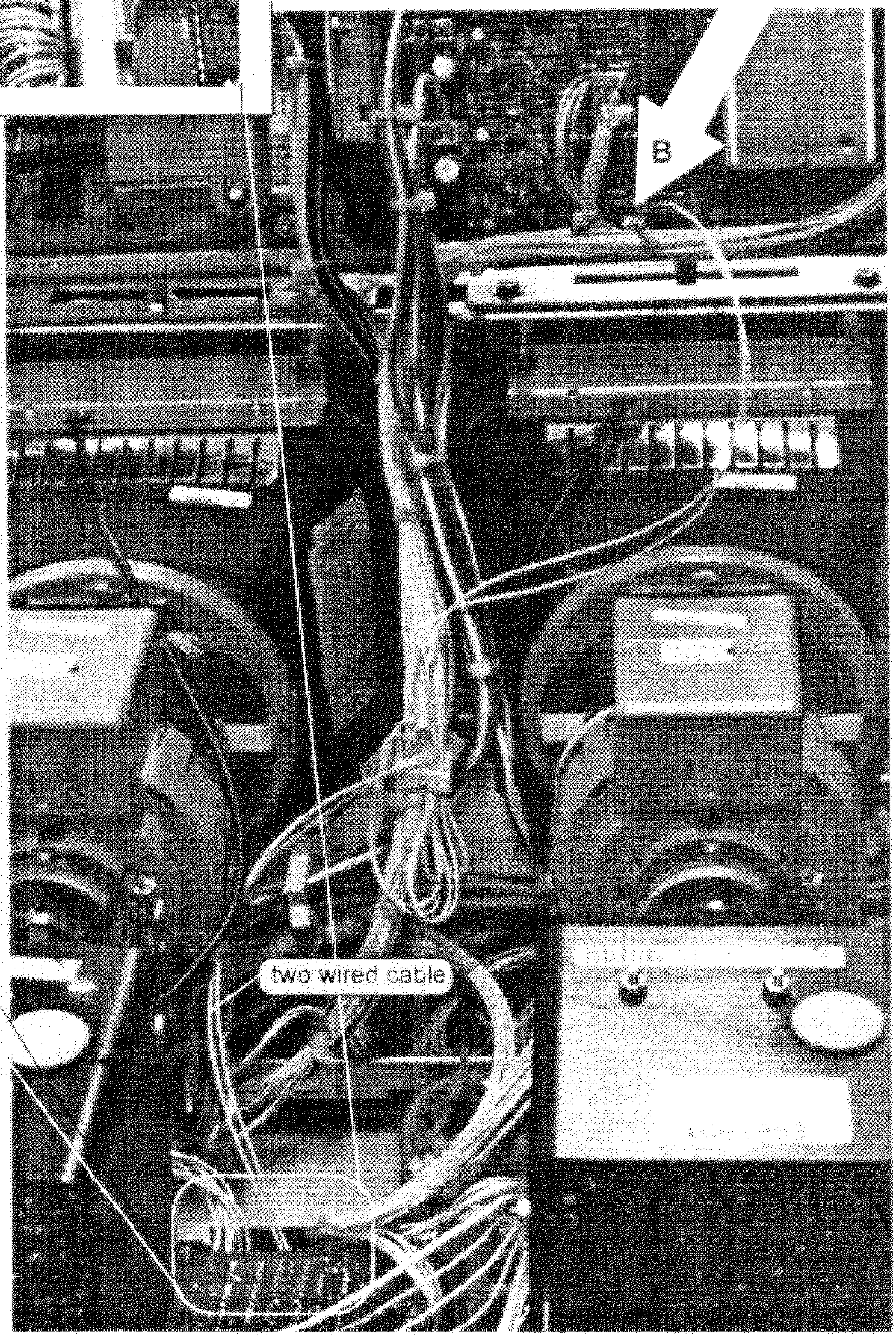


Module connection

Connect the ORBITING module to the Synchronisation module by plugging in the ORBITING plug (A) into the ORBITING connector (J11) on the Synchro module

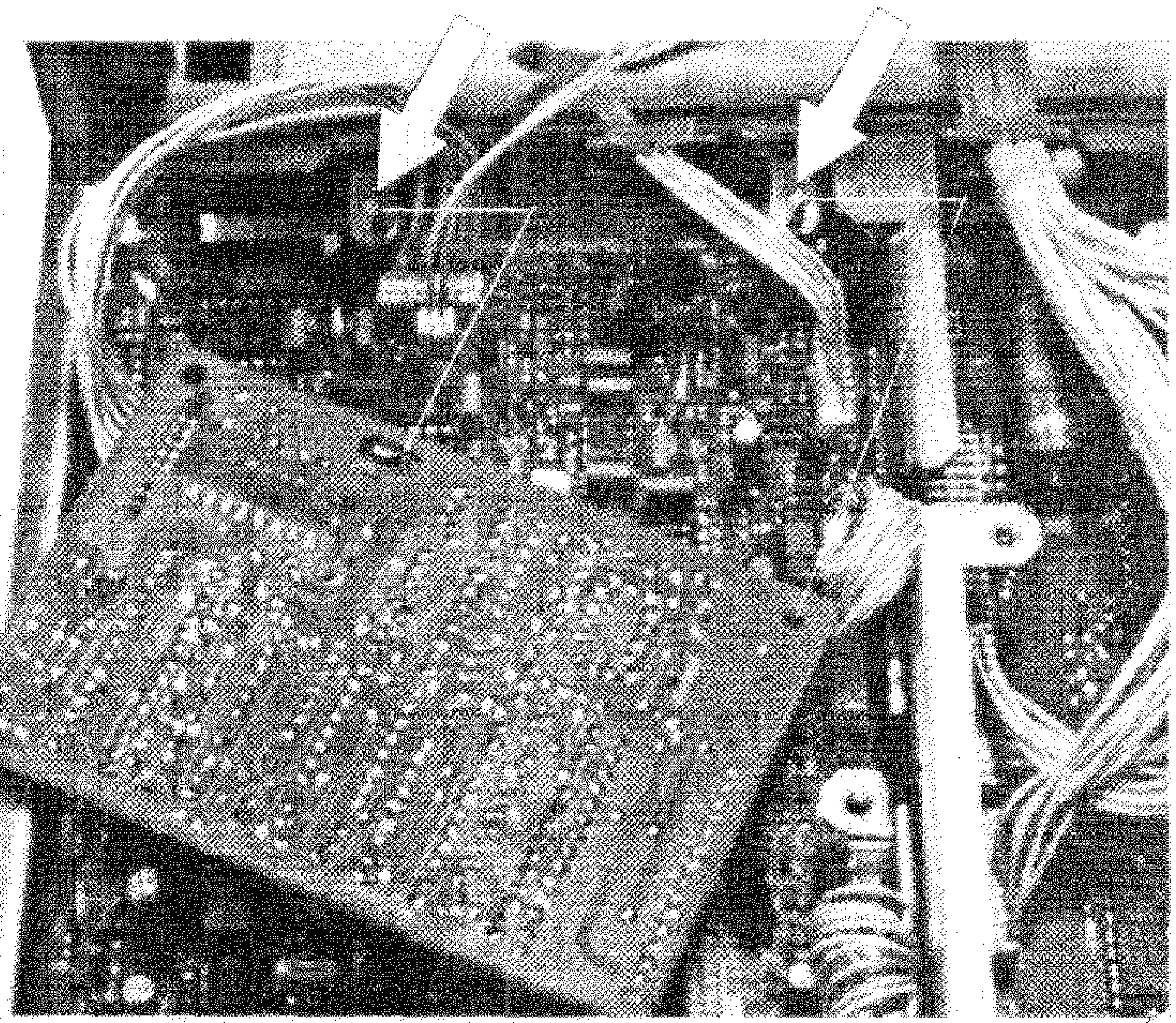
Interconnection Syncho/Deflection module

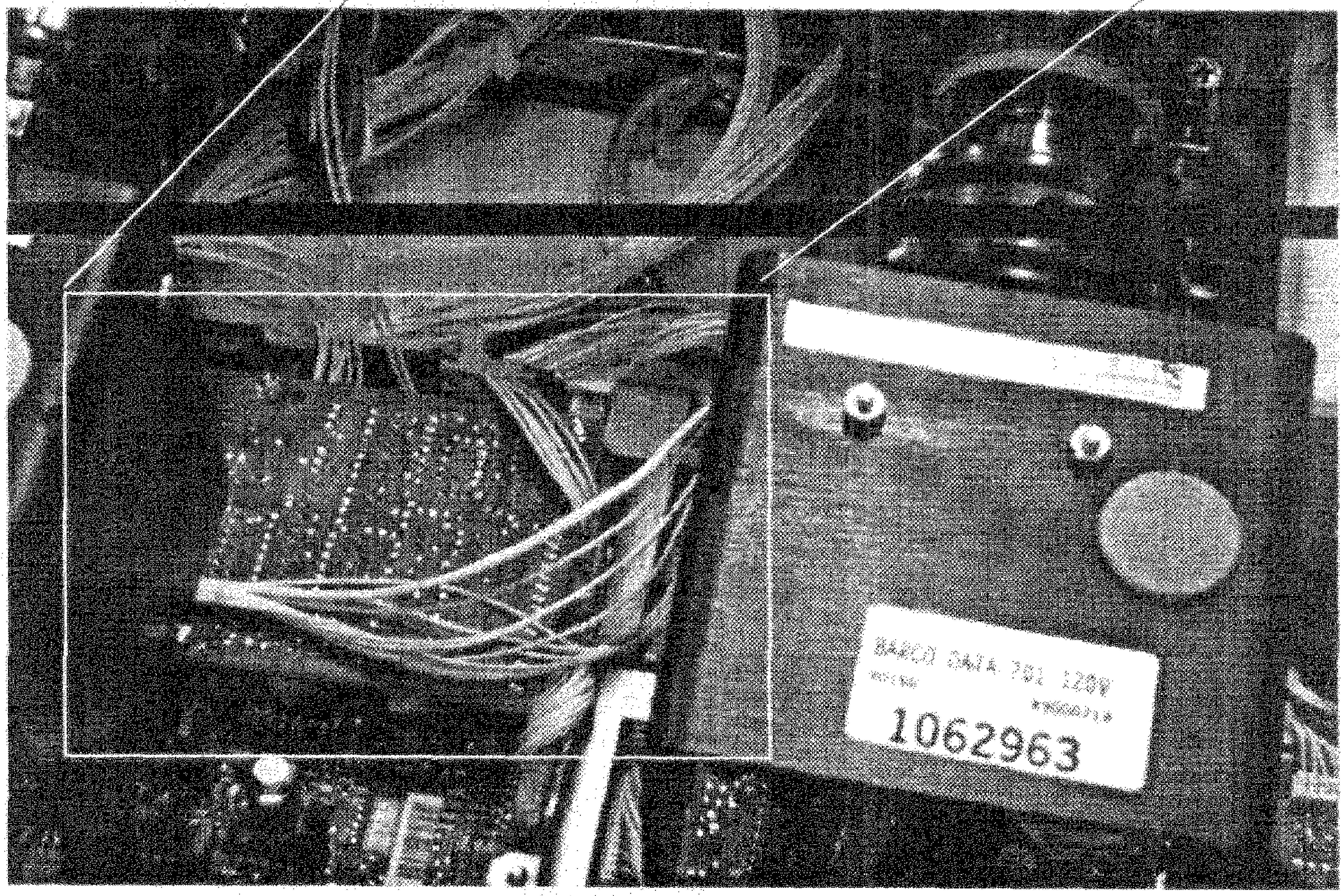
Install the connection between the Synchro and the Deflection module by means of the two wired cable with plugs (B) (refer to illustration)



Mechanical mounting

Place the ORBITING module on the mechanical frame lining up the two holes in the module with the threaded pins on the frame. Fix the module to the frame by inserting and tightening the two provided nuts with washer.





Parts listing ORBITING module R762268U

SIT.	ITEM NO.	DESCRIPTION	QUANTITY
	R34840710	CD CT FTFT P 7 120	1
	R3485037	CD CT $FTFT P 3 200	1
1010	R3631049	SCR D933 M 3 X 6 XIC	4
1000	R803299	SPR L37 H 5.5 M 3 B	2
C 1	R113728	C POMERA 220N K 63E2 85	1
C 2	R111531	C EL RA 10M M 35E2 85	
C 3	R111531	C EL RA 10M M 35E2 85	
C 4	R113724	C POMERA 100N K 63E2 85	
C 5	R113724	C POMERA 100N K 63E2 85	
C 6	R111478	C EL RA 220M M 25E2 85	1
C 7	R113728	C POMERA 220N K 63E2 85	1
C 8	R113728	C POMERA 220N K 63E2 85	1
C 9	R113728	C POMERA 220N K 63E2 85	1
C 10	R113728	C POMERA 220N K 63E2 85	1
C 11	R111478	C EL RA 220M M 25E2 85	1
C 12	R111478	C EL RA 220M M 25E2 85	1
C 13	R111478	C EL RA 220M M 25E2 85	1
C 14	R113728	C POMERA 220N K 63E2 85	
C 15	R111531	C EL RA 10M M 35E2 85	
C 16	R111531	C EL RA 10M M 35E2 85	
C 17	R113724	C POMERA 100N K 63E2 85	
C 18	R113724	C POMERA 100N K 63E2 85	
C 19	R113724	C POMERA 100N K 63E2 85	
C 20	R113724	C POMERA 100N K 63E2 85	
C 21	R113724	C POMERA 100N K 63E2 85	
D 1	R131621	D S 1N4148 075150 DO35	
D 2	R131621	D S 1N4148 075150 DO35	
D 3	R131621	D S 1N4148 075150 DO35	
D 4	R131621	D S 1N4148 075150 DO35	
D 5	R131621	D S 1N4148 075150 DO35	
D 6	R131621	D S 1N4148 075150 DO35	
D 7	R131621	D S 1N4148 075150 DO35	
D 8	R131621	D S 1N4148 075150 DO35	
I 1	R132833	U 76013 SC DIP28 P	1
I 2	R132832	U 8574A PCF DIP16 P	1
I 3	R134113	U 084 TL DIP14 P	1
I 4	R137600	U 4052B DIP16 P	1
I 5	R134113	U 084 TL DIP14 P	1
I 6	R137303	U 4066B DIP14 P	1
I 9	R134029	U 337LZ TO92 P	1
I 26	R134028	U 317LZ LM TO92 P	1
J 1	R313947	J CT H MBS P 7 M2SN	1
J 2	R313943	J CT H MBS P 3 M2SN	1
PC	R780351	PCD PJ49 800 ORBIT 2	1
Q 1	R1314181	Q BC559B P SS TO92	
Q 2	R1314181	Q BC559B P SS TO92	
Q 3	R1314181	Q BC559B P SS TO92	
Q 4	R132916	Q BS250 FN SS TO92	1
Q 5	R131411	Q BC549C N SS TO92	
R 1	R101544	R MF H 4K7 F 0W4 E3	
R 2	R101544	R MF H 4K7 F 0W4 E3	
R 3	R101529	R MF H270E F 0W4 E3	
R 4	R101556	R MF H 47K F 0W4 E3	
R 5	R101554	R MF H 33K F 0W4 E3	
R 6	R101524	R MF H100E F 0W4 E3	
R 7	R101538	R MF H 1K5 F 0W4 E3	
R 8	R101563	R MF H180K F 0W4 E3	
R 9	R101554	R MF H 33K F 0W4 E3	
R 10	R101542	R MF H 3K3 F 0W4 E3	
R 11	R101555	R MF H 39K F 0W4 E3	
R 12	R101519	R MF H 39E F 0W4 E3	
R 13	R101525	R MF H120E F 0W4 E3	
R 14	R101548	R MF H 10K F 0W4 E3	
R 15	R101548	R MF H 10K F 0W4 E3	
R 16	R101544	R MF H 4K7 F 0W4 E3	
R 17	R101548	R MF H 10K F 0W4 E3	
R 18	R101542	R MF H 3K3 F 0W4 E3	
R 19	R101544	R MF H 4K7 F 0W4 E3	
R 20	R101542	R MF H 3K3 F 0W4 E3	
R 21	R101542	R MF H 3K3 F 0W4 E3	
R 22	R101550	R MF H 15K F 0W4 E3	
R 23	R101555	R MF H 39K F 0W4 E3	
R 24	R101560	R MF H100K F 0W4 E3	
R 25	R101567	R MF H390K F 0W4 E3	
R 26	R101567	R MF H390K F 0W4 E3	
R 27	R101550	R MF H 15K F 0W4 E3	
R 28	R101556	R MF H 47K F 0W4 E3	
R 29	R101556	R MF H 47K F 0W4 E3	
R 30	R101562	R MF H150K F 0W4 E3	
R 31	R101560	R MF H100K F 0W4 E3	
R 32	R101562	R MF H150K F 0W4 E3	
R 33	R101554	R MF H 33K F 0W4 E3	
R 34	R101564	R MF H220K F 0W4 E3	
R 35	R101560	R MF H100K F 0W4 E3	
R 36	R101560	R MF H100K F 0W4 E3	
R 37	R101556	R MF H 47K F 0W4 E3	
R 38	R101556	R MF H 47K F 0W4 E3	
R 39	R101524	R MF H100E F 0W4 E3	
R 40	R101528	R MF H220E F 0W4 E3	
R 41	R101530	R MF H330E F 0W4 E3	
R 42	R101548	R MF H 10K F 0W4 E3	
R 43	R101552	R MF H 22K F 0W4 E3	
R 44	R101548	R MF H 10K F 0W4 E3	
R 45	R101552	R MF H 22K F 0W4 E3	
R 46	R101552	R MF H 22K F 0W4 E3	
R 47	R101548	R MF H 10K F 0W4 E3	
R 48	R101552	R MF H 22K F 0W4 E3	
R 49	R101552	R MF H 22K F 0W4 E3	
R 50	R101548	R MF H 10K F 0W4 E3	
R 51	R101536	R MF H 1K F 0W4 E3	
R 52	R101536	R MF H 1K F 0W4 E3	