SECTION 9

CONVERGENCE MODULE

SUB-SECTIONS

ILLUSTRATIONS

TABLE

SECTION 9

CONVERGENCE MODULE

9.1 TECHNICAL DESCRIPTION

9.1.1 General Description

The Convergence module corrects and compensates errors in registration between the red, green and blue CRT images. The module uses digital-to-analog converters to continuously generate correction values which are memory-mapped to the CRT raster.

The Convergence module contains the following circuitry:

a) horizontal phase locked loop (HPLL)
b) vertical phase-locked loop (VPLL)
c) alpha generation
d) RAM bank switching
e) band switch
d) address generation and multiplexing
f) waveform channel

9.1.2 Circuit Description

9.1.2.1 Horizontal Phase Locked Loop

The HPLL is a closed, single loop, control system. It locks itself onto the Horizontal Flyback Pulse (HFB) over the range of 15KHz to 80KHz, then synthesises a high frequency clock (HPLLCLK) that is slightly more than 256 times the HFB frequency.

The HPLL is located on the main convergence board. The Horizontal PLL consists of a phase detector (IC19), a low pass filter (IC16B), a voltage controlled oscillator (VCO) (IC15), an ECL to TTL translator (IC 14), a divide-by-256 counting section (IC4), a divide-by-*n* counting section, a phase lead circuit (IC2), and a phase lead look-up table.

The phase detector (IC19) has both an analog and digital output. The outputs are combined and filtered to produce an error voltage which controls the frequency of the VCO (IC15) and biases the network which includes varactor diode D1. The output of the VCO is at ECL logic levels and the ECL to TTL translator (IC14) is used to supply the clock signal, HPLLCLK, to the rest of the module.

HPLLCLK is used to clock the divide-by-256 and divide-by-n counting sections. The divide by 256 counting section generates the Horizontal Zone (time slot) addresses B(0) to B(5) and HPLLCKK/2, HPLLCLK/2* and HPLLCLK/4. The divide-by-n counting section generates the H_LEAD and HRESET signals. At the end of the 256 count, a ripple carry signal disables the divide-by-256 counting section and enables the divide-by-n counting section.

A programmable gate array (IC40) integrates the divide-by-*n* counting section and phase lead circuitry. An initialization pulse, HPLL RST, enables the internal circuitry to determine the number of HPLLCLK pulses that occur in the HFB pulse width. This value, *n* (Q(0) to Q(6)), is stored and used to load the divide-by-*n* counter for insertion into the PLL counting loop.

The analog phase detector (IC19) provides a fixed phase lead of approximately 1.2 µS between the HFB reference and the H_LEAD signal. For modules requiring the HRESET signal to be in phase and sync with the HFB pulse, another programmable divide-by-*n* counting section (in the PGA) provides delay from the divide-by-*n* counting section in the main loop.

The Q(0) to Q(6) values are sent to the phase lead look-up table. This table contains phase lead values to keep HRESET in phase and sync with HFB. These values are loaded into a third programmable counter in the PGA which delays the start of HRESET by an integer multiple of the HPLLCLK clock.

9.1.2.2 Vertical Phase Locked Loop (Vertical PLL)

The vertical PLL section consists of IC29, IC31, and IC27b. The VPLL locks onto the vertical flyback pulse (VFB) and divides the period into 256 segments. A clock signal, VPLLCLK, is generated at 256 times the VFB frequency and is buffered by IC32a. The vertical PLL operates over a VFB range of 40 to 120 Hz. A vertical reset pulse, VRESET, is generated at the end of each 256 count by IC27b.

9.1.2.3 Alpha Generation

The alpha generation circuitry generates an alpha (α) value for every scan line. The alpha value represents the weighting factor required to perform linear interpolation in the vertical direction. It does this independent of the horizontal frequency using a patented method based on horizontal line counting and a look-up table. The alpha generation circuitry consists of IC6, IC7, IC8,IC9, IC24 and IC28.

In implementing vertical interpolation, the raster is divided into 8 vertical zones. Each zone contains an equal integer number of scan lines. This is done by evenly dividing the total number of scan lines in a raster by eight (IC28). This value, *n*, indicates the size of the vertical zone and is stored (IC9). The value *n* forms the MSB address of the look-up table (IC8). The value *n*-1 (IC6) loads a programmable down counter (IC7). The output of down counter forms the LSB address of the look-up table. The LSB address counts down from *n*-1 to 0 at the horizontal rate addressing the alpha values stored for a particular vertical zone size. When the down counter reaches zero, it increments (SCLK) the vertical zone counter (IC26) and reloads itself. The alpha value from the look-up table is output to a selectable invertor/multiplexer which selects between α and 1-α (IC24).

9.1.2.4 RAM Bank Switching

The Convergence module contains 12K of high speed static RAM configured as six banks of 2K x 8 bytes. The banks are mapped into the 8000H to 9FFFH address range of the system's external data memory. The bank switching circuitry (IC20,IC28) allows the microprocessor to individually write/read data to/from any of the six RAM banks. The microprocessor selects a RAM bank by writing to the I/O port SEL0*. This active low signal latches the data for bank selection in IC20. All data memory access into the convergence address space will be referenced to the selected bank until a new bank is selected. See Table 9-1 for RAM bank selection.

9.1.2.5 Band Switch Circuit

The Band Switch Select circuit determines if the projector is operating in the low band or high band. This is done by sensing the horizontal flyback pulse (HFB) which changes from 5.0µS in the low band to 2.5 µS in the high band. The circuit consists of IC10 and IC11a. A 3.0µS reference pulse (IC11a) is compared with the HFB pulse which sets the flip-flop (IC10a). The result is stored in flip-flop IC10b.

9.1.2.6. Address Generation and Multiplexing

The Convergence module uses two address sources:

a) - address lines A0 to A9, and A13 to A15 (generated by the microprocessor)

b) - address lines B0 to B5 (Horizontal Zone Address)
- address lines B6 to B9 (Vertical Zone Address)

Addresses A(0) to A(9) are isolated (IC13, IC32c, IC32d) from addresses B(0) to B(9) and from the convergence RAM. Normally, address lines B(0) to B(9) are presented to the convergence RAM. When the microprocessor accesses the convergence RAM it takes higher priority over the Convergence Module. The signal, ADDRSEL, forces the B(0) to B(9) address lines tristate and enables A(0) to A(9) to the convergence RAM.

The vertical zone address counter (IC26) internally contains two counters with multiplexed outputs (R and C). The R counter contains the current vertical zone address (N) while the C counter contains the next vertical zone address (N+1).

TABLE 9-1. ***Ram Bank Selection***

DATA								DESCRIPTION	LOCATION
D7	D6	D5	D4	D3	D2	D1	D0		
X	X	X	X	X	0	0	0	Blue Vertical RAM	8000H-9FFFH
X	X	X	X	X	0	0	1	Blue Horizontal RAM	8000H-9FFFH
X	X	X	X	X	0	1	0	Green Vertical RAM	8000H-9FFFH
X	X	X	X	X	0	1	1	Green Horizontal RAM	8000H-9FFFH
X	X	X	X	X	1	0	0	Red Vertical RAM	8000H-9FFFH
X	X	X	X	X	1	0	1	Red Horizontal RAM	8000H-9FFFH
X	X	X	X	X	1	1	0	Not Used	
X	X	X	X	X	1	1	1	Not Used	

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9.2.1.7 Waveform Channel

There are six waveform channels physically located on the Subconvergence PCB. These channels generate the waveforms that are output by the module. The channels are: Blue Vertical, Blue Horizontal, Green Vertical, Green Horizontal, Red Vertical and Red Horizontal. The channels are identical; each consists of:

(1) **2K x 8 static RAM** (IC41, IC43, IC45, IC47, IC49, IC51)
(1) **74HC245 octal bus transceiver** (IC40, IC42, IC44, IC46, IC48, IC50)
(1) **7545 12-bit multiplying DAC with latch** (IC57, IC61, IC64, IC67, IC71, IC73)
(1) **MC34082 biFET op-amp** (IC56, IC60, IC63, IC66, IC68, IC70)
(1/6) **74HC04 Invertor** (IC58)

Each channel has a potentiometer (R168, R176, R184, R192, R200, R208) which adjusts the reference voltage to the DAC. It is adjusted such that the convergence output waveform is 0V when the convergence RAM is reset (filled with 00H).

The user adjustable convergence points are interpolated by the microprocessor into 9 rows of 64 values for each color and axis. Between any two rows, interpolated values are calculated according to the equation:

$P=(1-\alpha) \times (HADRR,VADDR) + \alpha \times (HADDR,VADDR+1)$

The 9 rows of interpolated values correspond to the boundaries of the 8 vertical zones. Each vertical zone contains an equal number of scan lines. Each scan line receives a unique value of α depending on its position within the vertical zone. The horizontal address (B(0) to B(5)) divide the active horizontal scan line time into 64 equal time slots. Each time slot is divided into 2 by HPLLCLK/4 and divided into 4 by HPLLCK/2 and HPLLCLK/2*.

Consider one HADDR time slot:

In the first quarter of the time slot, HPLLCLK/2 is low, HPLLCLK/2* is high and HPLLCLK/4 is low. With HPLLCLK/4 low, VADDR+1 (IC26) is multiplexed to the RAM and α is inverted (IC24) to give $1-\alpha$. The two values are presented to the X and Y inputs of the MAC and clocked in on the rising edge of HPLLCLK/2.

In the second quarter of the time slot, HPLLCLK/2 is high, HPLLCLK/2* is low and HPLLCLK/4 is low. During this time period the multiplication of (HADDR,VADDR+1) and $(1-\alpha)$ is performed and the result is clocked out on the rising edge of HPLLCLK/2*. Since the ACC pin on the MAC is low the product generated is stored into the output registers.

In the third quarter of the time slot, HPLLCLK/2 is low, HPLLCLK/2* is high and HPLLCLK/4 is high. With HPLLCLK/4 high, VADDR is multiplexed to the RAM and α is not inverted. The two values are presented to the X and Y inputs of the MAC and clocked in on the rising edge of HPLLCLK/2.

In the forth quarter of the time slot, HPLLCLK/2 is high, HPLLCLK/2* is low and HPLLCLK/4 is high. During this time period the multiplication of (HADDR,VADDR) and α is performed and added to the product (HADDR,VADDR+1) x $(1-\alpha)$ since the ACC input of the MAC is high. The result is clocked out on the rising edge of HPLLCLK/2*.

During the next first half of the next time slot, HPLLCLK/4 is low. The WR* pin of the 7545 DAC is low and the newly calculated value for HADDR = 1 time slot is converted to an analog value. During the second half of the next time slot HPLLCLK/4 is high. The WR* pin of the 7545 DAC is high and the value for the HADDR = 1 time slot is latched for the rest of the time slot.

This is repeated for each horizontal time slot of each scan line in each vertical zone.

9.2 SERVICING AND ALIGNMENT

9.2.1 Disassembly and Access

CAUTION

STATIC SENSITIVE COMPONENTS
STATIC CONTROLLED WORK STATION REQUIRED

Module Location:
▸ rear panel card rack

Tools & Equipment Required:
▸ Phillips screw driver

a) Remove the back panel as described in Section 5.

b) Locate the Convergence module in the rear panel card rack. Using the printed circuit board extractor from the tool pouch, pull the module from the card rack as described in Section 5.2.

9.2.2 Alignment

If the projector convergence cannot be performed adequately with the keypad, or it is desired to readjust the on board convergence settings, proceed as follows:

Tools & Equipment Required:
- printed circuit board extractor
- extender board, Vidikron Part # A-03-230330-01P
- oscilloscope
- fine tip slot screwdriver

STEP 1 - Remove Convergence Module

a) Hook the printed circuit board extractor into the hole in the bottom outside corner of the Convergence module. Pull the module out of its slot.

b) Insert the extender board into the Convergence module slot. Put the Convergence module on the extender board. See Figure 9-1.

STEP 2 - Reset Convergence to 0

a) Press **CONVERGE** and **2** on the keypad. Press and hold **RESET** for 2 seconds minimum.

STEP 3 - Null Colors

a) With a digital voltmeter and the fine tip screwdriver, make the following adjustments:
- Adjust R168 until extender board row C, pin 1 = 0V.
- Adjust R176 until extender board row C, pin 2 = 0V.
- Adjust R184 until extender board row C, pin 3 = 0V.
- Adjust R192 until extender board row C, pin 4 = 0V.
- Adjust R200 until extender board row C, pin 5 = 0V.
- Adjust R208 until extender board row C, pin 6 = 0V.

b) Press **EXIT**.

STEP 4 - Phase Lead Adjust

Perform this procedure if the cross hatch, when displayed, is shifted too far to the right of the screen.

a) Locate the DIP switch (SW1) at the front edge of the module.

b) There are four switches on SW1. Only the center two switches are active (SW1-2 and SW1-3). To shift the crosshatch pattern slightly to the left, set the SW1 switch settings to that shown below.

	40HD Series		80HD Series	
	SW1-2	SW1-3	SW1-2	SW1-3
Factory Default	OFF	ON	OFF	OFF
Phase Shift (left)	ON	ON	ON	OFF

9.3 COMPONENT LAYOUT AND SCHEMATICS

Refer to the following pages for component layouts and schematics of the Convergence module.

54-7599-01P

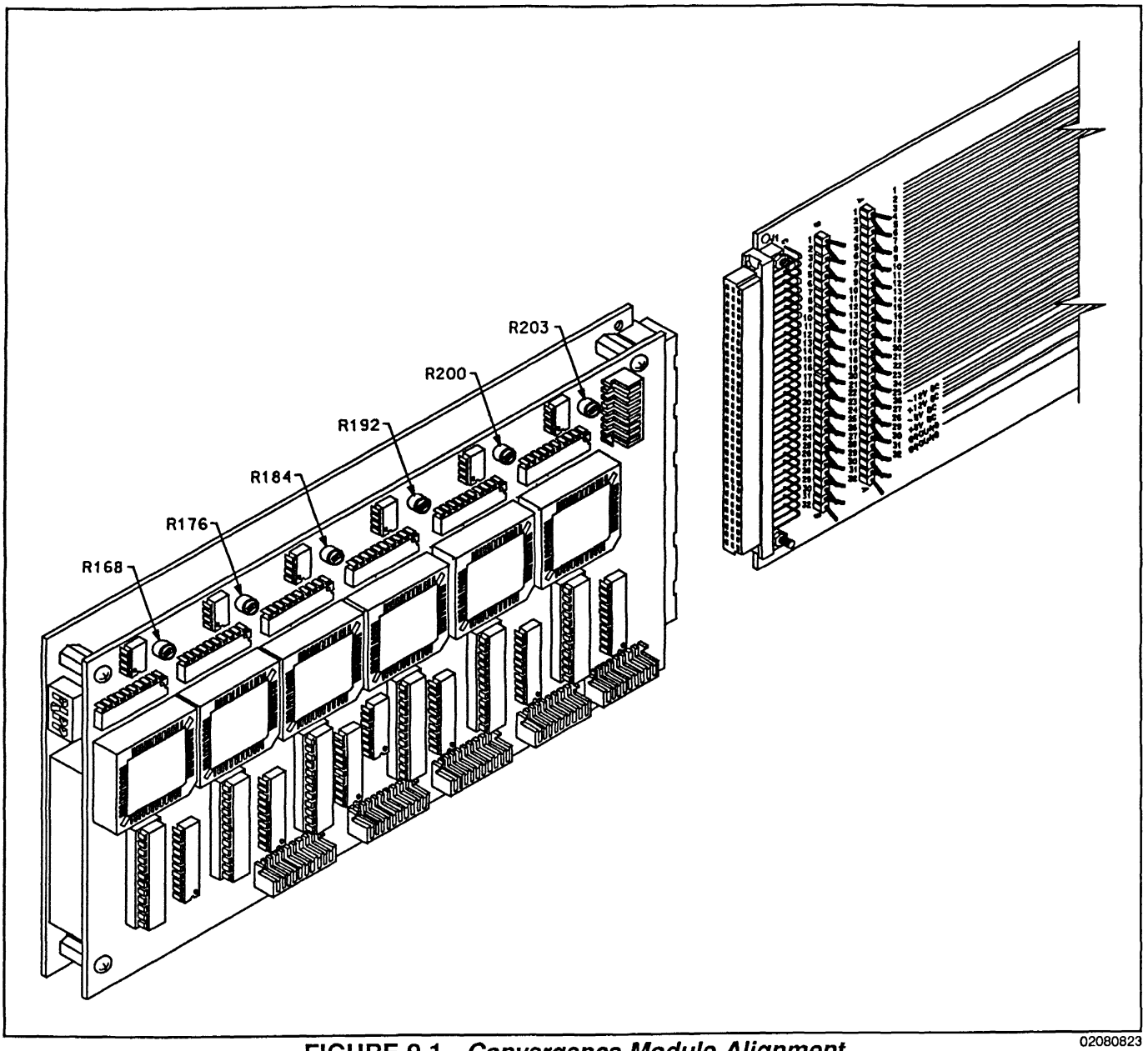
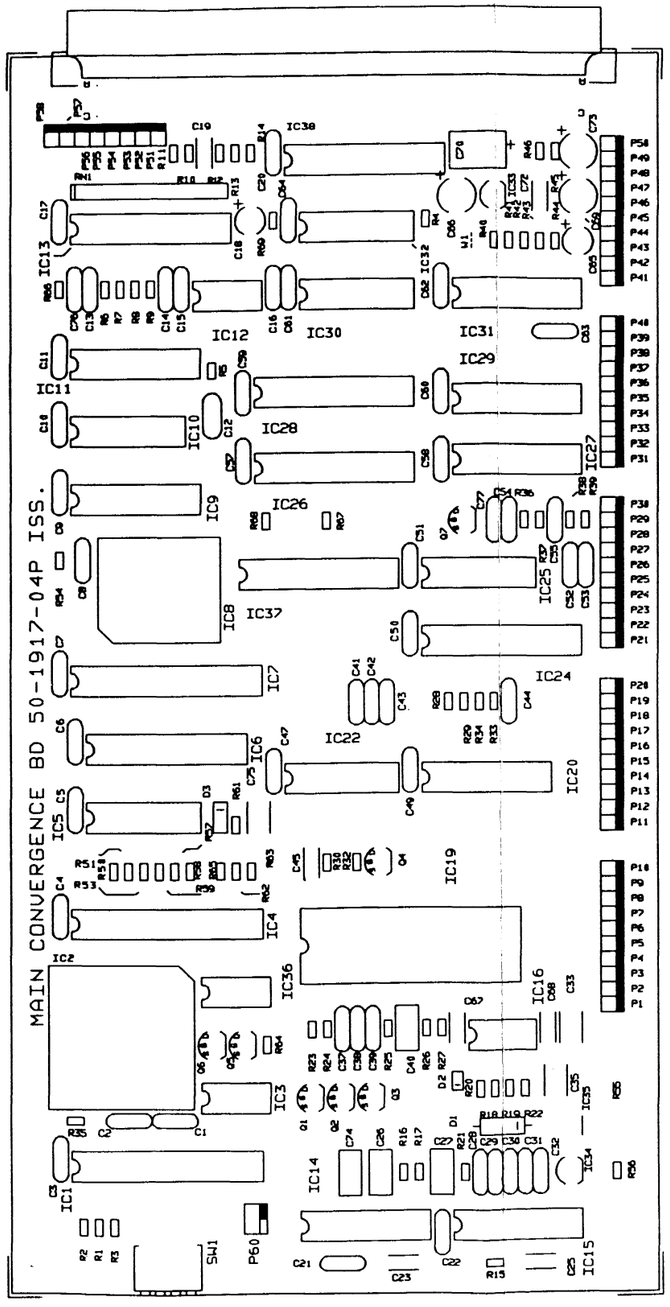
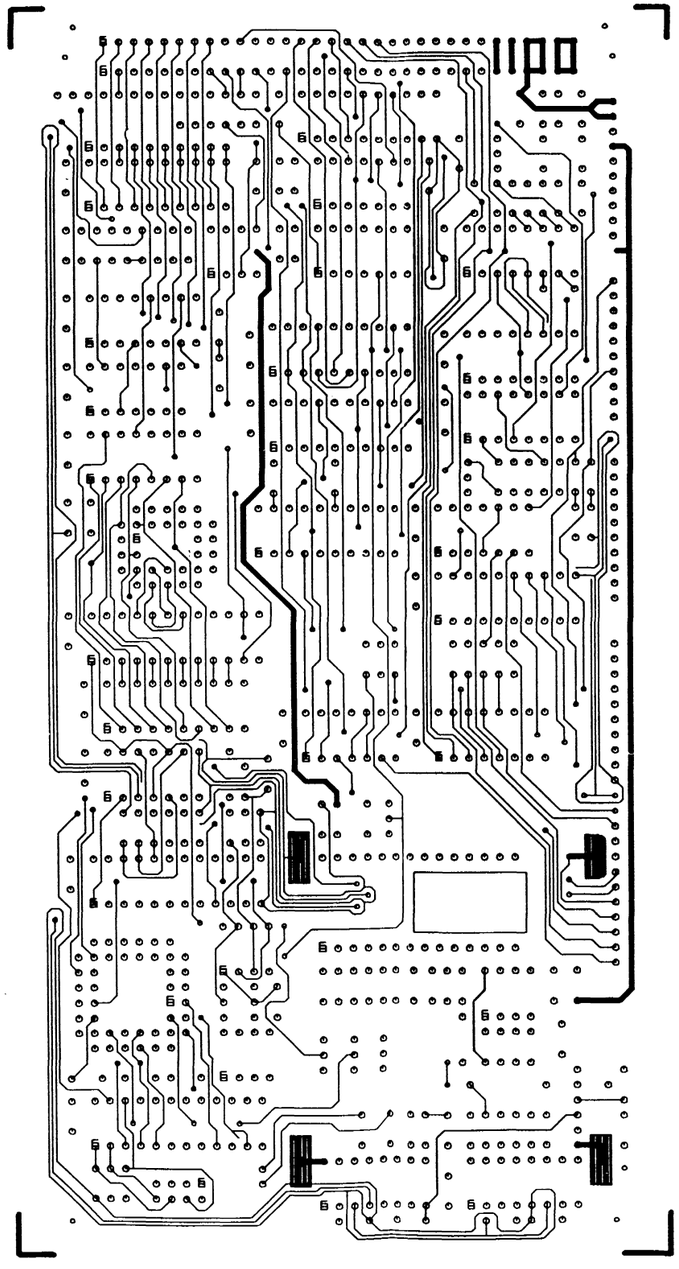


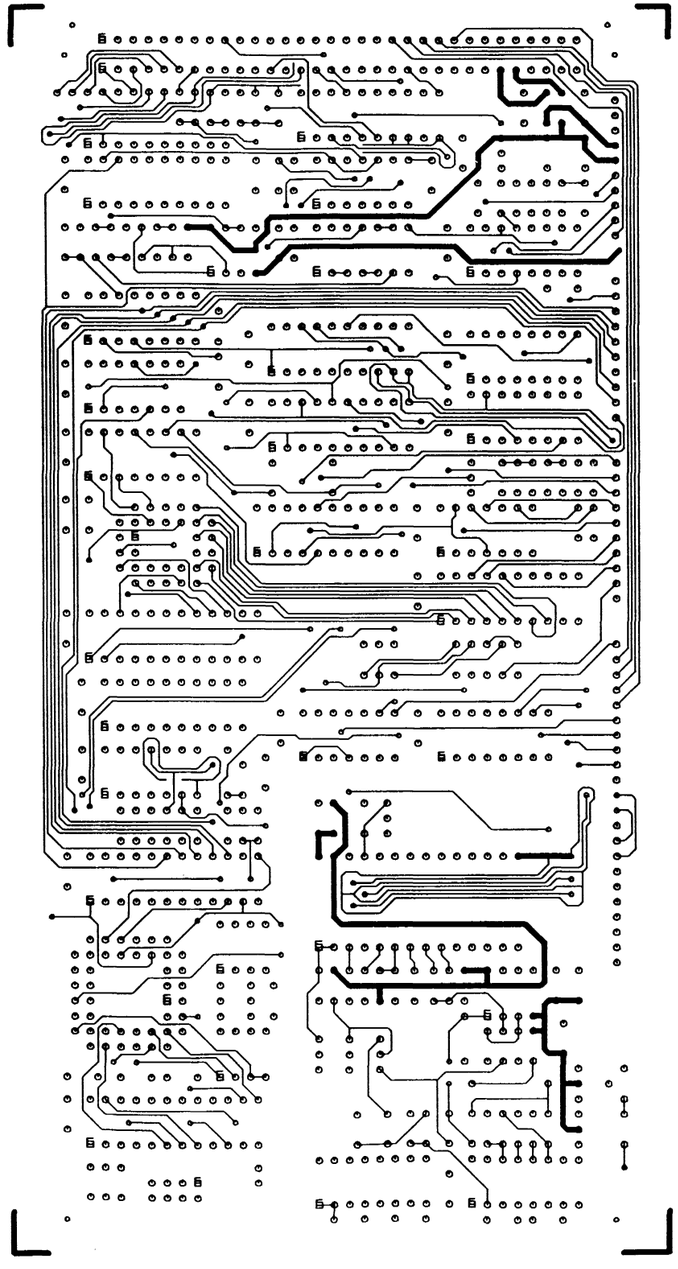
FIGURE 9-1. *Convergence Module Alignment*



Component Layout



Solder Side
(Viewed from Component Side)



Component Side

FIGURE 9-2. *Convergence PCB Component Layout*

NOTE: The main Convergence PCB is a four layer board. The two inner layers are ground plane and power plane. Since the inner lay foils can be difficult to read, the diagram on the left just shows the ground and power connection locations.

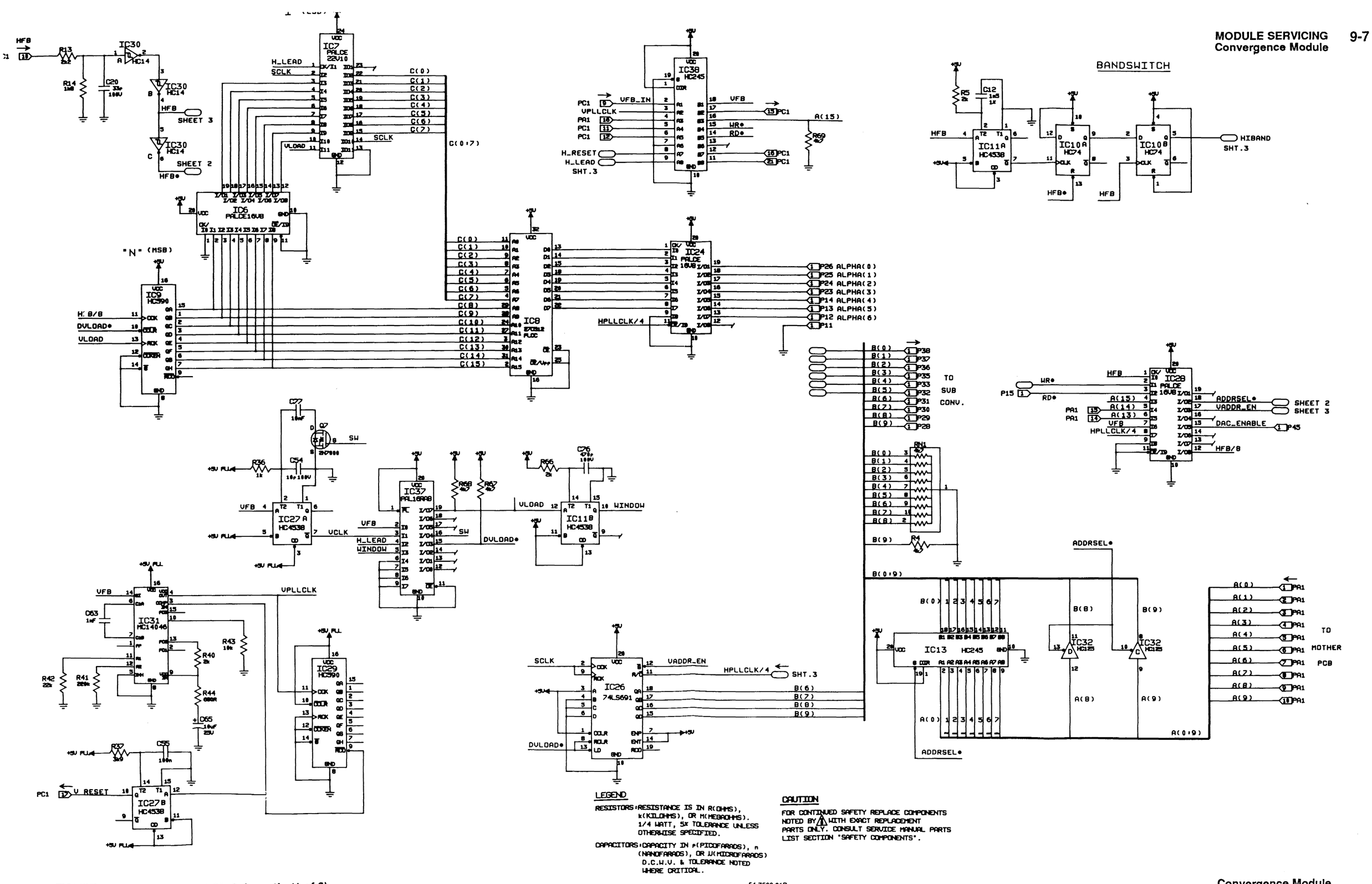


FIGURE 9-3. *Convergence PCB Schematic (1 of 3)*
00-270007-03P

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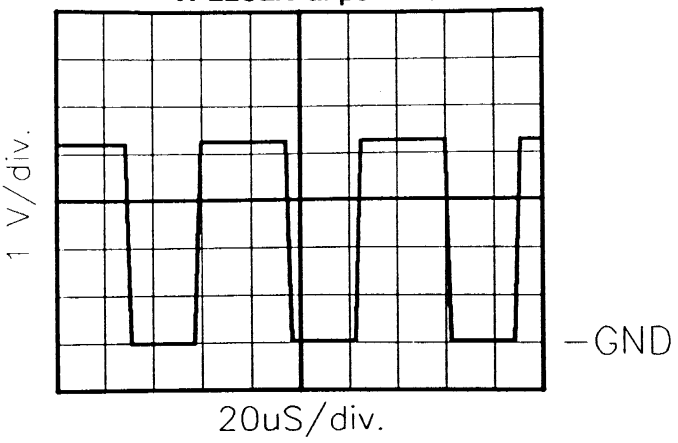
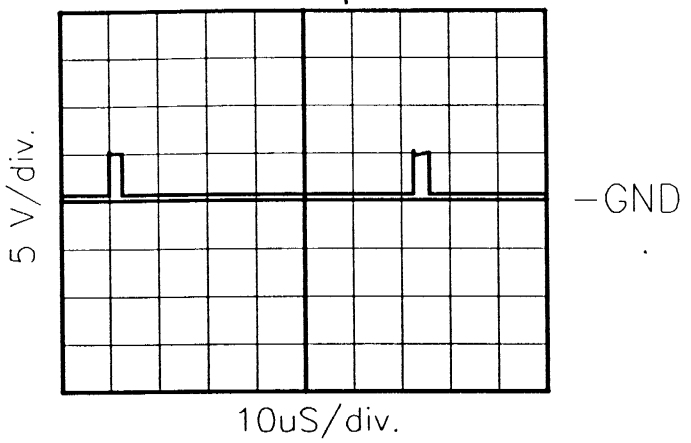
SCHEMATIC REFERENCE

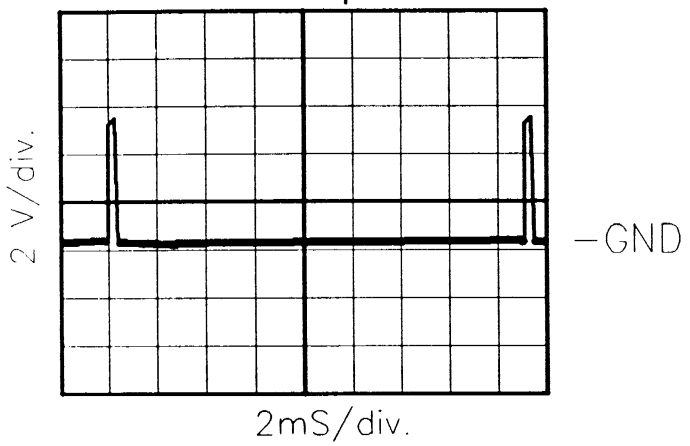
VPLLCLK at point **PC1<15**



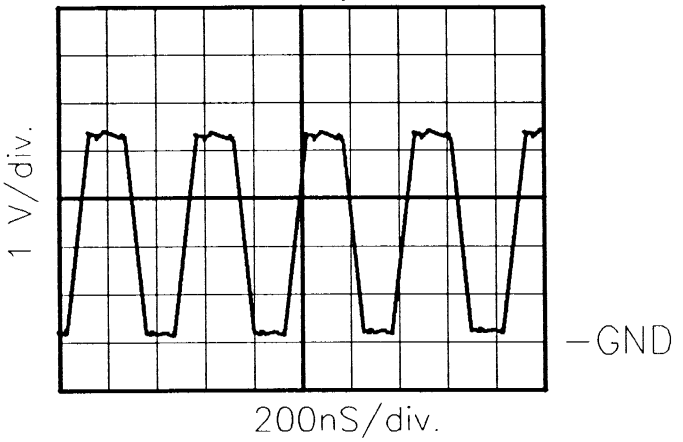
H RESET at point **PB1<16**



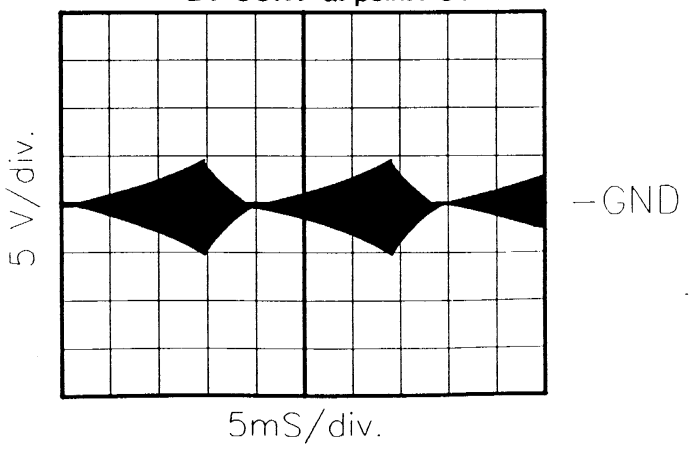
V RESET at point **PB1<17**



HPLLCLK at point **PC1<14**



BV CONV at point **PC1<1**



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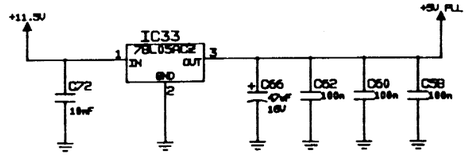

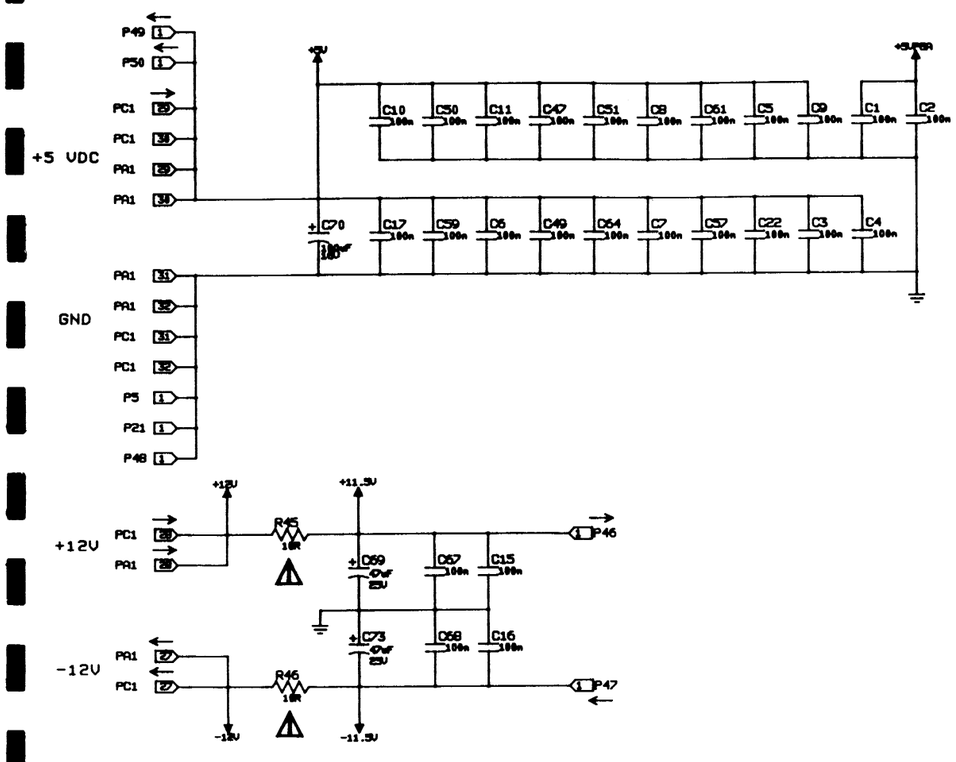

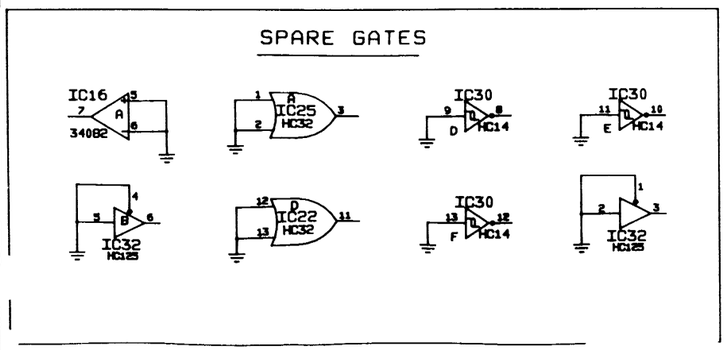

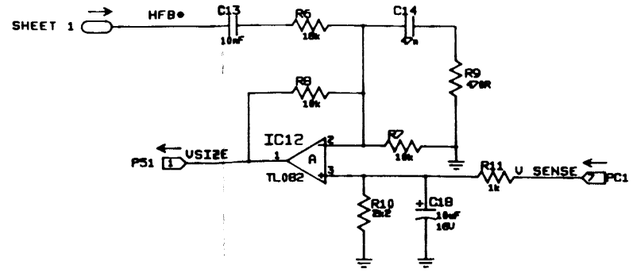

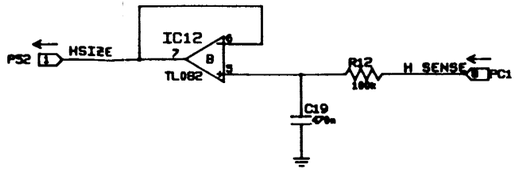

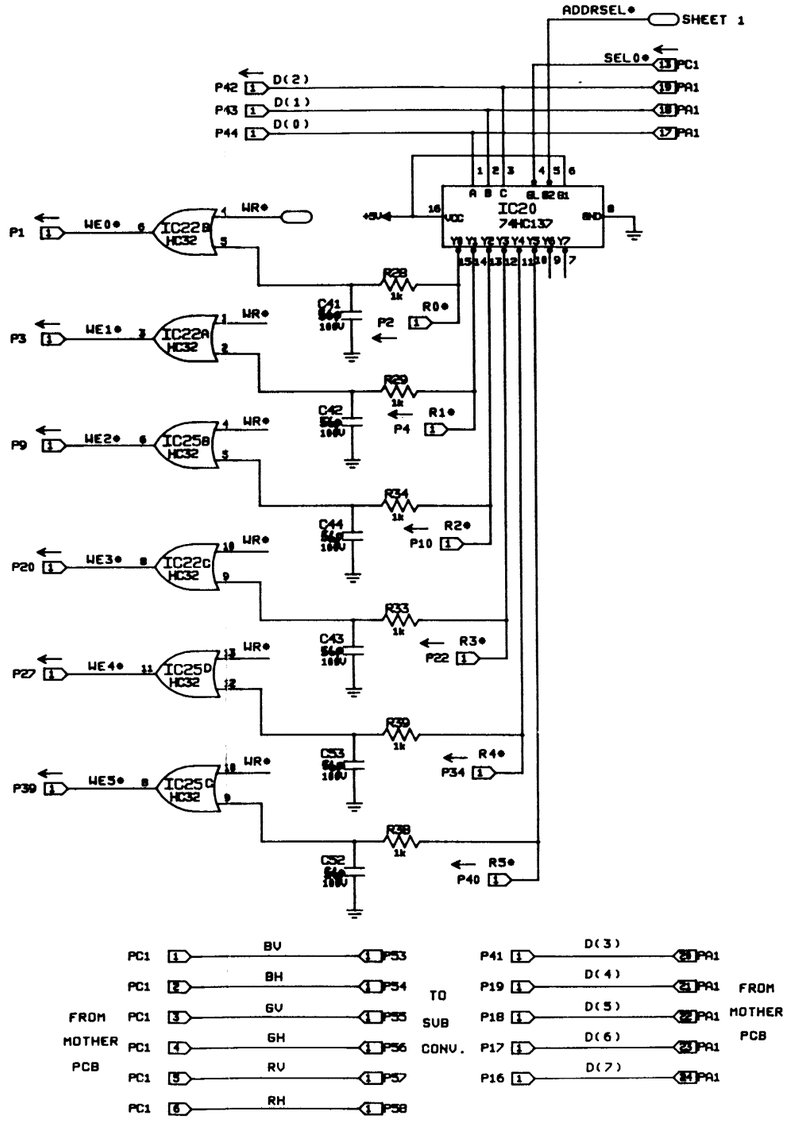

FIGURE 9-4. *Convergence PCB Schematic (2 of 3)*
00-270007-03P

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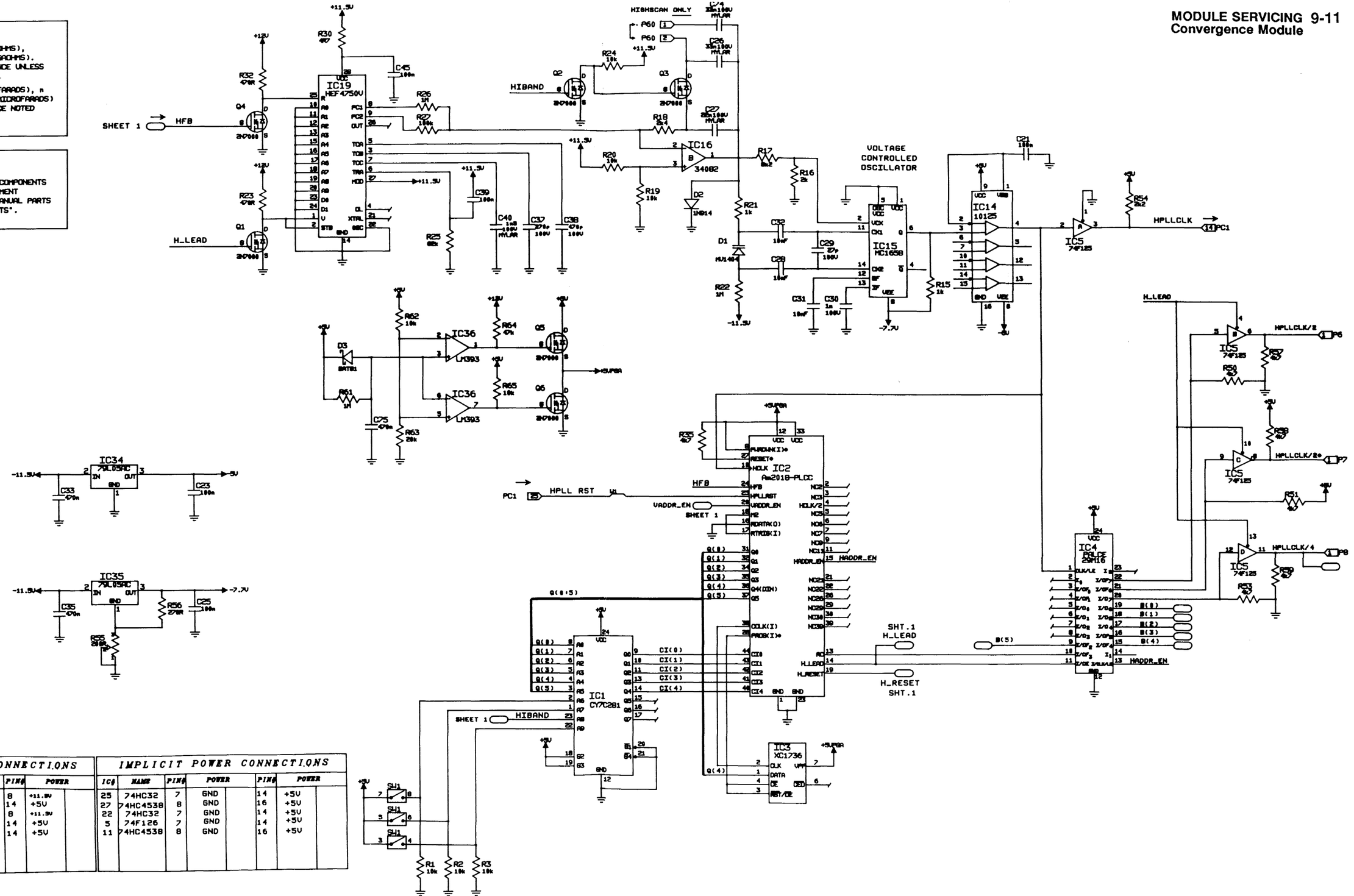
LEGEND

RESISTORS: RESISTANCE IS IN R(OHMS), k(KILOHMS), OR M(MEGAOHMS). 1/4 WATT, 5% TOLERANCE UNLESS OTHERWISE SPECIFIED.

CAPACITORS: CAPACITY IN p(PICOFARADS), n (NANOFARADS), OR µ(MICROFARADS) D.C.W.V. & TOLERANCE NOTED WHERE CRITICAL.

CAUTION

FOR CONTINUED SAFETY REPLACE COMPONENTS NOTED BY ⚠ WITH EXACT REPLACEMENT PARTS ONLY. CONSULT SERVICE MANUAL PARTS LIST SECTION "SAFETY COMPONENTS".

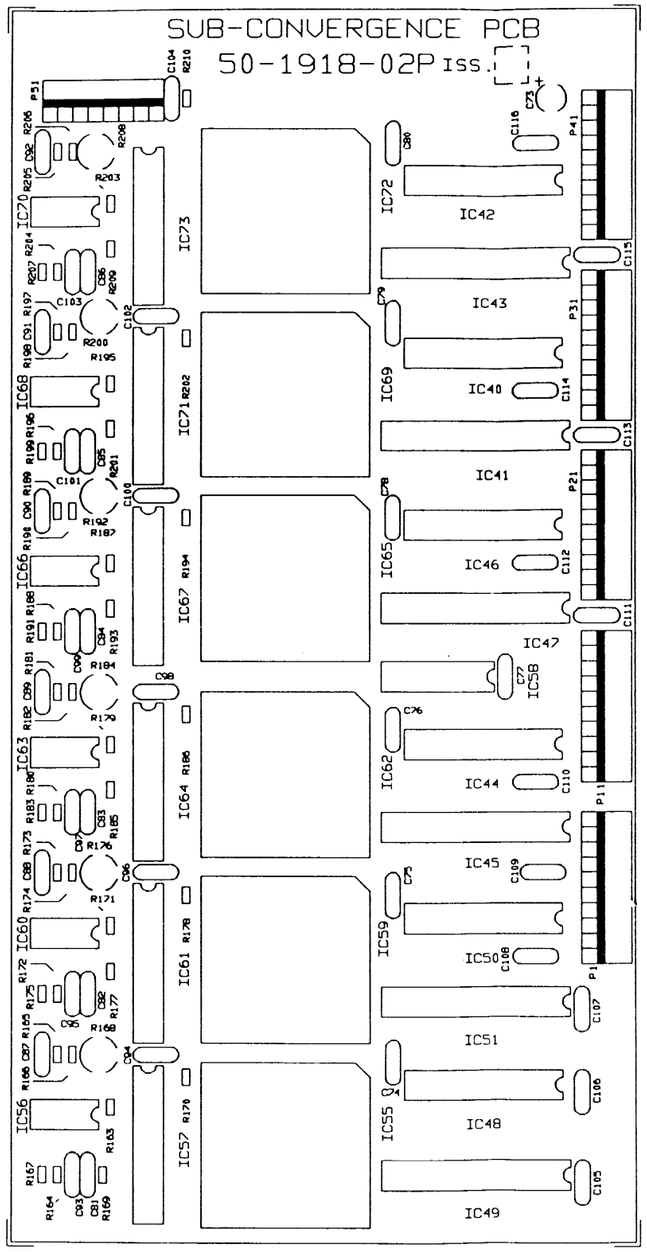


IMPLICIT POWER CONNECTIONS					
IC#	NAME	PIN#	POWER	PIN#	POWER
12	TL082	4	-11.5V	8	+11.5V
10	74HC74	7	GND	14	+5V
16	MC34082	4	-11.5V	8	+11.5V
30	74HC14	7	GND	14	+5V
32	74HC125	7	GND	14	+5V

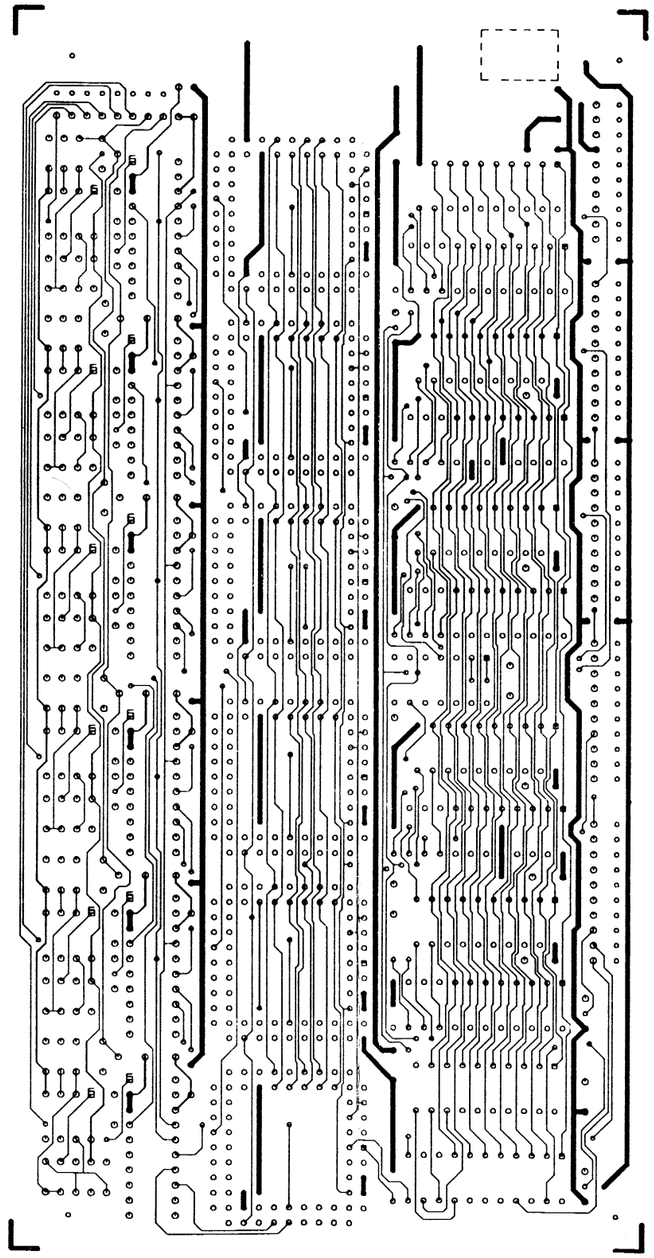
IMPLICIT POWER CONNECTIONS					
IC#	NAME	PIN#	POWER	PIN#	POWER
25	74HC32	7	GND	14	+5V
27	74HC4538	8	GND	16	+5V
22	74HC32	7	GND	14	+5V
5	74F126	7	GND	14	+5V
11	74HC4538	8	GND	16	+5V

FIGURE 9-5.

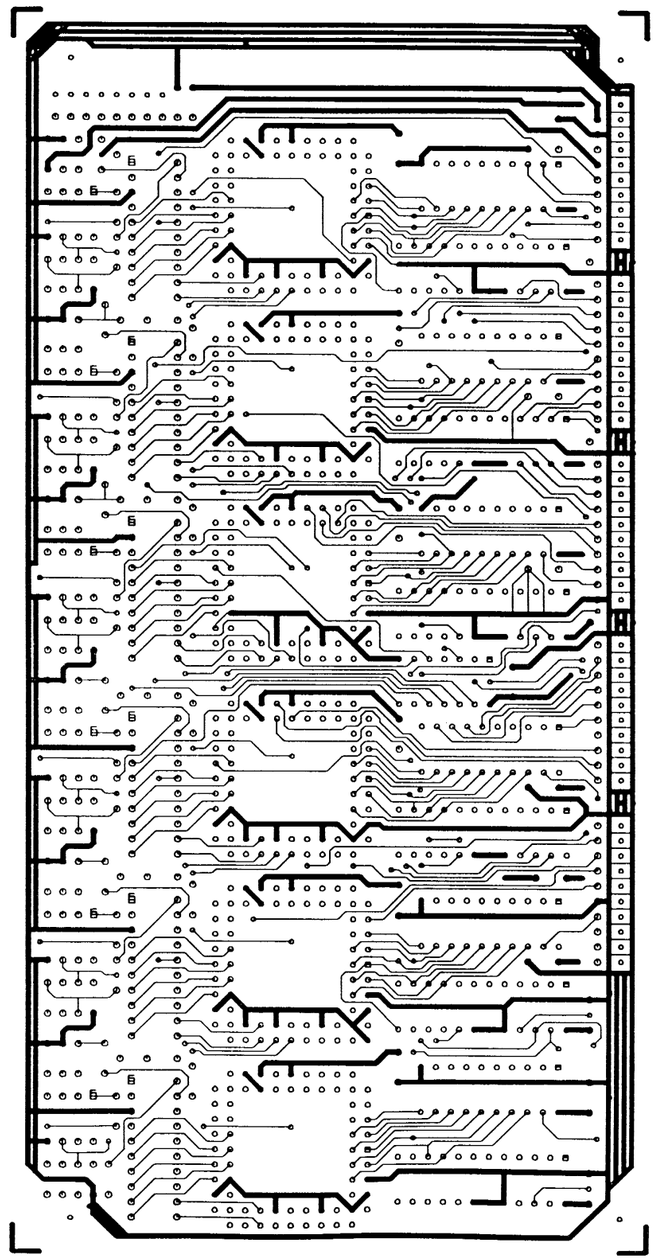
Convergence PCB Schematic (Sheet 3 of 3)



Component Layout



Solder Side
(Viewed from Component Side)



Component Side

FIGURE 9-6. *Sub-convergence PCB Component Layout*

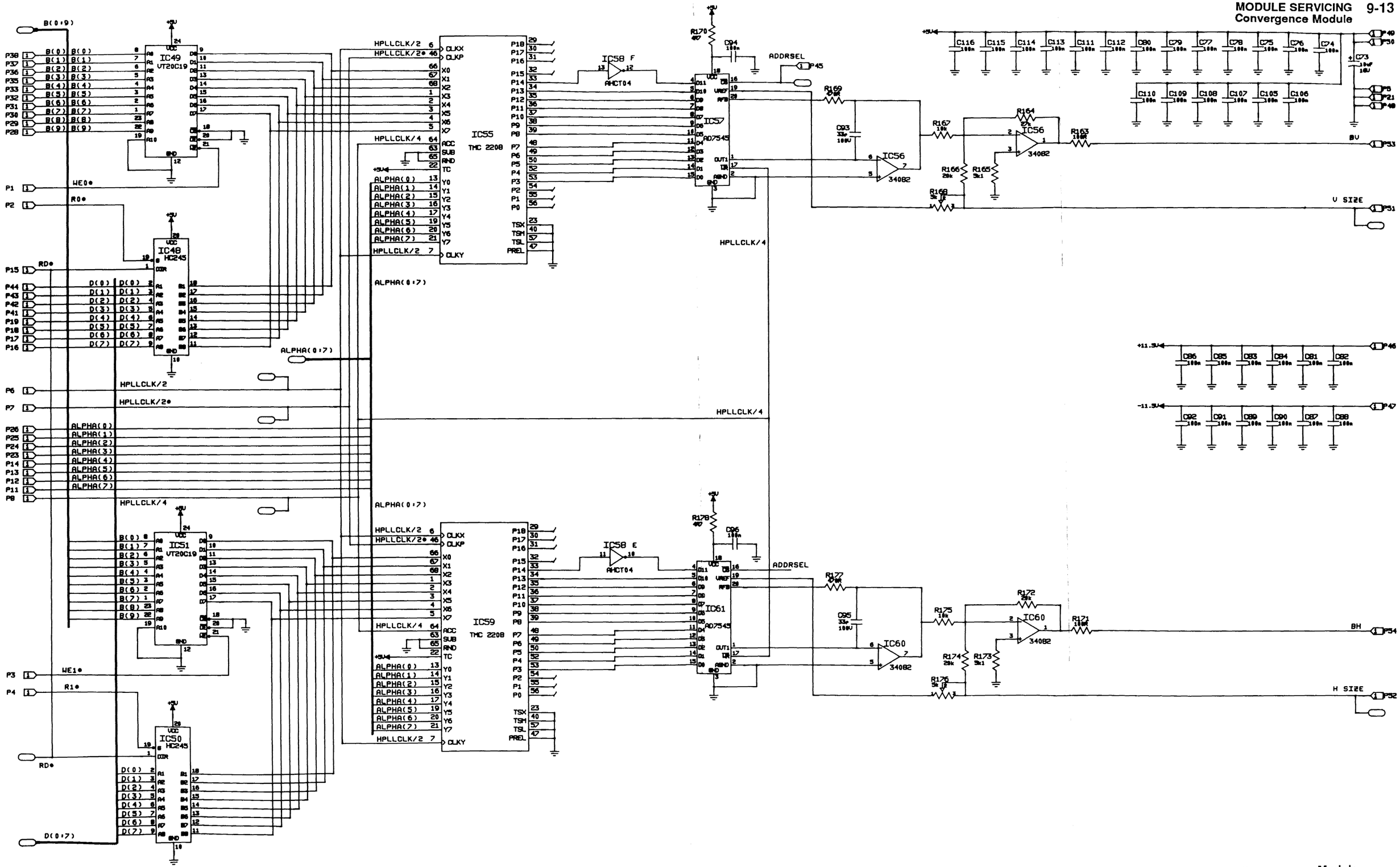


FIGURE 9-7. *Sub-convergence PCB Schematic (1 of 3)*

00-250007-02P

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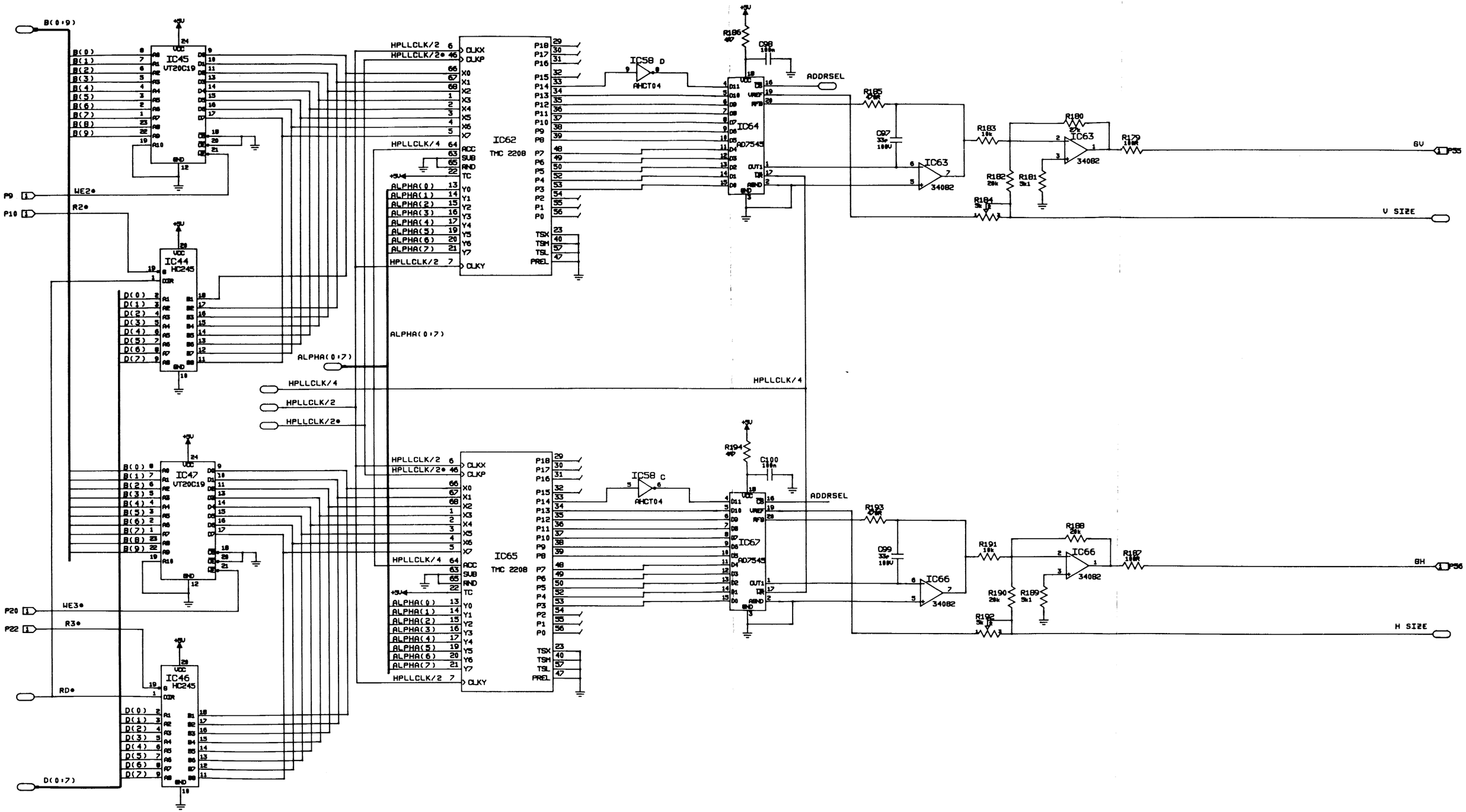

FIGURE 9-8. *Sub-convergence PCB Schematic (2 of 3)*
00-250007-02P

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54-7599-01P

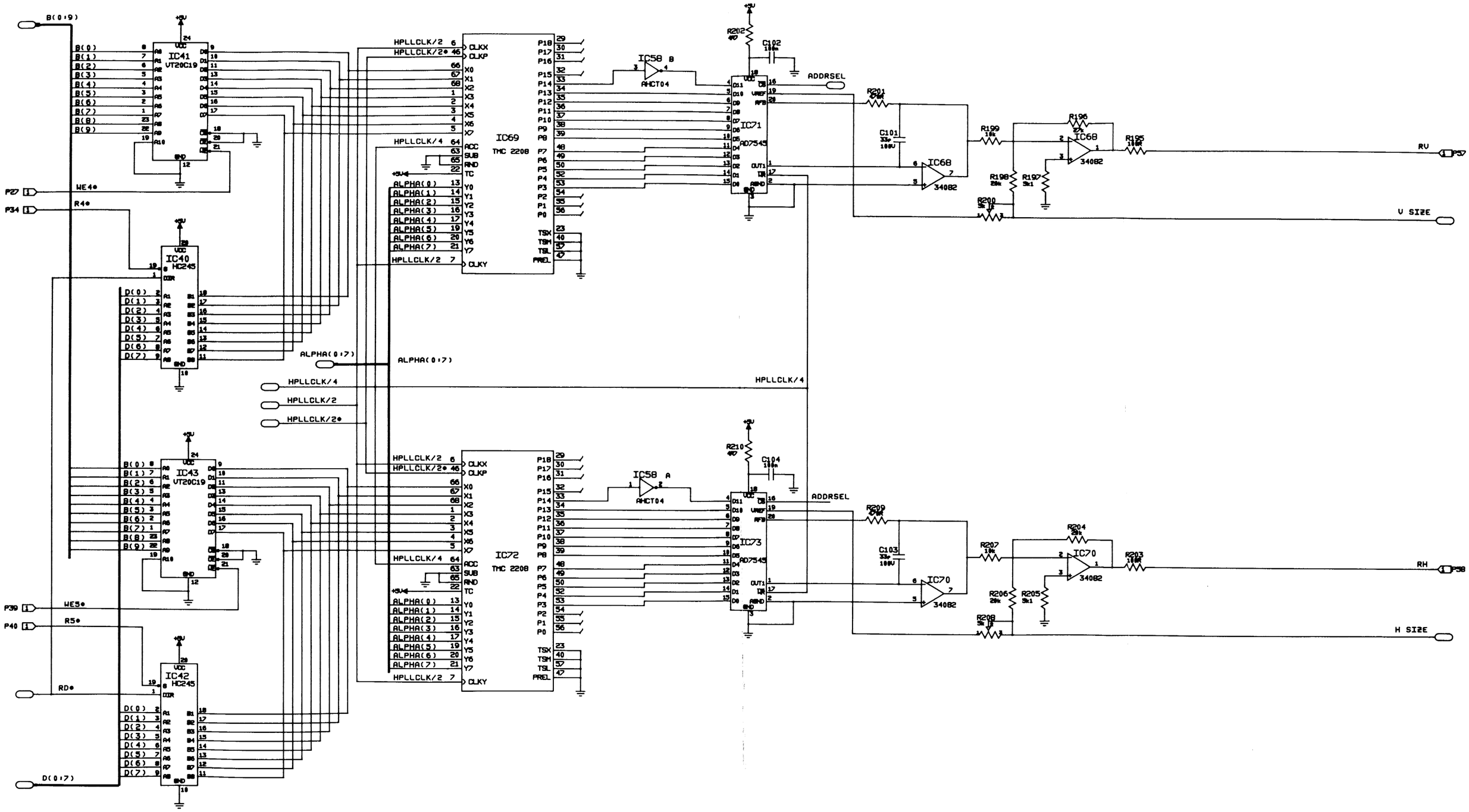

FIGURE 9-9. *Sub-convergence PCB Schematic (3 of 3)*
00-250007-02P

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54-7599-01P

9.4 PARTS LIST

⚠ - CRITICAL SAFETY COMPONENT
(REPLACE WITH IDENTICAL PART)

9.4.1 Convergence PCB

Item Ref.	Part No.	Description
Integrated Circuits		
IC5	IC-14-004703-01P	74F126, tri-state non-inverting buffer
IC9,IC29	IC-14-A04067-01P	74HC590, 8 bit binary counter
IC10	IC-14-A04007-01P	74HC74, H-CMOS dual flip-flop
IC11,IC27	IC-14-A04041-01P	MM14538B, CMOS, precision dual monostable
IC12	IC-14-002813-09P	TL082BC, linear op amp
IC13,IC38	IC-14-A04042-01P	74HC245, octal bus transceiver
IC14	IC-14-003053-01P	MC10125, quad MCCL TO TTL translator
IC15	IC-14-004701-01P	SP1658, digital multivibrator voltage control
IC16	IC-14-002164-02P	MC34082, dual linear j-fet op-amp
IC19	IC-14-A04088-01P	HEF4750V, frequency synthesizer
IC20	IC-14-A04044-01P	74HC137, 3-8 line dec. demultiplexer
IC22,IC25	IC-14-A04005-02P	74HC32, 2-input quad
IC26	IC-14-004697-01P	74LS691, sync controller
IC30	IC-14-A04073-01P	74HC14, hex schmitt trigger inverter
IC31	IC-14-A02006-02P	MC14046, CMOS phase lock loop
IC32	IC-14-A04078-01P	74HC125, digital quad bus buffer
IC33	IC-14-002814-02P	LM78L05ACZ, +5V regulator
IC34,IC35	IC-14-002844-01P	MC79L05AC, negative voltage regulator
Transistors and Diodes		
Q1-Q4,Q7	TR-14-A00705-01P	2N7000, TMOS, 60V, 0.2A, 4W
D1	DV-14-000519-02P	MV1404, varactor, 120pF
D2,D4	D-14-000513-01P	1N914, diode, 0.075A, 75V
Capacitors		
C1-C3,C5-C11, C15-C17,C21-C23,C25, C39,C45,C47,C49-C51, C55,C57-C62,C64,C67, C68	C-89-000032-03P	100 nF, 50V, 20%, ceramic, multi layer
C12	C-89-000033-04P	1.5 nF, 1%, 50V, NPO, ceramic, multi layer
C13,C28,C31,C32,C72, C77	C-89-000032-04P	10 nF, 50V, 20%, ceramic, multi layer
C14	C-89-000032-09P	4.7 nF, 50V, 20% Z5U, ceramic, multi layer
C18,C65	C-84-710003-02P	10 µF, 25V, "super mini", electolytic
C19,C33,C35	C-89-000032-02P	0.47 µF, 50V, ±20%, ceramic, multi layer
C20	C-86-633032-04P	33 pF, 100V, ceramic
C26,C74	C-88-173331-01P	33 nF, 100V mylar
C27	C-88-172231-02P	22 nF, 100V, mylar
C29	C-86-627032-04P	27pF, 100V, ceramic
C30	C-86-610252-02P	1 nF, 100V, ceramic
C37	C-86-627151-02P	270 pF, 100V, 10%, ceramic
C38,C76	C-86-647151-02P	470 pF, 100V, ceramic
C40	C-88-171521-01P	1.5 nF, 100V, 20%, mylar
C41-C44,C52,C53	C-86-682034-04P	82 pF, 2%, 100V, ceramic
C54	C-86-610031-04P	10 pF, ceramic
C63	C-89-000032-05P	1 nF, 50V, 20%, ceramic, multi layer

9.4 PARTS LIST (cont.)

⚠ - CRITICAL SAFETY COMPONENT
(REPLACE WITH IDENTICAL PART)

9.4.1 Convergence PCB (cont.)

Item Ref.	Part No.	Description
Capacitors (cont.)		
C66,C69,C73	C-84-747002-03P	47 µF, 16V, "super mini", electolytic
C70	C-84-410104-03P	100 µF, 25V, electolytic
C78	C-86-622032-04P	22pF, 100V, ceramic
C79	C-86-315113-51P	150 pF, 50V, Z5P, ceramic disc
Resistors		
R2,R3,R7,R8,R19,R20, R24,R43	R-80-110025-11P	10K, 1/2W, 5%, metal film
R4,R50,R51,R53, R57-R59,R67-R69	R-80-147015-11P	4.7K, 1/2W, 5%, metal film
R5,R16,R40,R66	R-80-120015-11P	2K, 1/2W, 5%, metal film
R6	R-80-118025-11P	18K, 1/2W, 5%, metal film
R9,R23,R32,R70	R-80-147005-11P	470R, 1/2W, 5%, metal film
R10,R13,R54	R-80-122015-11P	2.2K, 1/2W, 5%, metal film
R11,R15,R21,R28,R29, R33,R34,R36,R38,R39, R71	R-80-110015-11P	1K, 1/2W, 5%, metal film
R12,R27	R-80-110035-11P	100K, 1/2W, 5%, metal film
R14	R-80-118015-11P	1.8K, 1/2W, 5%, metal film
R17	R-80-182015-11P	8.2K, 1/2W, 5%, metal film
R18	R-80-124015-11P	2.4K, 1/2W, 5%, metal film
R22,R26	R-80-110045-11P	1M, 1/2W, 5%, metal film
R25	R-80-162025-11P	62K, 1/2W, 5%, metal film
R30	R-80-147085-11P	4.7R, 1/2W, 5%, metal film
R37	R-80-139015-11P	3.9K, 1/2W, 5%, metal film
R41	R-80-122035-11P	220K, 1/2W, 5%, metal film
R42,R75	R-80-122025-11P	22K, 1/2W, 5%, metal film
R44	R-80-168005-11P	680R, 1/2W, 5%, metal film
R45,R46	R-80-110095-11P	10R, 1/2W, 5%, metal film
R55	VR-41-000370-05P	200R, trim pot
R56	R-80-127005-11P	270R, 1/2W, 5%, metal film
RN1	RN-43-000053-01P	4.7K, 10 pin, resistor network
Miscellaneous		
SW1	SW-26-000346-04P	switch, rocker, SPST

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9.4 PARTS LIST (cont.)

⚠ - CRITICAL SAFETY COMPONENT
(REPLACE WITH IDENTICAL PART)

9.4.2 Sub-convergence PCB

Item Ref.	Part No.	Description
Integrated Circuits		
IC40,IC42,IC44,IC46, IC48,IC50	IC-14-A04042-01P	74HC245, octal bus transceiver
IC41,IC43,IC45,IC47, IC49,IC51	IC-14-A05046-02P	VT20C19-20NS, high speed SRAM
IC56,IC60,IC63,IC66, IC68,IC70	IC-14-002164-02P	MC34082, dual linear j-fet op-amp
IC57,IC61,IC64,IC67, IC71,IC73	IC-14-A03040-01P	HDAC7545A, buffered multiplying DAC
IC58	IC-14-A04075-01P	74AHCT04, hex inverter
IC55,IC59,IC62,IC65, IC69,IC72	IC-14-A04087-01P	TMC2208, multiplier accumulator
Capacitors		
C73	C-84-410004-01P	10 OF, 25V, electolytic
C74-C92,C94,C96,C98, C100,C102,C104-C116	C-89-000032-03P	100 nF, 50V, 20%, ceramic, multi layer
C93,C95,C97,C99,C101, C103	C-86-633032-04P	33 pF, 100V, ceramic
Resistors		
R163,R171,R179,R187, R195,R203	R-80-110005-11P	100R, 1/2W, 5%, metal film
R165,R173,R181,R189, R197,R205	R-80-151015-11P	5.1K, 1/2W, 5%, metal film
R166,R172,R174,R182, R188,R190,R198,R204, R206	R-80-120025-11P	20K, 1/2W, 5%, metal film
R167,R175,R183,R191, R199,R207	R-80-110025-11P	10K, 1/2W, 5%, metal film
R168,R176,R184,R192, R200,R208	VR-41-000370-09P	5K, cermet trim pot., single turn
R164,R180,R196	R-80-127025-11P	27K, 1/2W, 5%, metal film
R169,R177,R185,R193, R201,R209	R-80-147005-11P	470R, 1/2W, 5%, metal film
R170,R178,R186,R194, R202,R210	R-80-147085-11P	4.7R, 1/2W, 5%, metal film

9.5 SPECIFICATIONS

Connector P1, Row A:

Pin 1 . . . . . digital input, address line **A(0)**
Pin 2 . . . . . digital input, address line **A(1)**
Pin 3 . . . . . digital input, address line **A(2)**
Pin 4 . . . . . digital input, address line **A(3)**
Pin 5 . . . . . digital input, address line **A(4)**
Pin 6 . . . . . digital input, address line **A(5)**
Pin 7 . . . . . digital input, address line **A(6)**
Pin 8 . . . . . digital input, address line **A(7)**
Pin 9 . . . . . digital input, address line **A(8)**
Pin 10 . . . . . digital input, address line **A(9)**
Pin 11 . . . . . digital input, address line **A(10)**
Pin 12 . . . . . digital input, address line **A(11)**
Pin 13 . . . . . digital input, address line **A(12)**
Pin 14 . . . . . digital input, address line **A(13)**
Pin 15 . . . . . digital input, address line **A(14)**
Pin 16 . . . . . digital input, address line **A(15)**

Pin 17 . . . . . digital in/output, data line **D(0)**
Pin 18 . . . . . digital in/output, data line **D(1)**
Pin 19 . . . . . digital in/output, data line **D(2)**
Pin 20 . . . . . digital in/output, data line **D(3)**
Pin 21 . . . . . digital in/output, data line **D(4)**
Pin 22 . . . . . digital in/output, data line **D(5)**
Pin 23 . . . . . digital in/output, data line **D(6)**
Pin 24 . . . . . digital in/output, data line **D(7)**

Pin 27 . . . . . -12V power supply **-12 VDC**
current . . . . . 50 mA max

Pin 28 . . . . . +12V power supply **+12 VDC**
current . . . . . 90 mA max

Pin 29 . . . . . +5V power supply **+5 VDC**
current . . . . . 200 mA max

Pin 30 . . . . . connected to Pin 29 **+5 VDC**

Pin 31 . . . . . ground **GND**

Pin 32 . . . . . connected to Pin 31 **GND**

Connector P1, Row C:

Pin 1 . . . . . analog output **BV CONV**
signal level . . . . . -8 to 8V peak

Pin 2 . . . . . analog output **BH CONV**
signal level . . . . . -8 to 8V peak

Pin 3 . . . . . analog output **GV CONV**
signal level . . . . . -8 to 8V peak

Pin 4 . . . . . analog output **GH CONV**
signal level . . . . . -8 to 8V peak

Pin 5 . . . . . analog output **RV CONV**
signal level . . . . . -8 to 8V peak

Pin 6 . . . . . analog output **RH CONV**
signal level . . . . . -8 to 8V peak

Pin 7 . . . . . analog input **FBK V SIZE**
signal level . . . . . 2 to 3VDC

Pin 8 . . . . . analog input **H SENSE G**
NOTE: see Power Deflection module

Pin 9 . . . . . digital input **VFB**
signal . . . . . 5V square wave

Pin 10 . . . . . digital input **HFB**
signal . . . . . 12V square wave

Pin 11 . . . . . digital input $\overline{\textbf{WR}}$
write signal . . . . . TTL

Pin 12 . . . . . digital input $\overline{\textbf{RD}}$
read signal . . . . . TTL

Pin 13 . . . . . digital input **SEL0**
input/output select 0 . . . . . TTL

Pin 14 . . . . . digital output **HPLLCLK**
256 x HFB square wave
signal . . . . . 5V ±10% square wave
load . . . . . 220 pF
rise time . . . . . 10.2 ns

Pin 15 . . . . . digital output **VPLLCLK**
256 x VFB
signal . . . . . 5V ±10% square wave

Pin 16 . . . . . digital output **HRESET**
signal . . . . . 5V ±10% square wave
pulse width . . . . . 2 to 5 µs ±10%

Pin 17 . . . . . digital output **VRESET**
signal . . . . . 5V square wave
pulse width . . . . . 300 µs ±10%

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