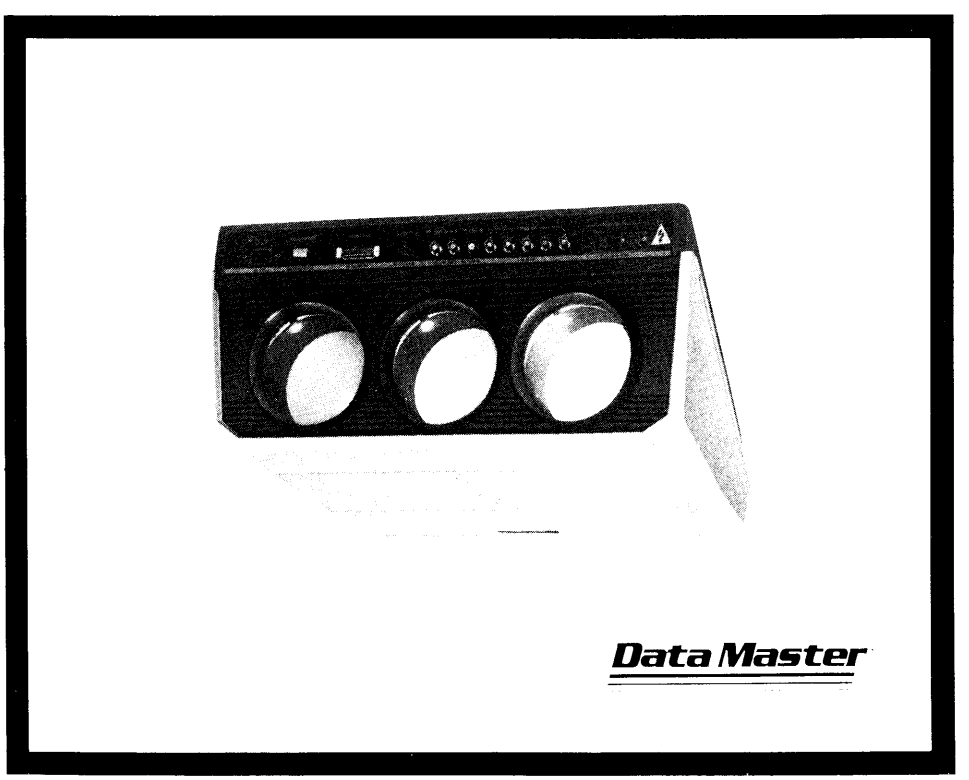
ORDER NO. VED88090091G1

Technical Guide

Vol. 1
chassis No. Q10

Color Video/Data Projector

Model No. PT-105



Panasonic

Video Equipment Division
Matsushita Electric industrial Co., Ltd.

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⚠ WARNING

This service literature is designed for experienced repair technicians only and is not designed for use by the general public. It does not contain warnings or cautions to advise non-technical individuals of potential dangers in attempting to service a product. Products powered by electricity should be serviced or repaired only by experienced professional technicians. Any attempt to service or repair the product or products dealt with in this service literature by anyone else could result in serious injury or death.

OVERALL BLOCK DIAGRAM

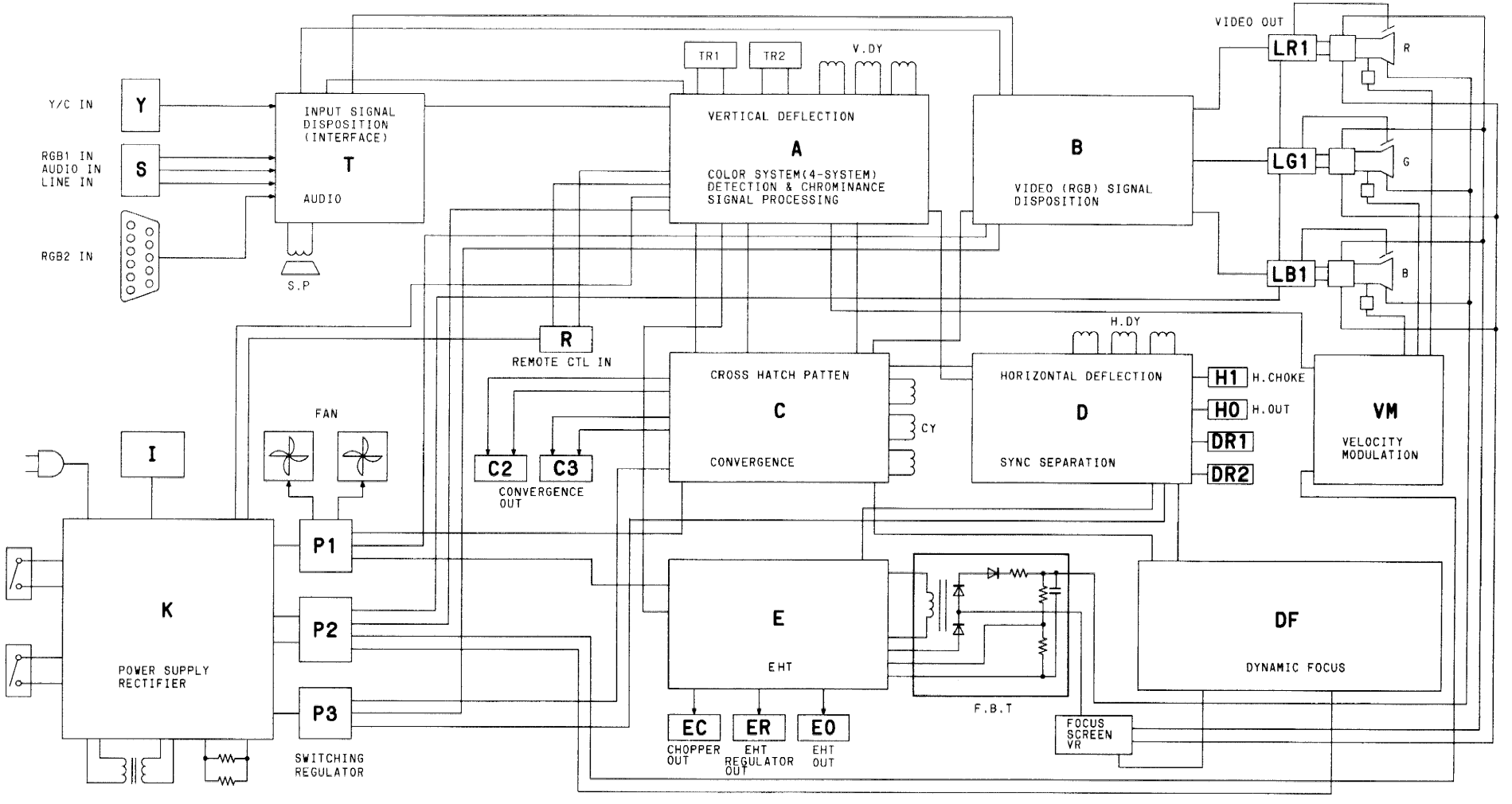


Fig. 1

I. OPTICAL SYSTEM AND CHASSIS DESIGN

1. PT-105 Chassis Layout Diagram

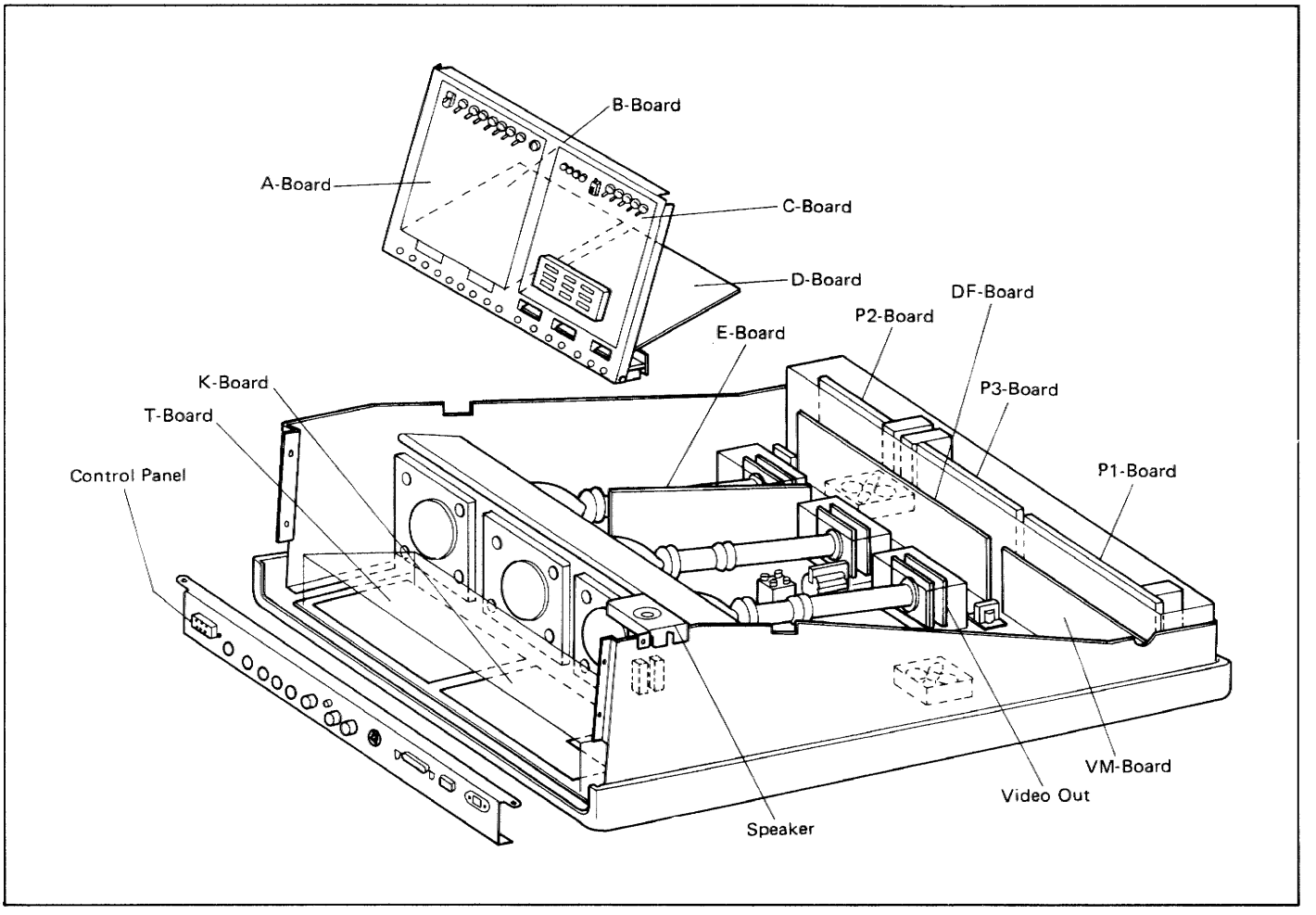


Fig. 2

2. Features of Chassis Design

(1) New optical system incorporating optical coupling technology.

Silicon gel is sealed in at the coupling of the CRT and lens assembly to eliminate a layer of air that would otherwise be created between the CRT and lens assembly, thereby significantly reducing the reflection of unnecessary light. The result of this measure is to achieve a 2-fold increase in contrast ratio compared to conventional designs. (Refractive indexes of silicon gel and CRT glass are nearly equal.)

(2) Use of chromatic aberration correction hybrid lens assembly.

The lens assembly consists of three glass lenses and two plastic lenses. The three glass lenses provide correction of chromatic aberration on blue color, thereby enabling increased clarity.

(Glass lenses can be made to have almost identical refractive index. This is practically impossible for plastic lenses because of inherent characteristics of the material.)

Configuration of lens assembly

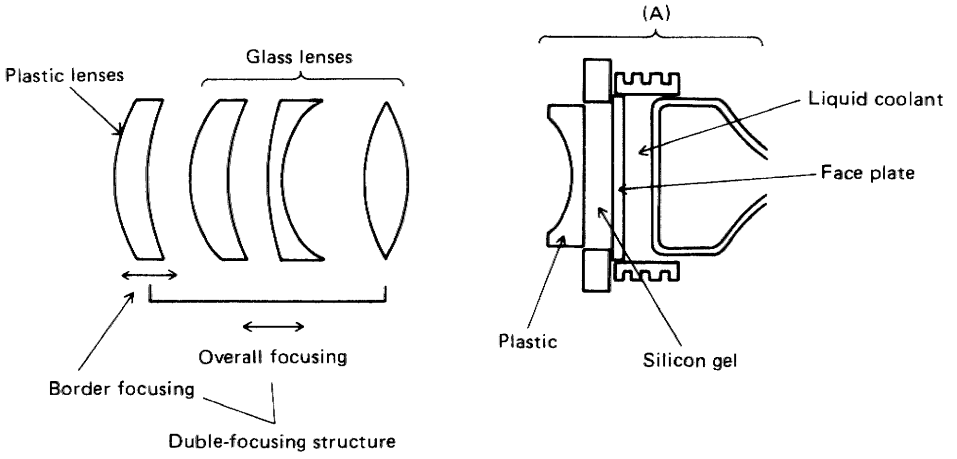


Fig. 3

(3) The lens assembly is designed (and guaranteed) so that the same unit can be used for 60 ~ 120 inch projection sizes (except for (A) in above diagram).

(4) High-density component packaging techniques are used to achieve compact chassis design.

- Double stacking of printed circuit boards (PCB) and use of standing type of PCBs.

(5) Improved serviceability

① 2-position open/close mechanism for A-, B-, C- and D-board.

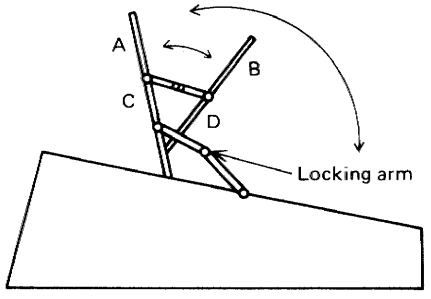
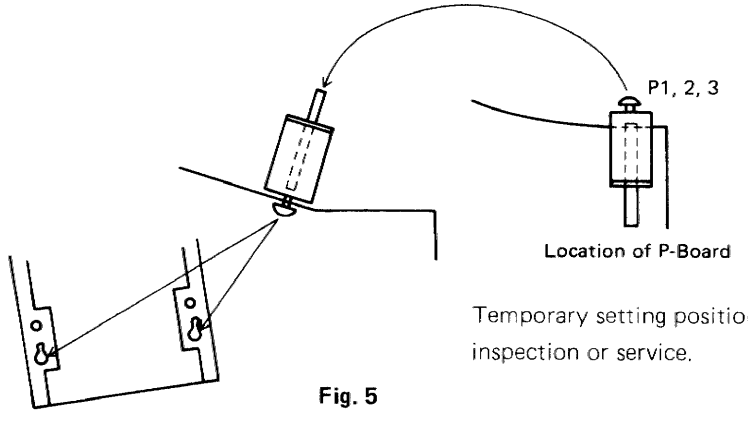


Fig. 4

Use of 2-position open/close mechanism as shown at left which enables the inspection and servicing from both sides of the PCB.

Note: The locking arm must be set straight.

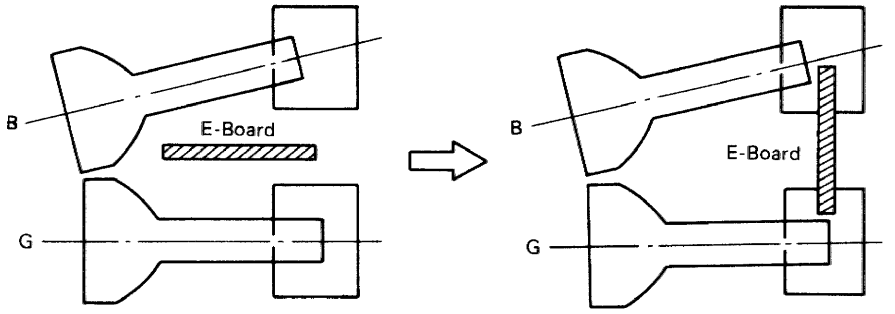
② Temporary setting mechanism on P-board for inspection and servicing.



Temporary setting position of P-board for inspection or service.

Fig. 5

③ Temporary setting mechanism on E-board for inspection or service.



Temporary setting position of P-board for inspection or service.

Fig. 6

④ Ease of optical block (CRT and lens assembly) replacement.

- The optical block is designed in such a way that it can be replaced by working from one direction only as shown below.

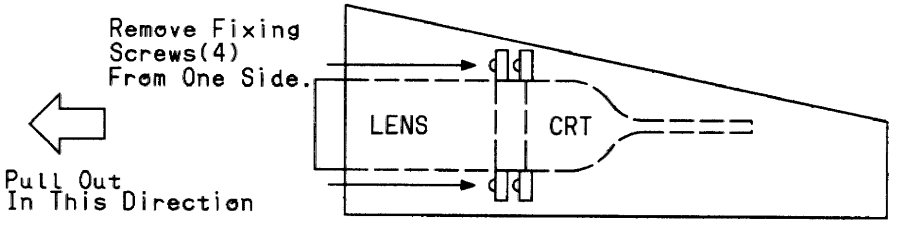


Fig. 7

Note: Screws on top and bottom need not be removed.

(6) Variable projection size

There are two types of PT-105, each supporting different ranges of projection sizes. The ranges and method of projection size variations are as shown below:

	72 INCH TYPE			120 INCH TYPE		
SUPPORTED RANGE (INCHES)	60"~79"			80"~120"		
* SET UP ANGLE (3-POSITION) MARKING	60	70	79	80	100	120
* INCH SIZE RANGE FOR EACH SET UP ANGLE	60"~64"	65"~74"	75"~79"	80"~89"	90"~109"	110"~120"

* set up angles are marked as 60, 70 and 79 or 80, 100 and 120 on the CRT holding stay.

(7) Illumination on the user control and dynamic convergence adjustment controls.
To enable adjustment of the user control and dynamic convergence adjustment controls, illumination is provided. When opening the door illumination switching ON.

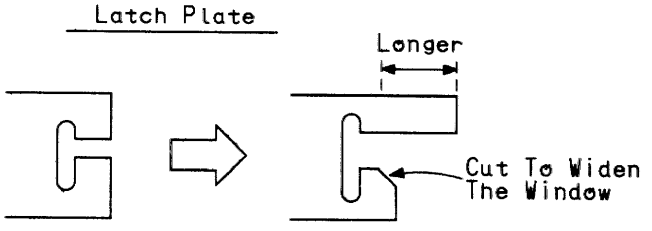


Fig. 8

(8) Display sheet for convergence adjustment guidance.
Pictorial guidance is provided on a sheet that is placed on the dynamic convergence adjustment control block.

(9) Improved ceiling mounting
For easier ceiling mounting, the following parts have been redesigned (from PT-101, Series).

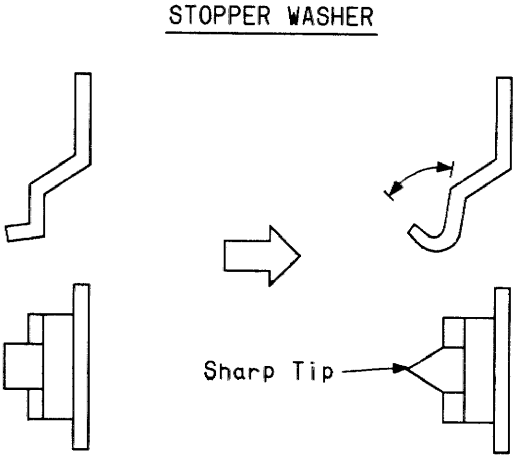


Fig. 9

II. SIGNAL CIRCUITS

1. Input Signal Types

(1) S-VIDEO input ..... DIN 4P (Y signal 1Vp-p C signal 0.285Vp-p)

(2) LINE input ..... BNC 1 ± 0.3Vp-p
* LINE output ..... BNC
(75Ω termination resistor ON/OFF switching function is built-in within BNC, and 75Ω is opened circuit when BNC is inserted ——→ Auto-termination)

(3) RGB1 input . . . . .BNC
(analog)
(Color signal: 0.7Vp-p, positive polarity; SYNC signal: 0.3 ~ 4.0 Vp-p, negative polarity)

Input signal composition

① R, G, B, (Color) H, V (SYNC)

② R, G, B, (Color) H/V (SYNC)

Notes:

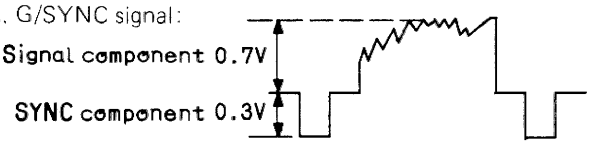
A. Composite video signal can also be inputed to the H/V input terminal.

B. 75Ω termination

③ R, G/SYNC, B

Notes:

A. G/SYNC signal:



B. The G/SYNC mode determination is made by an internal discrimination circuit, specifically by detecting the presence or absence of the SYNC signal in the input to the H. H/V terminal.
(Note that G/SYNC will not occur if there is an input signal to the H. H/V input terminal.)

(4) RGB2 input . . . . .D sub 9 pin
(TTL)
Color switch
8 colors ——→ R, G, B, H, V
16 colors ——→ R, G, B, I, H, V
64 colors ——→ R, G, B, R', G', B', H, V
(Regardless of the input SYNC signal's polarity [i.e., positive or negative], the set automatically determines the polarity and enable input.)
AUTO ——→ Automatic determination of the 16-color color graphic adapter (CGA) or the 64-color enhanced graphic adapter (EGA).

* **Automatic determination of 16-colors or 64-colors**

As shown below, CGA and EGA have opposite V. SYNC polarities, and this difference is used for color type determination.

CGA and EGA output modes		
CGA	H. SYNC	Positive polarity
	V. SYNC	Positive polarity
EGA	H. SYNC	Positive polarity
	V. SYNC	Negative polarity

Note: In the 16-color/CGA mode, display color will be brown (for IBM specification; yellow in general cases) when input conditions are R=1, G=1, I=0, and B=0. To change to yellow display, (1) connect the I signal from personal computer (PC) to D sub 9 pin's ②/R', ⑥/G' and ⑦/B' in parallel and (2) set the color switch to the 64-color position.

2. Input Signal Processing (Interface) Circuit (T-Board)

(1) Block Diagram

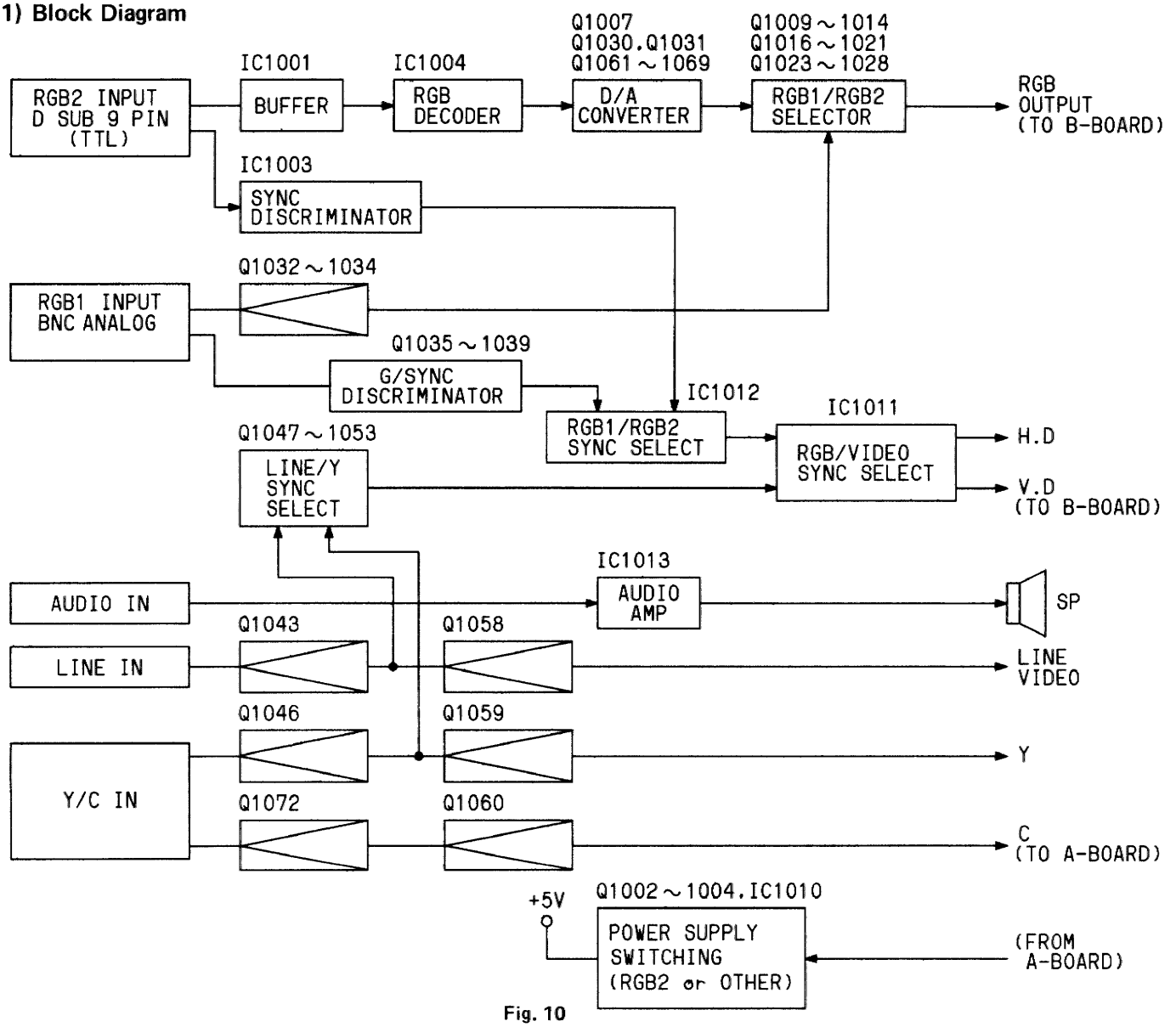


Fig. 10

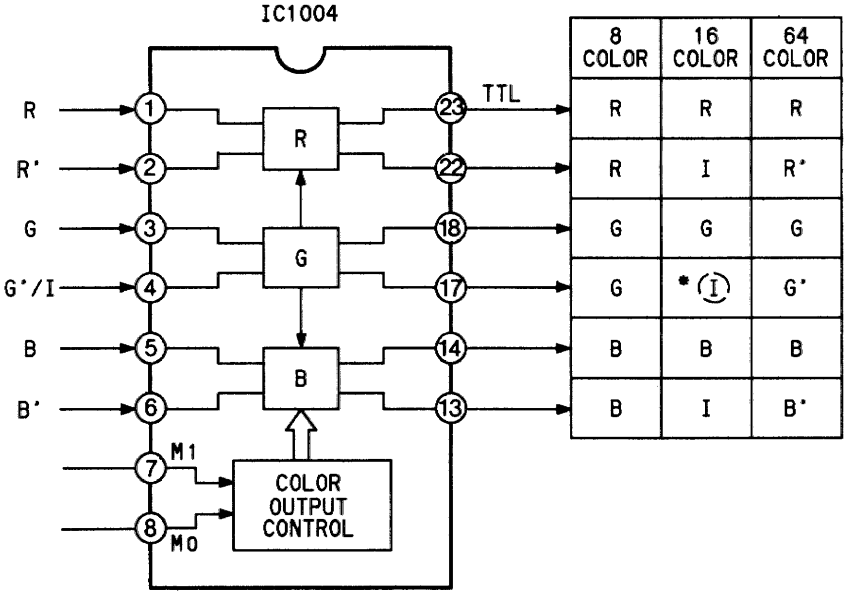
(2) RGB decoder (supports RGB2 input)

A. Function

IC1004 is a logic circuit, and it generates for each input signal 2 bit level signal (H or L) output for each color. The following summarizes the relations between the input and output signals:

Note: The output marked asterisk (*) is L level when R=1, G=1, I=0 and B=0.

Which ever color output will be determined by the control levels (H or L) that are inputed to pins ⑦ and ⑧ on IC1004. The following table summarizes the results:



8 COLOR	16 COLOR	64 COLOR
R	R	R
R	I	R'
G	G	G
G	*(I)	G'
B	B	B
B	I	B'

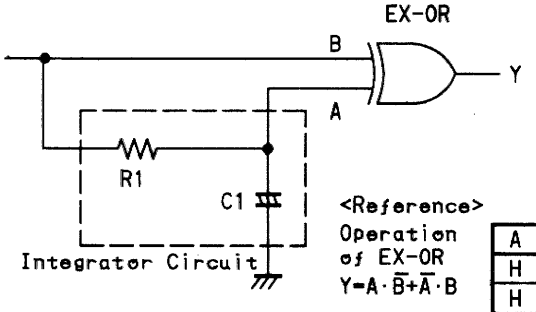
Fig. 11

	8 COLOR	16 COLOR	64 COLOR
⑦ M1	H	L	L
⑧ M0	L	(L)	(H)

Discrimination between 16 color/CGA and 64 color/EGA is made by the input level (L or H) to pin ⑧.
(Automatic discrimination)

(3) SYNC signal polarity discrimination and conversion circuits

Basic circuitry



<Reference>
Operation of EX-OR
$Y=A\cdot\overline{B}+\overline{A}\cdot B$

A	B	Y
H	H	L
H	L	H
L	H	H
L	L	L

The basic circuitry consists of an EX-OR circuit and an integrator circuit made of R1 and C1, as shown above.

Fig. 12

B. Circuit Operation

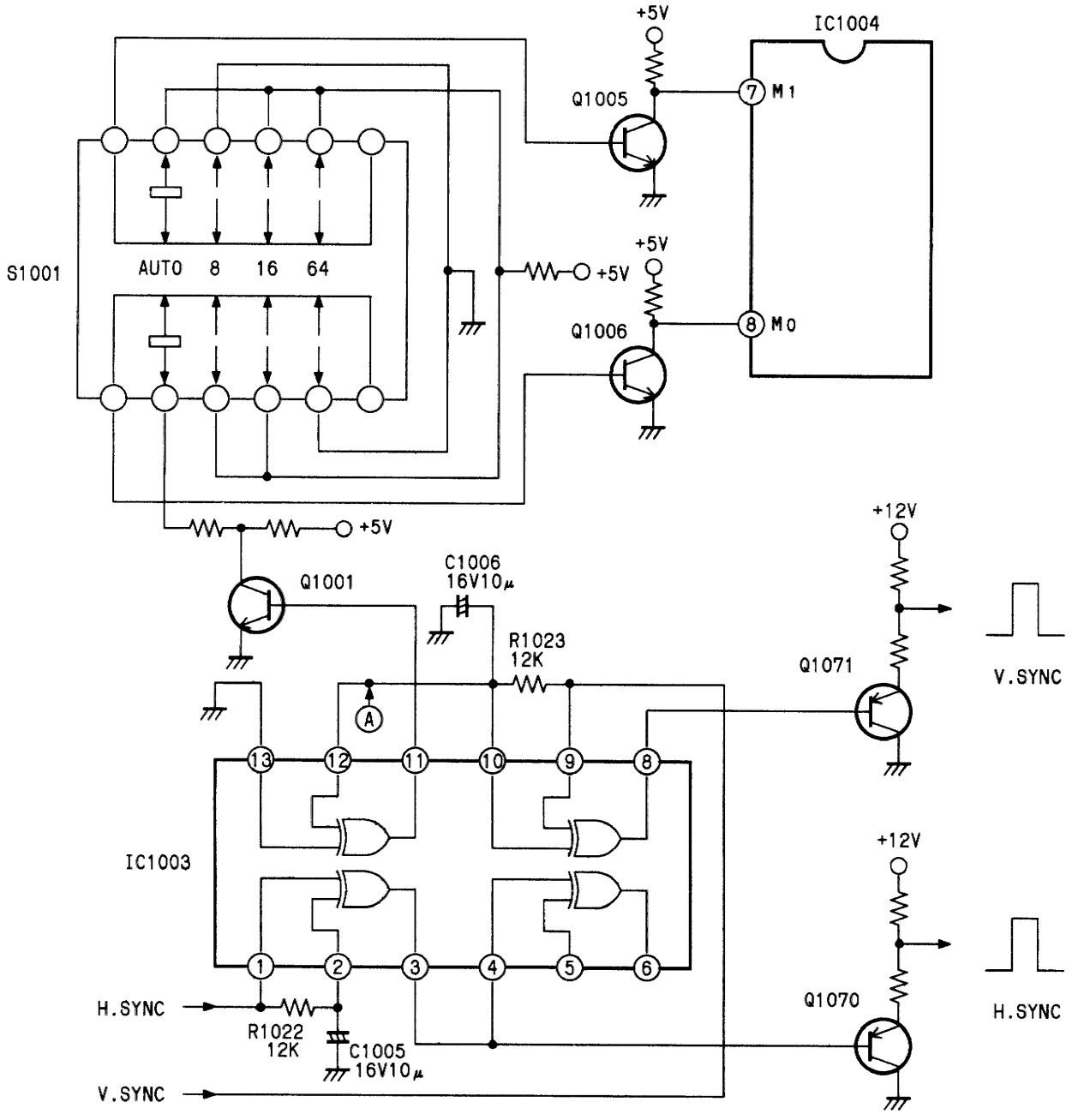


Fig. 13

Input SYNC signal polarity conversion

V. SYNC component of RGB2 input is applied directly to pin ⑨ of IC1003, and V. SYNC that has been integrated by the integration circuit consisting of R1023 and C1006 is inputed to pin ⑩ . The EX-OR operation of the basic circuit described above will cause a positive polarity V. SYNC to be outputed to pin ⑧ (regardless of the polarity of the input V. SYNC).

For example, if a positive polarity V. SYNC is inputed, integration by R1023 and C1006 will cause the input to ⑩ to be nearly L level DC-wise, and the positive polarity V. SYNC that goes to ⑨ is outputed. If, however, a negative polarity V. SYNC is inputed, integration by R1023 and C1006 will cause the input to ⑩ to be nearly H level DC-wise, and the negative polarity V. SYNC input to ⑨ will be inverted and outputed (as positive polarity signal).

H. SYNC polarity conversion works in the same way, and a positive polarity H. SYNC signal is always outputed.

SYNC signal polarity discrimination

(Auto 16 color/CGA and 64 color/EGA switching)

As described above, IC1003's ⑫ is H or L level depending on the polarity of V. SYNC input. This difference is used to control the RGB decoder IC1004 and automatically switch between 16 and 64 color modes.

DIFFERENCES BETWEEN SYNCS FOR CGA AND EGA		
PC	H.SYNC	V.SYNC
CGA	⎍	⎍
EGA	⎍	⎍

As shown in the table at left, the difference between the CGA and EGA modes is the polarity of V. SYNC, and mode discrimination can be made by focusing on this difference. (H. SYNC has a positive polarity in both modes, so that it is not used for color mode discrimination.)

⑬ in IC1003 is always grounded and therefore at L level. Thus the output to ⑪ is L or H level depending on the level of the signal at ⑫ . The output level at ⑪ is used to switch Q1001 or Q1006 ON and OFF to switch IC1004's ⑧ M_0 to H or L level.

	PC V SYNC	IC1003 ⑫	Q1001	Q1006	IC1004 ⑧ /M0	IC1004 OPERATION
CGA	⎍	L	OFF	ON	L	16 COLOR
EGA	⎍	H	ON	OFF	H	64 COLOR

(4) D/A Conversion Circuit

A. Function

The D/A conversion circuit converts the color signals (2 bits each) output from IC1004's RGB decoder to analog signals.

B. Circuit Operation

(Only the portion for R signal is shown below. The circuitry for G and B are basically the same.)

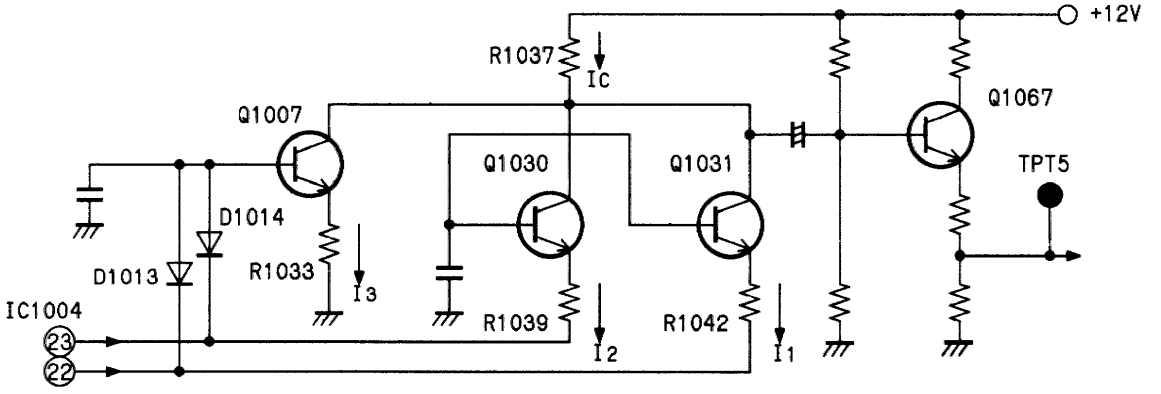


Fig. 14

The level (H or L) of the output from IC1004's RGB decoder is used to control the current that flow through Q1007, Q1030 and Q1031 (I_3, I_2 and I_1, respectively) which results in control of the total current Ic. This enables the control of the current flow at four levels, which in turn enables extraction at TPT5 of four levels of voltage as shown below:

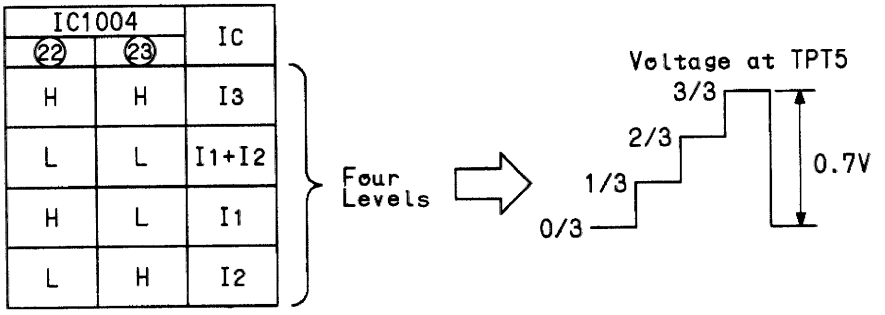


Fig. 15

(5) RGB1/RGB2 Signal Select Circuit

A. Function

(Only the portion for R signal is shown below. The circuitry for G and B are basically the same.)

The purpose of this circuit is to select RGB1 or RGB2 mode signal.

B. Circuit Operation

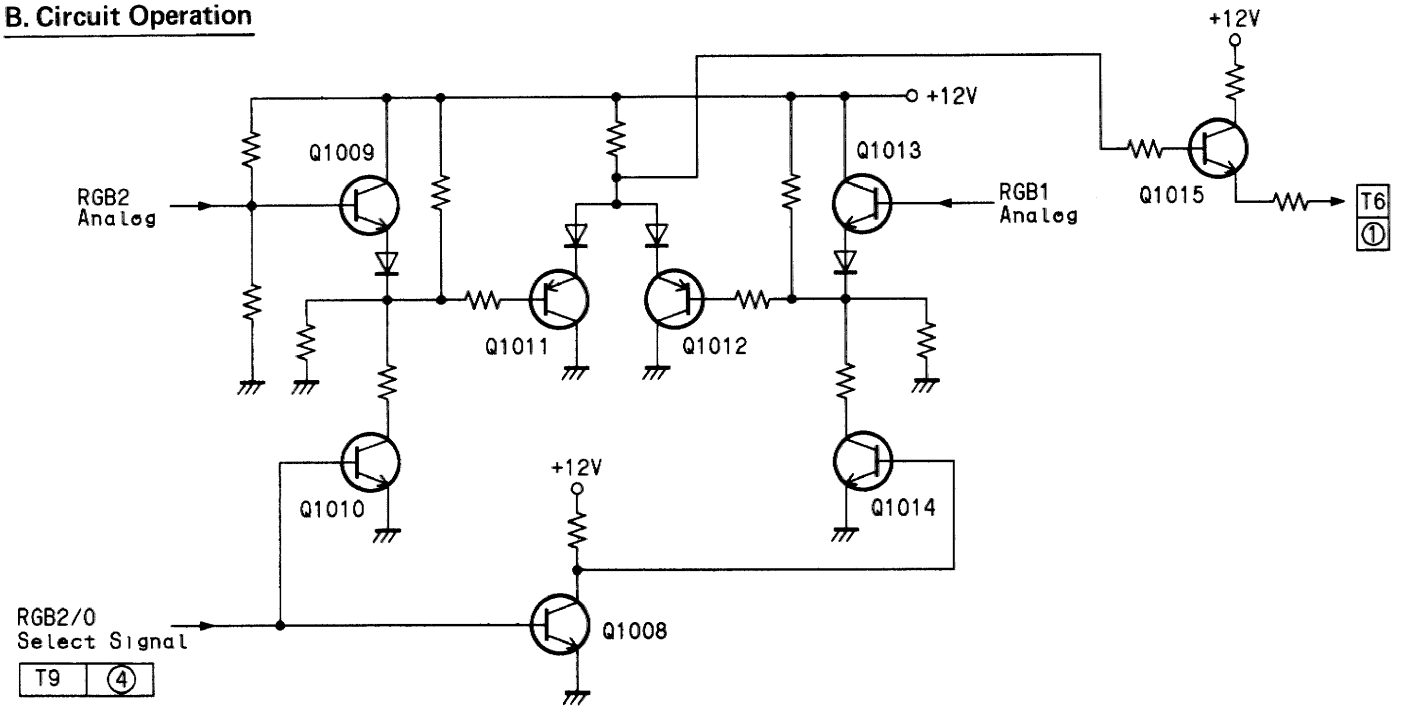


Fig. 16

When the RGB2 input mode is selected, H level is output from T9 ④. This H level signal switches Q1010 ON or Q1014 OFF, causing RGB2 (analog) signals to go via Q1009, Q1001 and Q1015. At this time, RGB1 signals are not outputed because Q1014 is OFF.

(6) G/SYNC Mode Discrimination Circuit

A. Function

Q1035 ~ Q1038 are used to determine whether or not there is a signal input to H. H/V IN terminal and, therefore, whether or not the system is in the G/SYNC mode. Basically, there are three input terminals (R, G/SYNC and B) in the G/SYNC mode. The G/SYNC mode will not be in effect when there is SYNC signal input to the H. H/V terminal. Thus, only the above mentioned three terminals are used for input in the G/SYNC mode.

B. Circuit Operation

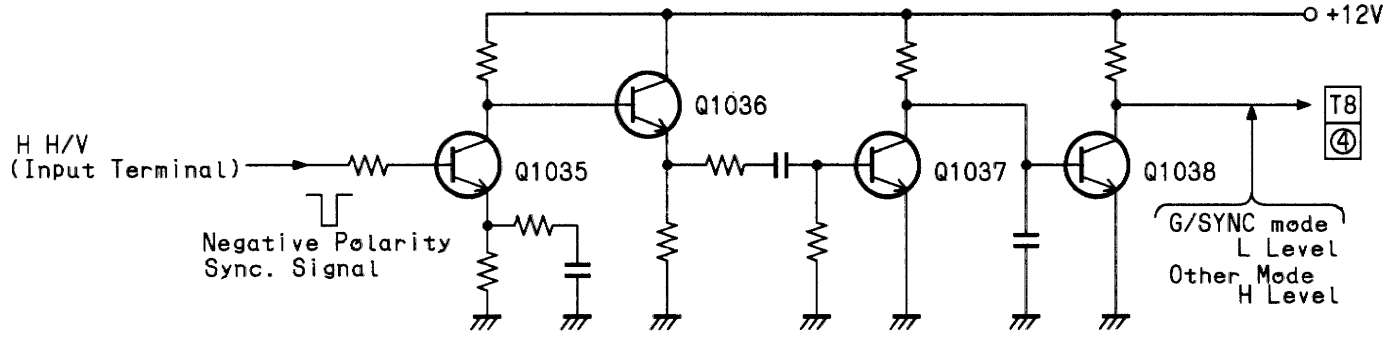


Fig. 17

(7) LINE/Y SYNC Select Circuit

A. Function

Q1047 ~ Q1052 are used to select SYNC between VIDEO SYNC portion of the LINE signal and the Y signal.

B. Circuit Operation

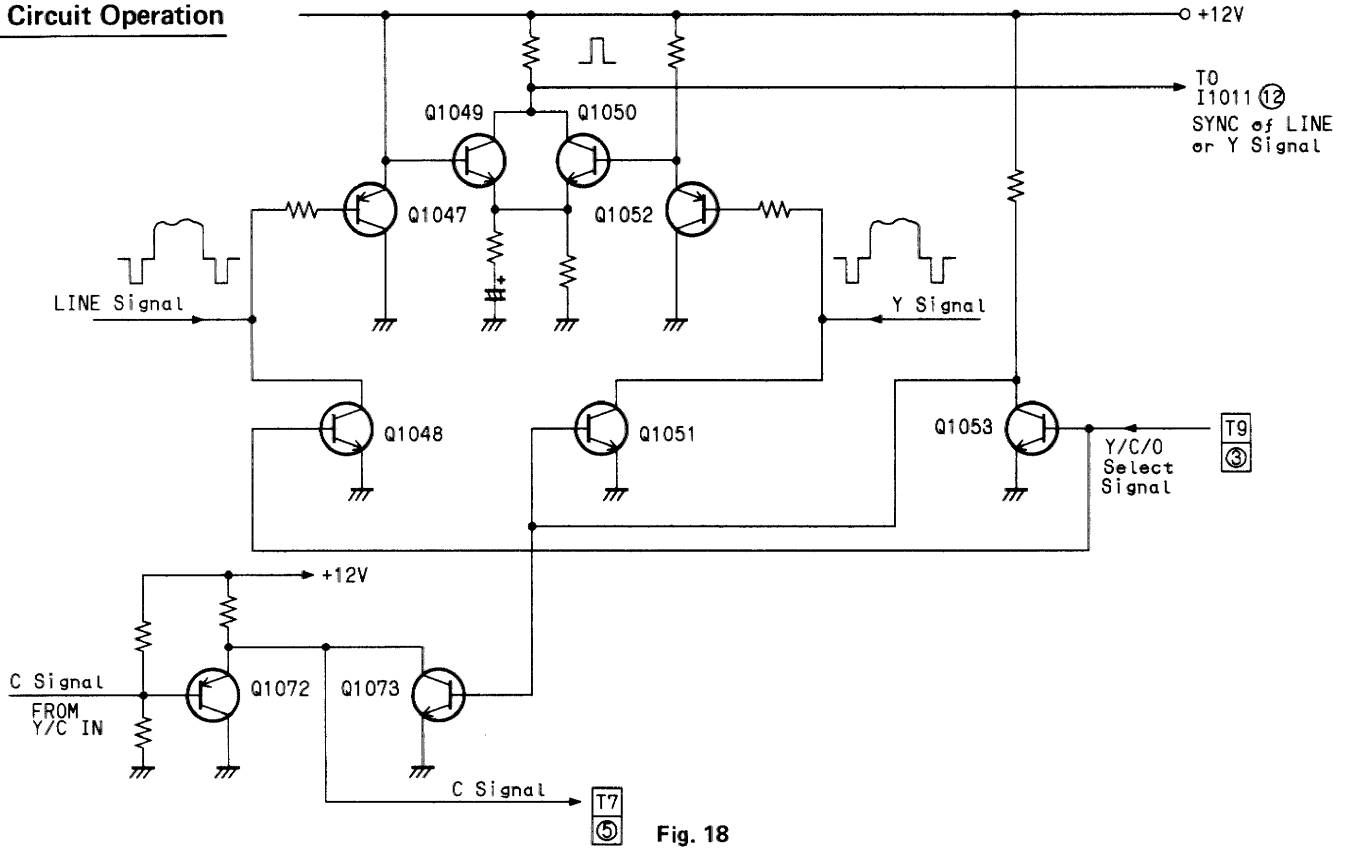


Fig. 18

When S-VIDEO is selected by the input selector switch, H level select signal goes to Q1053's base, which switches Q1053 ON and Q1051 OFF and causes the Y signal that was inputed to Q1052's base to be outputed via Q1050 to IC1011's ⑫ . At this time, Q1048 becomes ON and the LINE signal input to Q1047's base is dropped to ground.

(8) RGB1/RGB2 SYNC select circuit and RGB/ VIDEO SYNC Select Circuit

A. Function

The circuitry centered around IC1012 selects either RGB1 SYNC or RGB2 SYNC, and the circuitry centered around IC1011 selects either RGB SYNC or VIDEO SYNC.

B. Circuit Operation

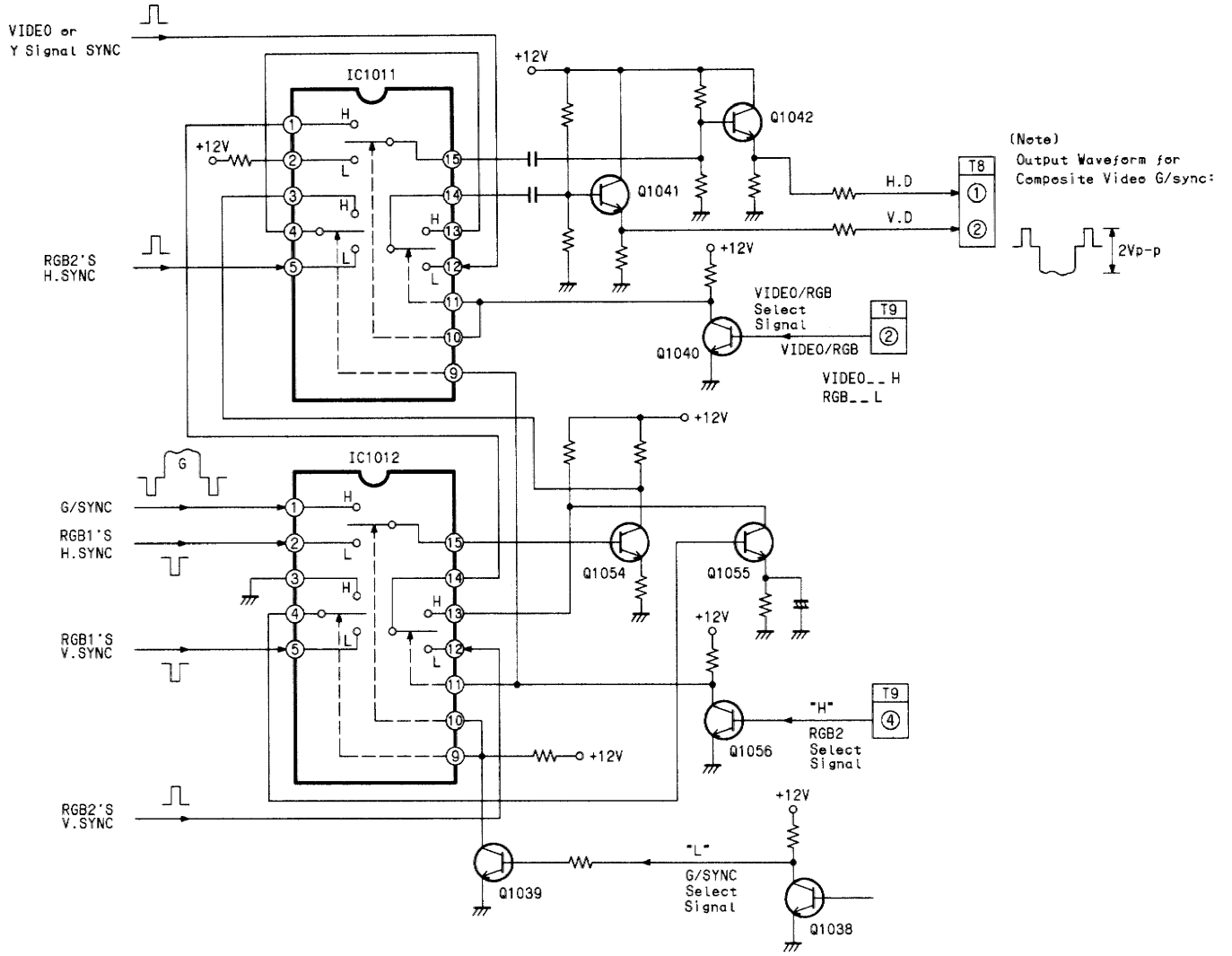


Fig. 19

As described above, IC1012 selects RGB1 SYNC or RGB2 SYNC. It has another function, which is to select RGB1 SYNC or G/SYNC.

If RGB2 mode selection is made, H level signal from T9 ④ is added as Q1056 ON control signal. This switches Q1056 ON and causes the signal at IC1012's ⑪ to be at Low level, resulting in an output of RGB2 V. SYNC from ⑭. RGB2 V. SYNC output from IC1012's ⑭ is inputed to IC1011's ①. At this time, the control signal from T9 ② is at Low level and Q1040 is OFF, and therefore IC1011's ⑪ is at H level and RGB2 V. SYNC input from ① is output to ⑮. RGB2 H. SYNC being inputed from IC1011's ⑤ is outputed from ④ and inputed to ⑬ because IC1011's ⑨ is at L level, and then outputed from ⑭ because ⑪ is at H level. For RGB1 SYNC selection, the operation is opposite of the above. Selection of V. SYNC and H. SYNC for G/SYNC or RGB1 are determined based on Q1038's collector level. For G/SYNC, IC1012's ⑩ is at H level and G/SYNC being input to ① is outputed from ⑮.

Selection between VIDEO and RGB is determined by the control signal from T9 ②. For VIDEO IC1011's ⑪ is at L level and the video signals being inputed to ⑫ is outputed from ⑭.

	Q1056	Q1040	IC1012			IC1012									Q1039	IC1011			IC1011							
	Ⓒ	Ⓒ	⑪	⑩	⑨	①	②	⑮	③	④	⑤	⑭	⑬	⑫	Ⓒ	⑪	⑩	⑨	①	②	⑮	③	④	⑤	⑭	⑬	⑫
RGB1 SYNC	H	H	H	L	L		②	–	⑮	④	–	⑤	⑭	–	⑬	L	H	H	H		①	–	⑮	③	–	④	⑭	–	⑬
RGB2 SYNC	L	H	L	L	L		②	–	⑮	④	–	⑤	⑭	–	⑫	L	H	H	L		①	–	⑮	④	–	⑤	⑭	–	⑬
G/SYNC	H	H	H	H	H		①	–	⑮	③	–	④	⑭	–	⑬	H	H	H	H		①	–	⑮	③	–	④	⑭	–	⑬
VIDEO	H	L	H	L	L		②	–	⑮	④	–	⑤	⑭	–	⑬	L	L	L	H		①	–	⑮	③	–	④	⑭	–	⑬

(9) Audio Circuit

A. Function

The audio circuit is designed around IC1013, and this circuit generates 1.5W speaker output.

3. 4-system Video Signal Processing Circuit (A-Board)

(1) Block Diagram

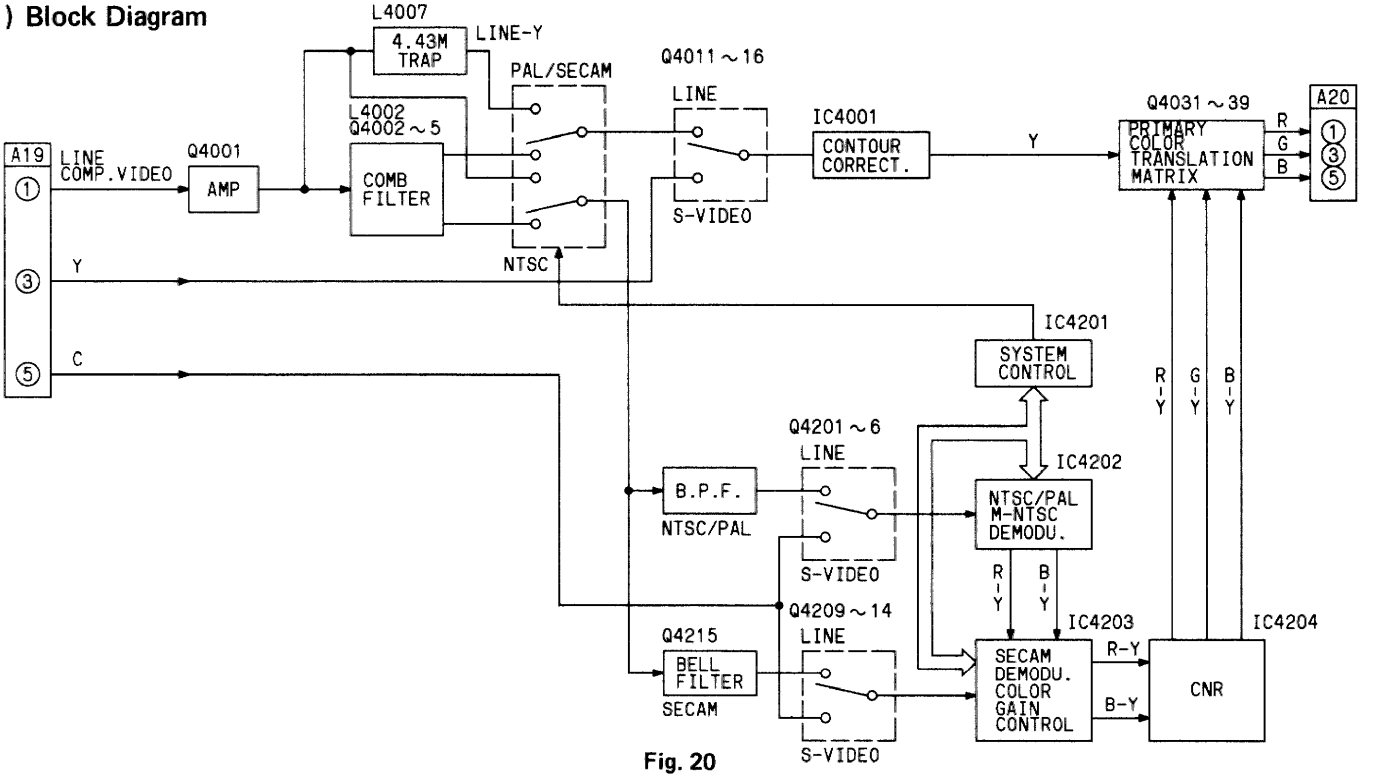


Fig. 20

(2) Comb Filter and Signal Switching Circuits

A. Function

The comb filter circuit separates NTSC composite signal to the chrominance (C) signal portion and the luminance (Y) signal portion. The basic operation of this circuit are identical to the corresponding circuit in the earlier model, and the only difference is that this is now a broad-band filter. Because of the similarity, only the signal switching operation is described.

B. Circuit Operation

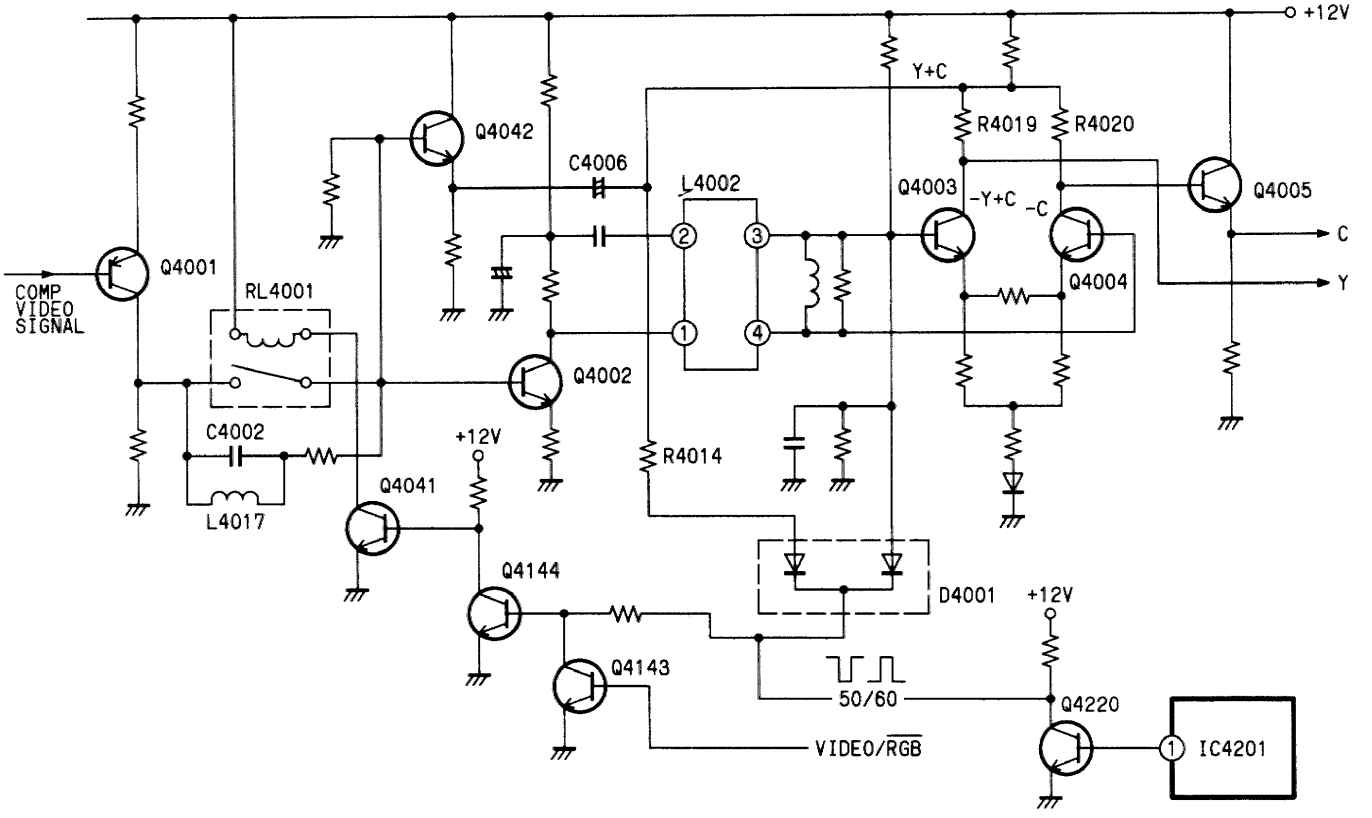


Fig. 21

When NTSC video signal is inputed, L level control signal is outputed from the system control IC4201's ①, which is inverted by Q4220 and added to Q4144's base. This switches Q4144 ON and Q4041 OFF, causing the RL4001 relay circuit to be in the open condition. The composite video signal is outputed from Q4001's emitter to the input of Q4002's base via C4002 and L4017. The function of C4002 and L4017 is to help flatten the frequency characteristics of the signal that has gone through the comb filter circuit. The signal output by the comb filter circuit tends to have a slightly higher frequency characteristics, so that C4002 and L4017 are used to lower the frequency characteristics of the filter circuit input. The NTSC video signal passes through Q4002, Q4042, L4002, Q4003 and Q4004, and its Y signal component is outputed from Q4003's collector and its C signal component is outputed from Q4004's collector. When PAL/SECAM video signal is inputed, the above mentioned relay circuit's RL4001 switches ON and the video signal is added directly (without going through the C4002 and L4017 filter) to Q4042's base. Also in the case of PAL/SECAM, D4001's anode side is at L level and Q4003 and Q4004 are not biased, causing the composite video signal to be outputed via R4019 and R4020.

(3) LINE Input Signal/S-VIDEO Signal Select Circuit

A. Function

The circuit consists of Q4201 ~ Q4206 which selects the C signal component of NTSC/PAL and S-VIDEO signals.

The circuit consisting of Q4011 ~ Q4016 selects the Y signal component of NTSC/PAL/SECAM and S-VIDEO signal.

The circuit consisting of Q4209 ~ Q4214 selects the C signal component of SECAM and S-VIDEO signals.

B. Cricuit Operation

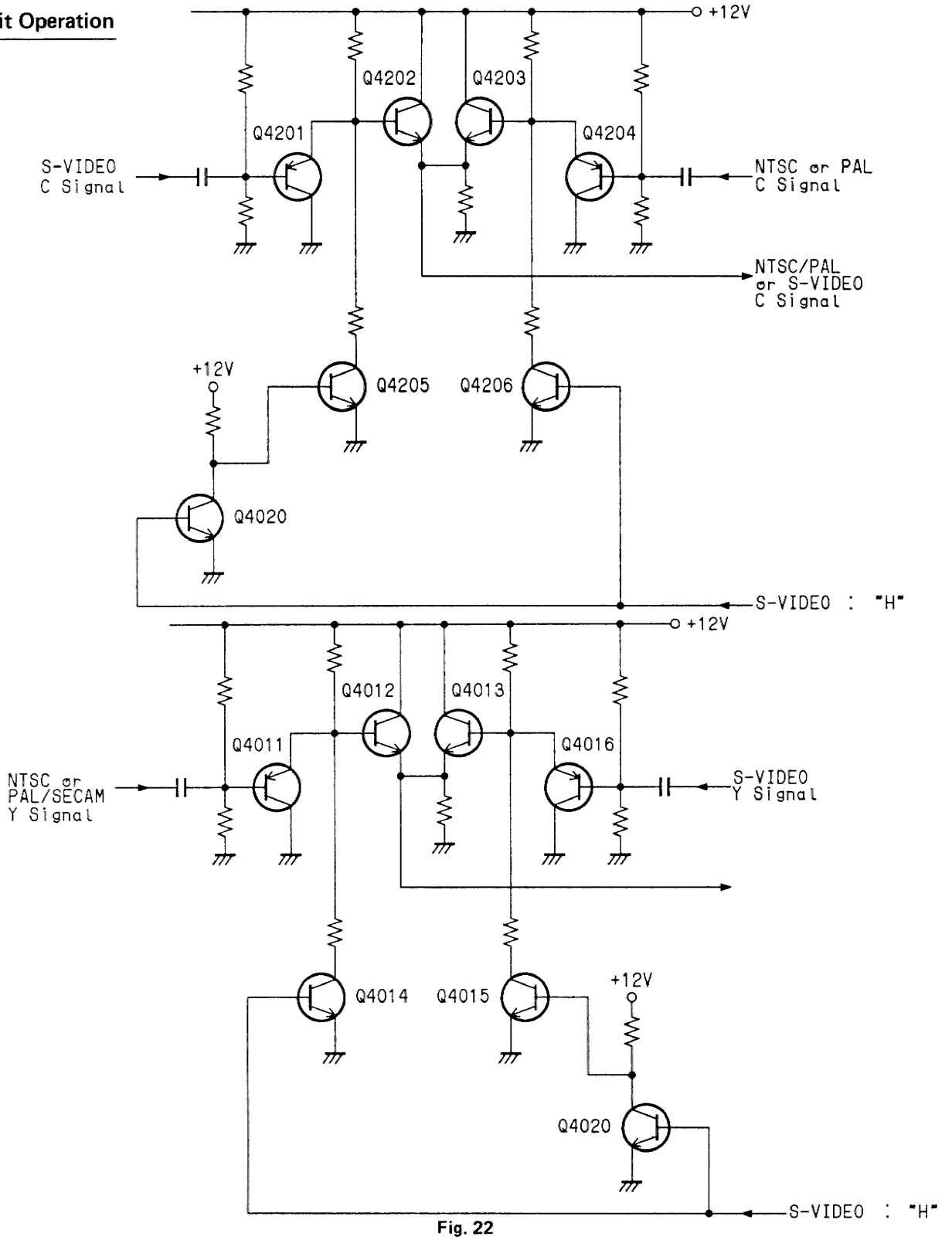


Fig. 22

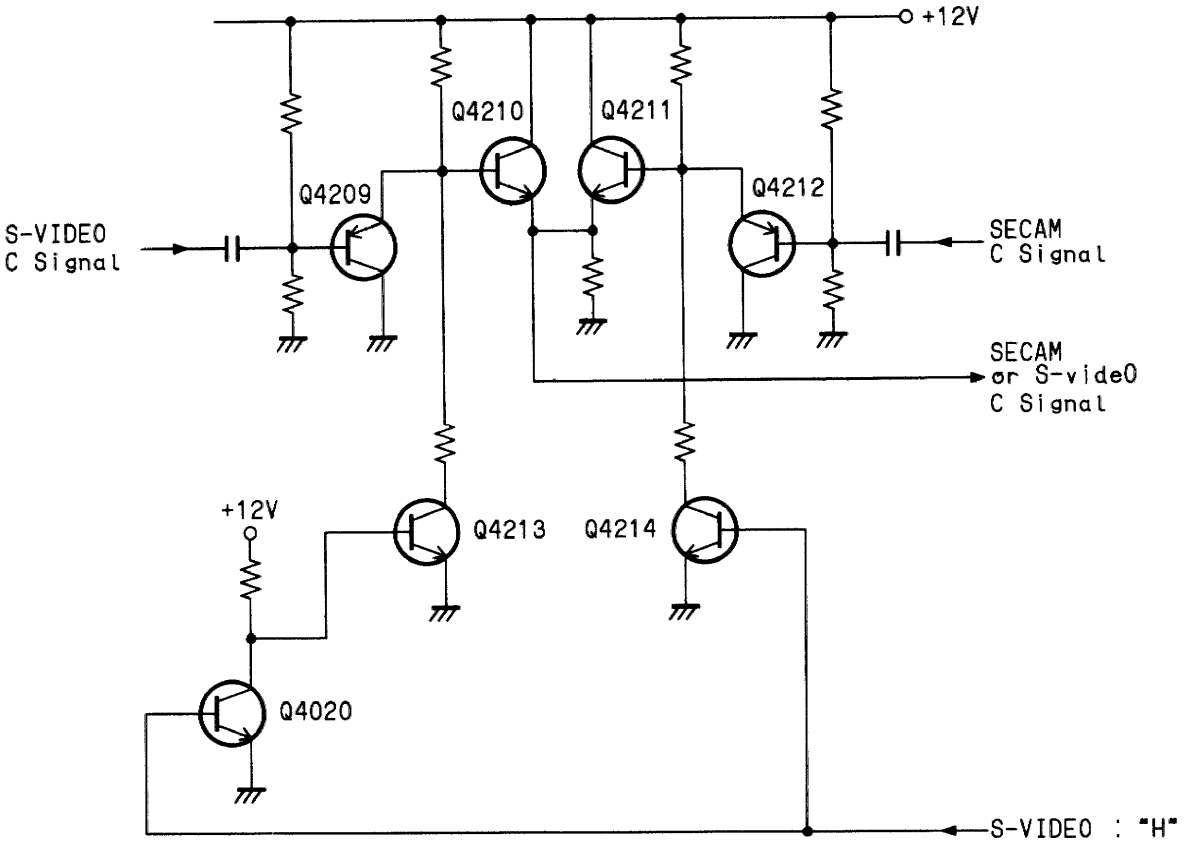


Fig. 23

(4) Operation of Y Signal Delay Circuit (4.43 MHz Trap Circuit)

This circuit causes a delay of 1H on Y signal relative to the chrominance signal in order to make the R-Y and B-Y signals.

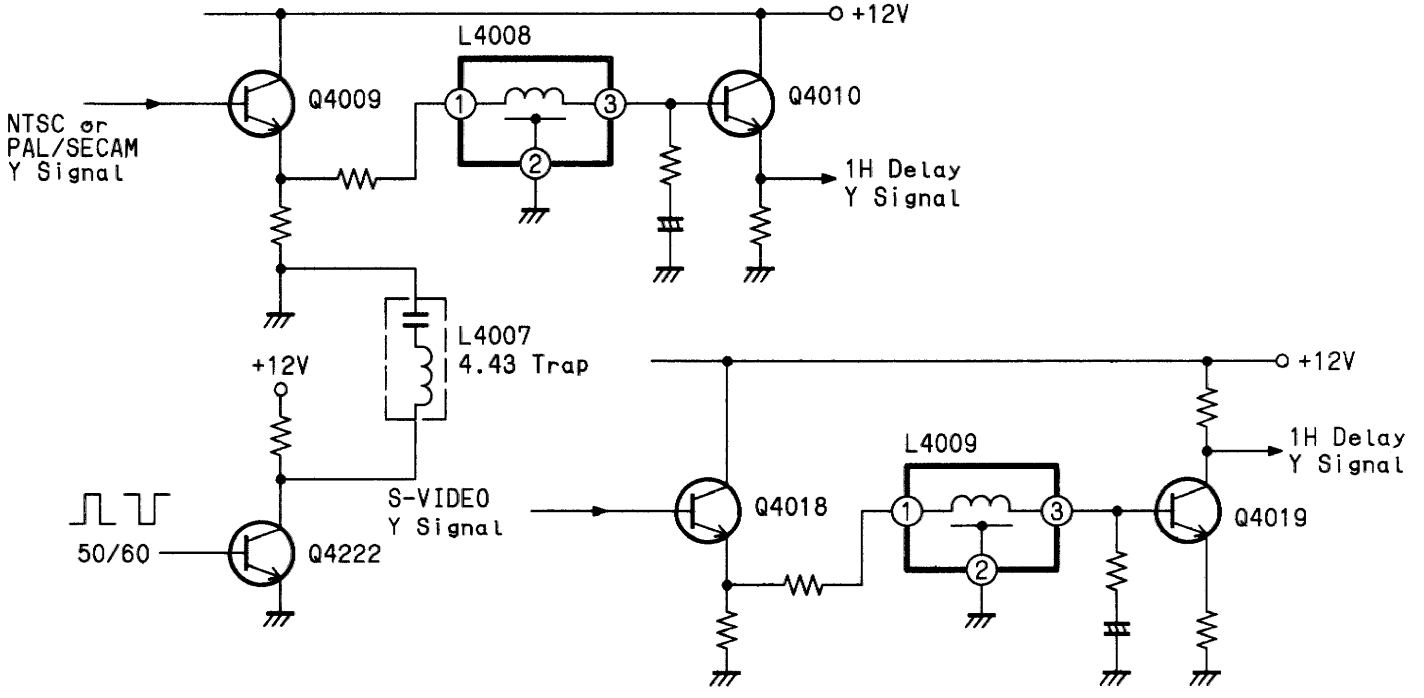


Fig. 24

(5) Contour Correction Circuit

A. Function

In addition to the convertional secondary differentiation type contour correction, the time base compression type contour correction is used. The later type features contour correction without sacrificing the S/N ratio.

Comparison of secondary differentiation and time base compression type contour correction

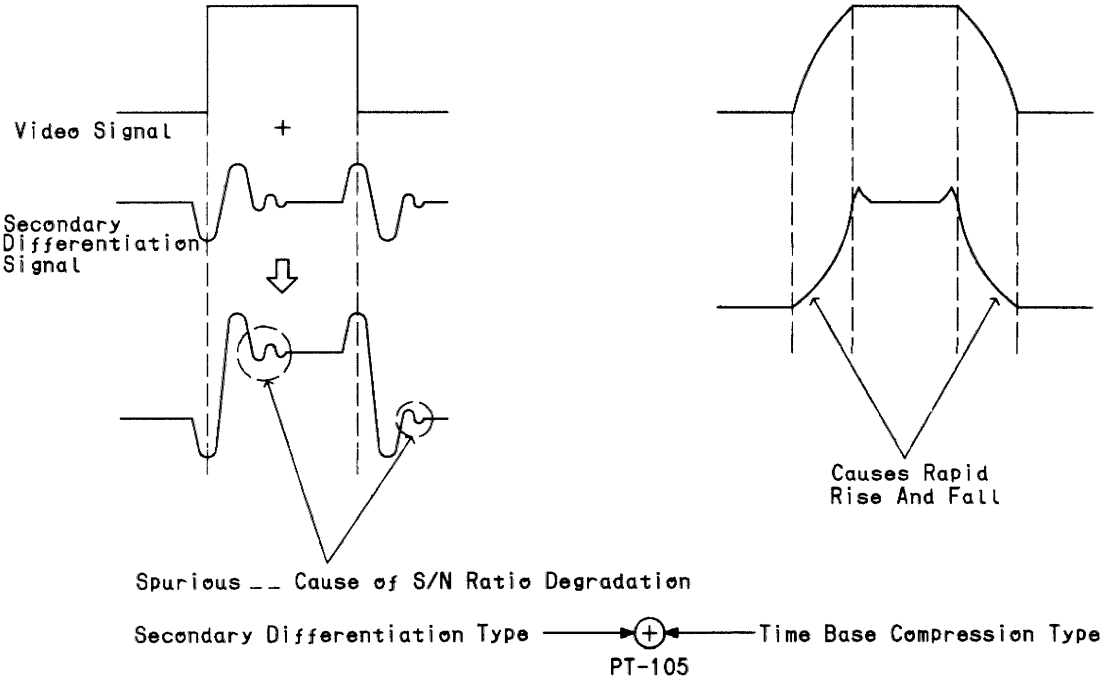


Fig. 25

B. Circuit Operation

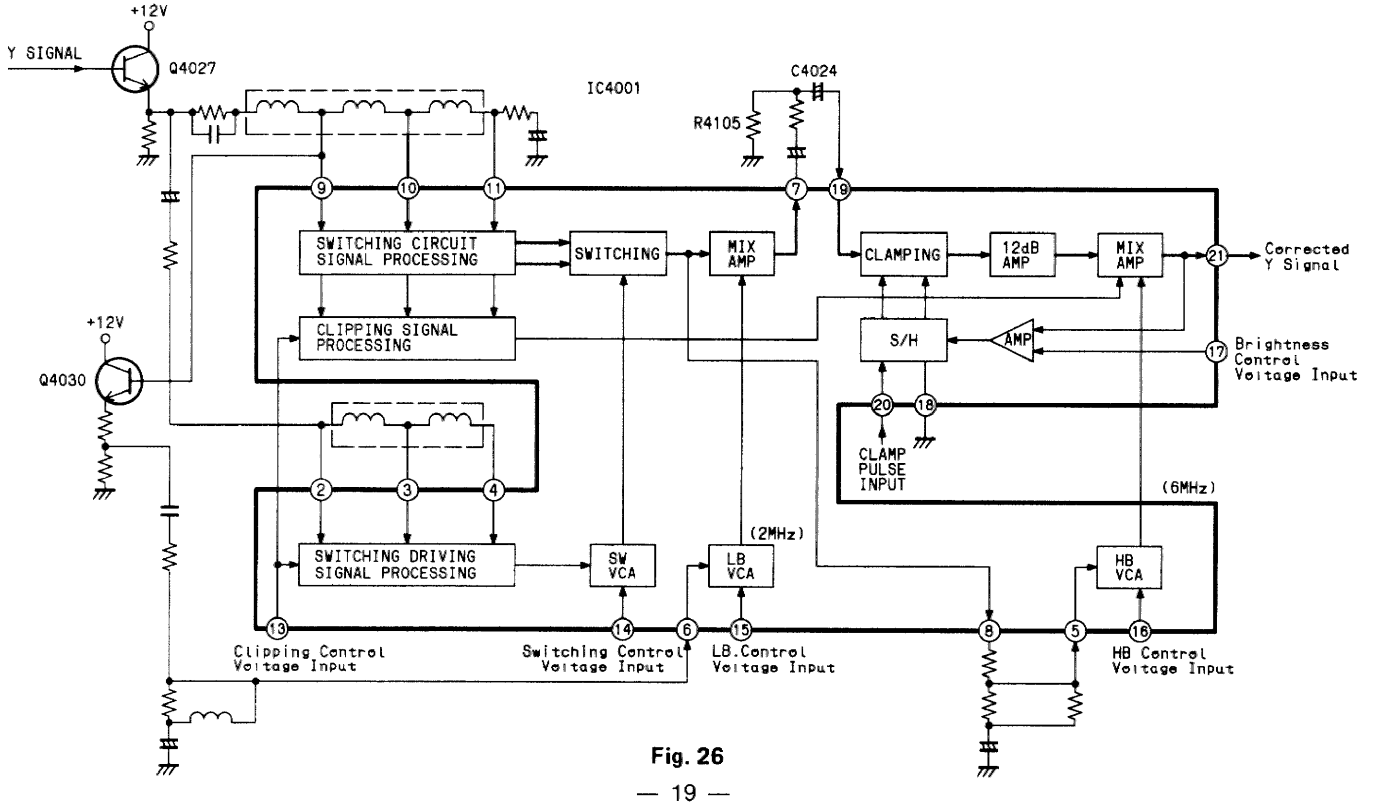


Fig. 26

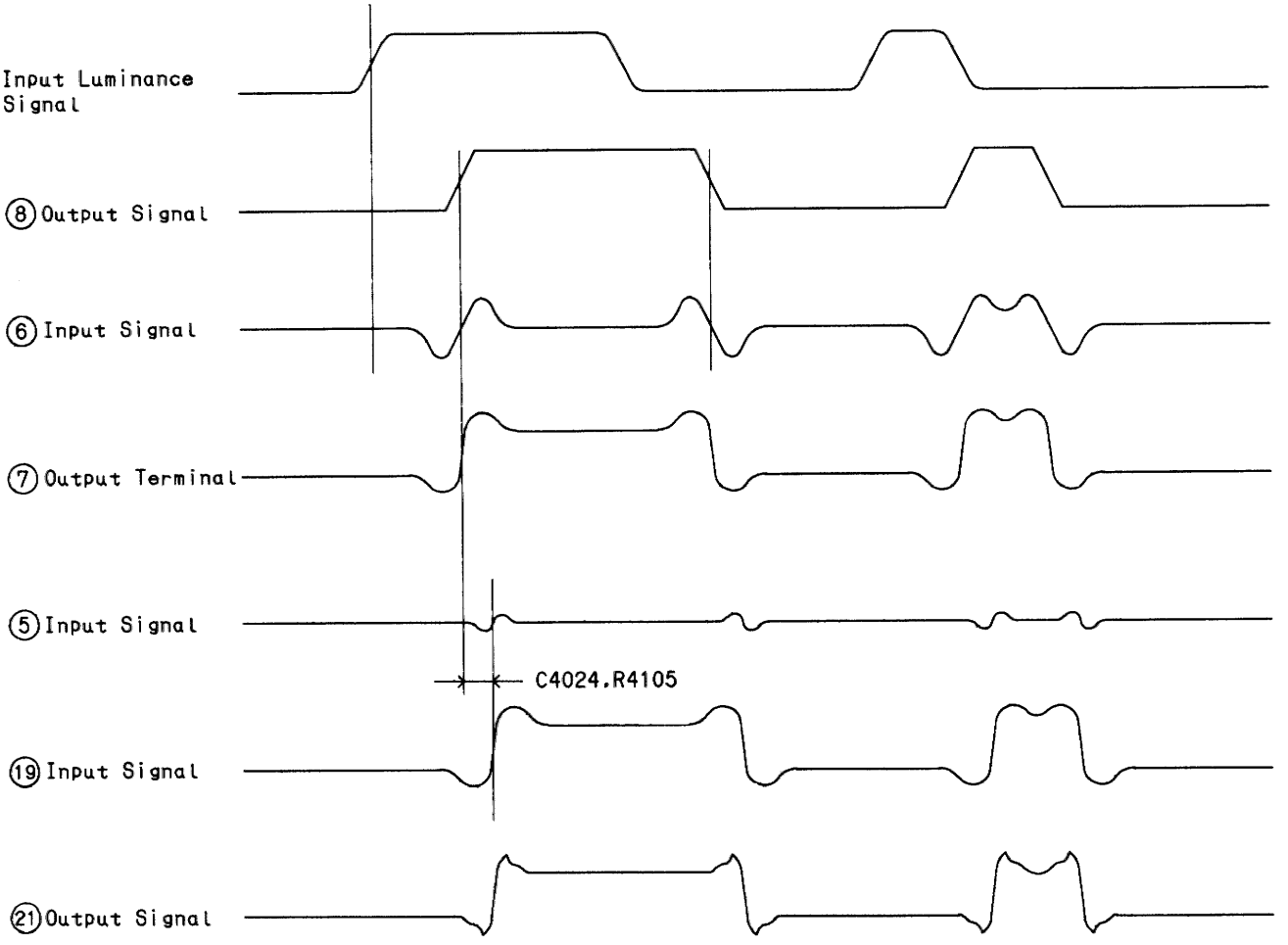


Fig. 27

The contour correction applied output waveform from IC4001's ㉑ has natural, sharp pattern.

(6) Color Noise Reduction (CNR) Circuit

A. Function

This circuit removes the noise from the color signal based on the following principle (for SECAM only):

CNR's operating principle

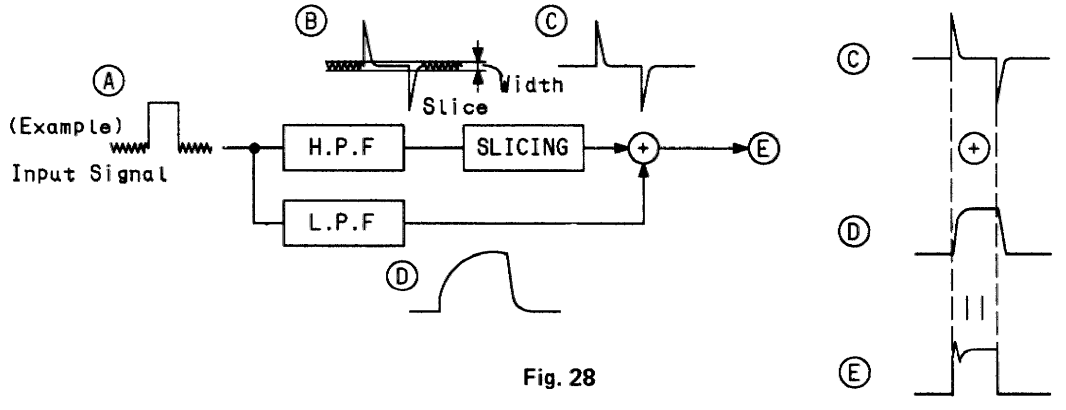


Fig. 28

Ⓑ is the waveform that has been differentiated by H.P.F.
Ⓒ is the (CNR applied) waveform that has been sliced at a certain (noise component) level width.
Ⓓ is the waveform that has been integrated by L.P.F.

B. Circuit Operation

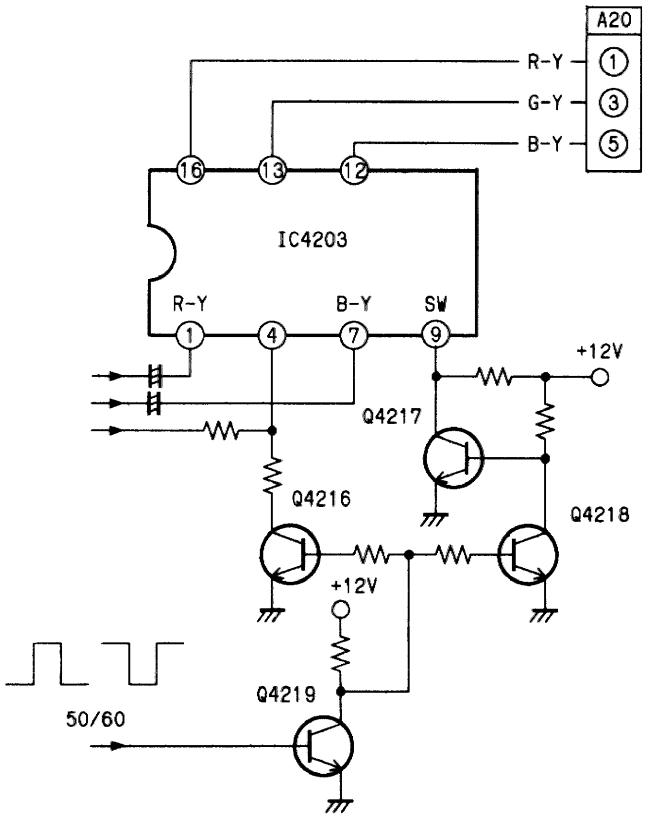


Fig. 29

SECAM signal has 50 Hz frequency so that the H level select signal input to Q4219's base switches Q4219 ON, Q4218 OFF and Q4217 ON which in turn switches IC4203's ⑨ ON causing color signal to pass through the CNR circuit. This results in removal of noise component from the color signal.

4. Video (RGB) Signal Processing Circuit (B-Board)

(1) Block Diagram

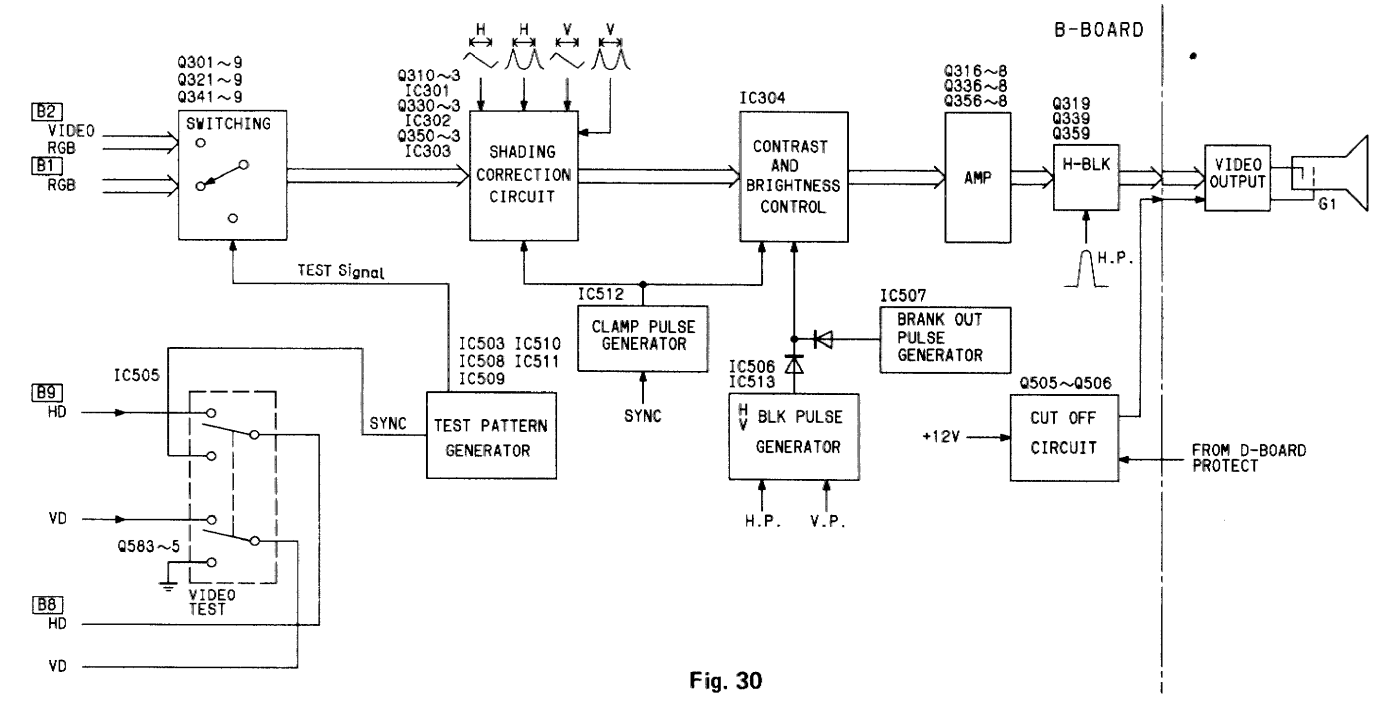


Fig. 30

(2) RvGvBv/RGB/TEST Signal Select Circuit

This circuit switches between three signals (RGB signal from B1 connector, RvGvBv signal from B2 connector and TEST signal generated by the test pattern generating circuit) according to the input mode selection.

Circuit Operation

(Only the portion of circuit for R is shown because it is exactly same for G and B)

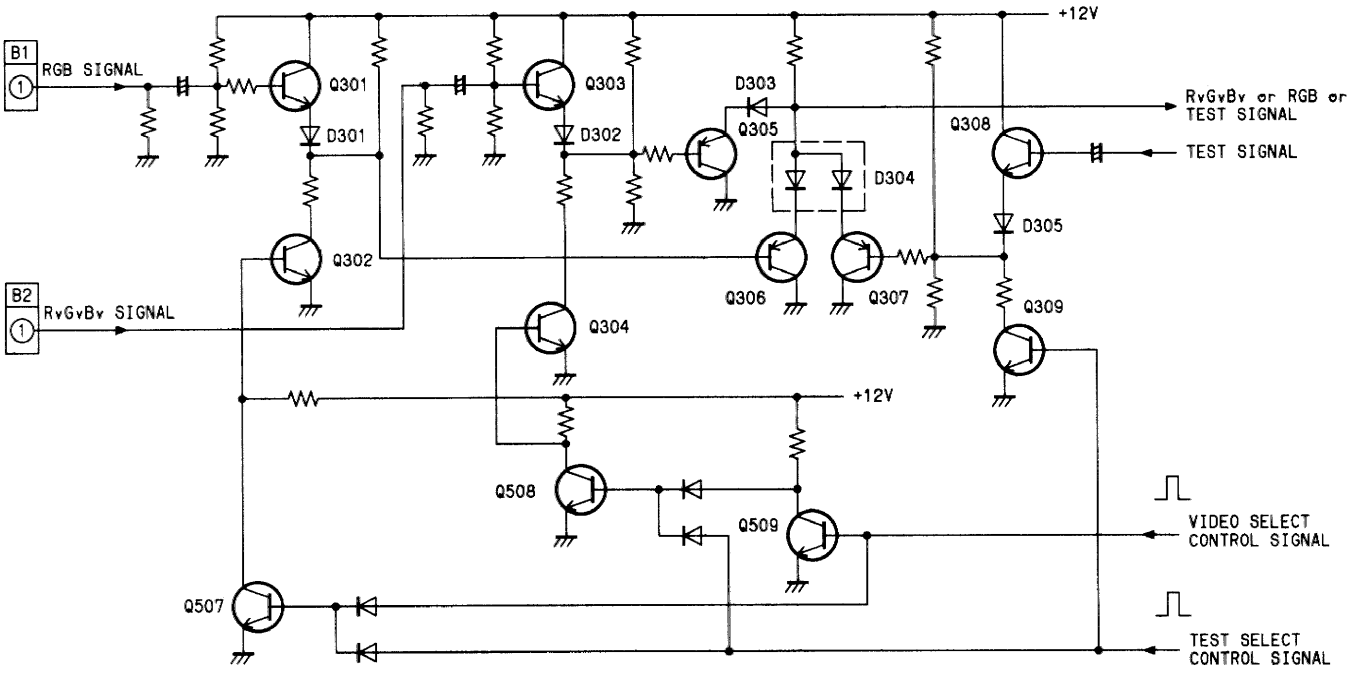


Fig. 31

For example, if the video mode (LINE or S-VIDEO) has been selected as the input mode, an H level select signal is added to Q509 or Q507, switching Q509 ON, Q508 OFF and Q304 ON. This makes the anode side of D302 to be at L level, causing the signal from Q303 to be outputed to the base side of Q305. At this time, the anode sides of D301 and D305 are at H level, suppressing the output of the RGB signal being inputed to Q301 and the TEST signal being inputed to Q308.

(3) Shading correction Circuit

A. Function

Using the H. PARABOLA, H. SAWTOOTH, V. PARABOLA, V. SAWTOOTH correction waveforms, the shading correction circuit performs the following:

① Color correction . . . . . .H. SAWTOOTH waveform

② Horizontal direction center and border brightness correction . . . . . .H. PARABOLA waveform

③ Vertical direction and border brightness correction . . . V. PARABOLA waveform

④ Vertical direction up/down brightness correction. . . . . V. SAWTOOTH waveform

B. Circuit Operation

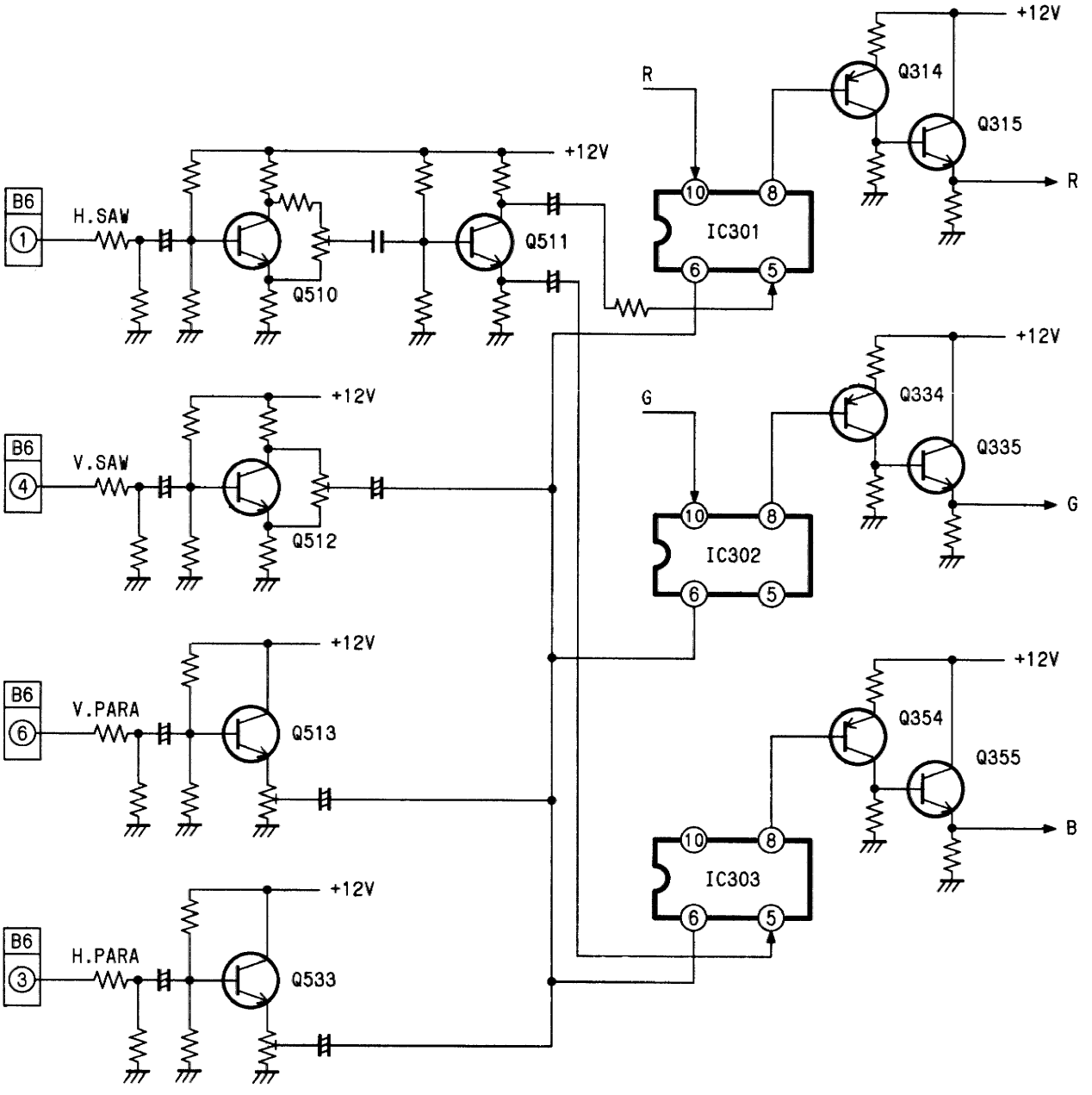


Fig. 32

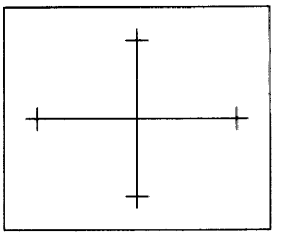
(4) Test Pattern Generator Circuit

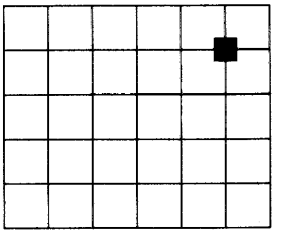
This circuit generates two types of test patterns. One test pattern is generated using an internal oscillator and without using any external signal, and the other test pattern is generated by synchronizing to an external signal.

① Test pattern by internal oscillator

f_H : 15.75 kHz — Cross bar pattern

f_V : 60 Hz — Cross hatch pattern





② Synchronized test pattern with external signal

f_H : 15 ~ 37 kHz — Cross hatch pattern

f_V : 50 ~ 100 Hz

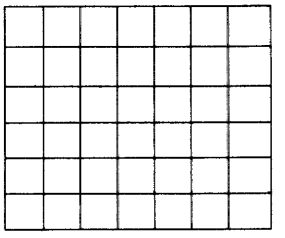


Fig. 33

Circuit Operation (internal oscillator test pattern generator circuit)

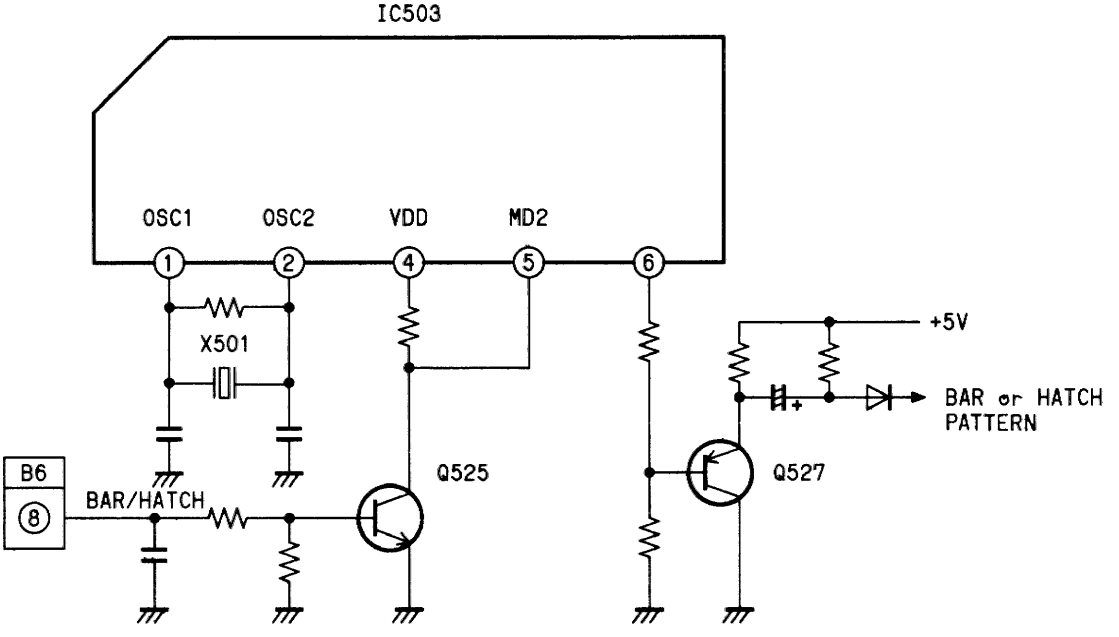


Fig. 34

A 3.58 MHz oscillator is placed between ① and ② of IC503, and its signals are divided within IC503 to generate a cross bar or hatch signal of f_H = 15.75 kHz and f_V = 60 Hz. Cross bar or cross hatch pattern is selected by applying the selected signal to Q525's base.

Circuit Operation (Test pattern generating circuit synchronized with external signal.)

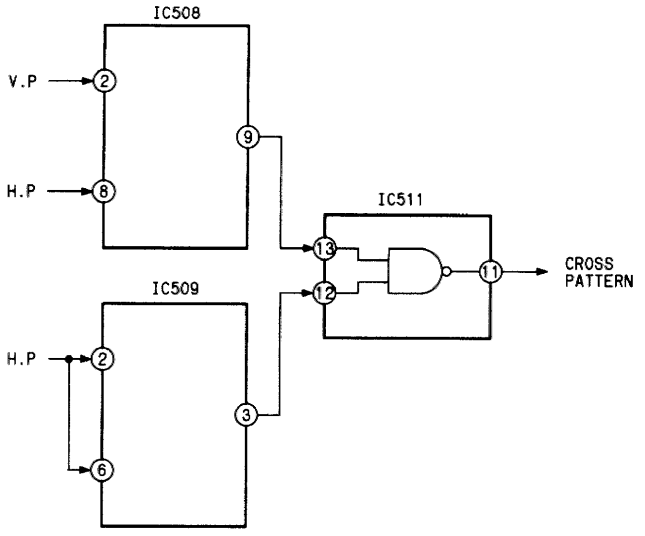


Fig. 35

The circuit centered around IC508 generates the horizontal line pattern.
The circuit centered around IC509 generates vertical line pattern.
IC511 mixes the horizontal and vertical lines.

Circuit Operation (Select circuit for internal oscillator and external signal synchronized test patterns)

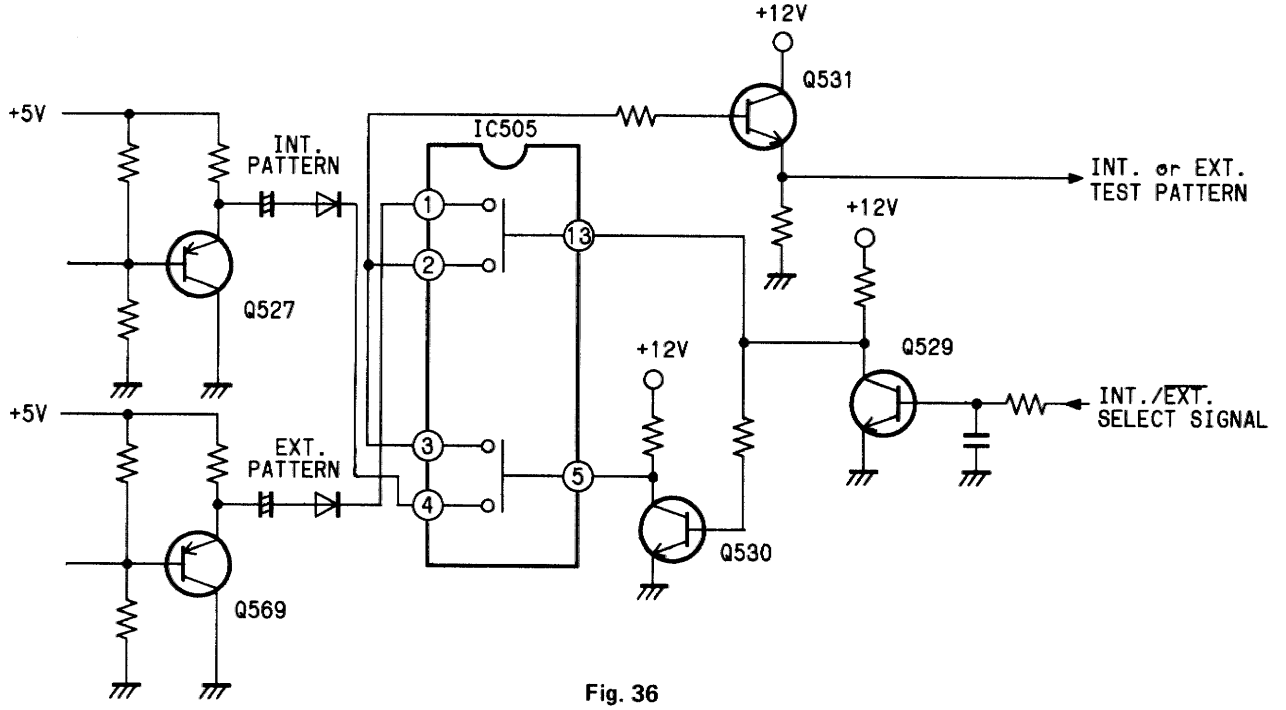


Fig. 36

If the TEST PATTERN SW next to the convergence VR block is put in the VIDEO position, H level INT select signal is inputed to Q529's base and IC505's ③ and ④ becomes closed, causing the INT pattern (test pattern generated using the internal oscillator) to be applied to ④ and the output goes to Q531. At this time, EXT pattern (test pattern generated to be synchronized to the external signal) is not outputed because IC505's ① and ② are open.

(5) Clamping Pulse Generation Circuit

A. Function

This circuit generates two types of clamping pulses (back porch clamping pulse and center clamping pulse) and adds them to the shading correction circuit and the contrast/brightness control circuit to stabilize the image.

① Back porch clamping pulse ...Clamping pulse for video (Y/C, LINE) and G/SYNC signals.

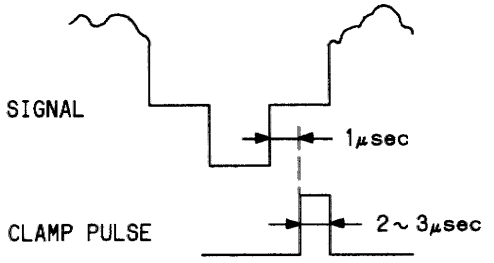


Fig. 37

② Center clamping pulse .....Clamping pulse for RGB signal (excluding G/SYNC)

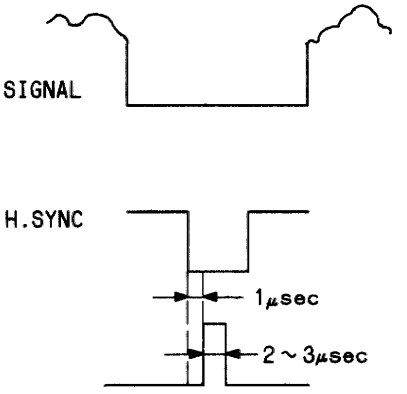
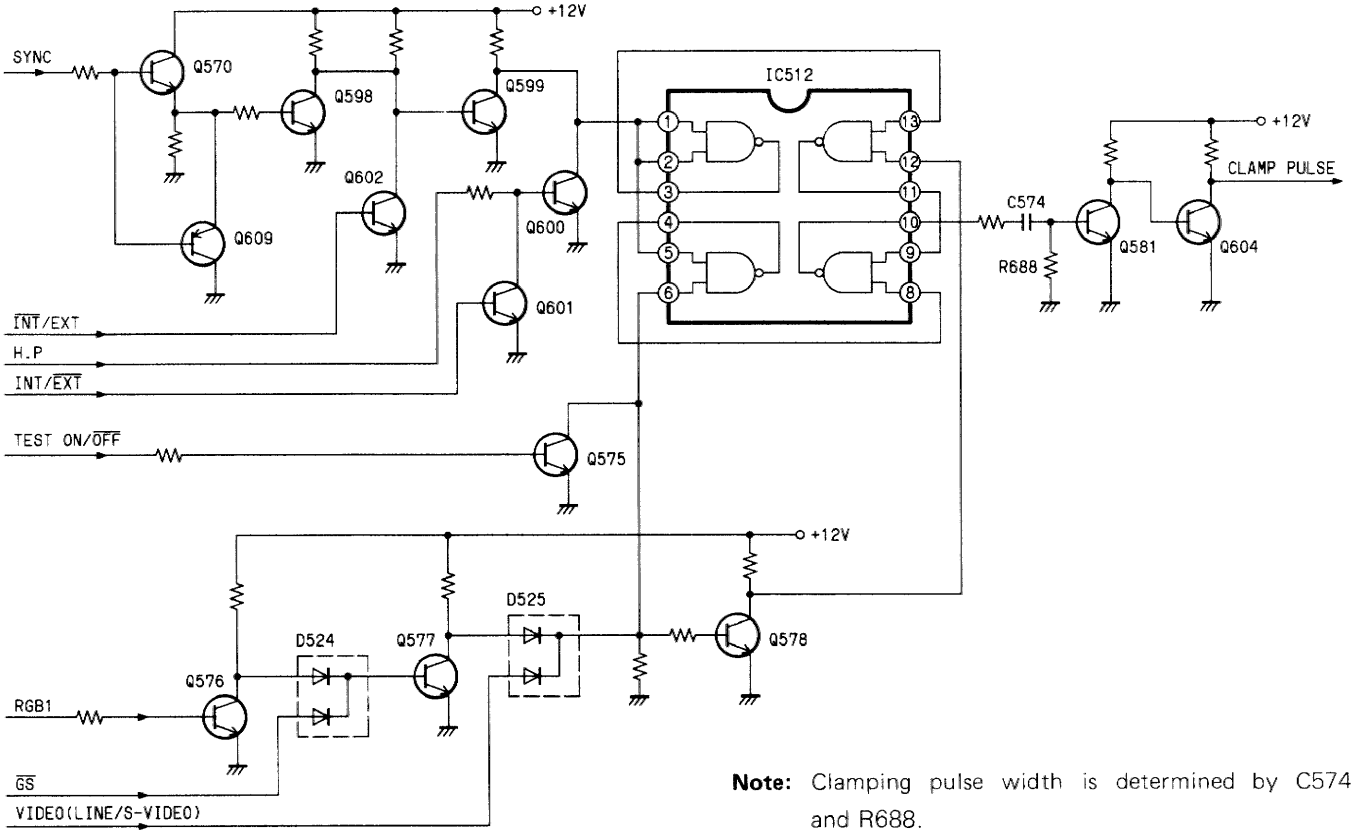


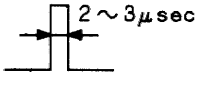
Fig. 38

B. Circuit Operation



Note: Clamping pulse width is determined by C574 and R688.

Fig. 39



For video (Y/C, LINE) and G/SYNC, negative polarity pulse is generated from IC512's ⑩. For RGB (except G/SYNC), positive polarity pulse is generated. The negative or positive pulse is differentiated by the generate back porch or center clamping pulse.

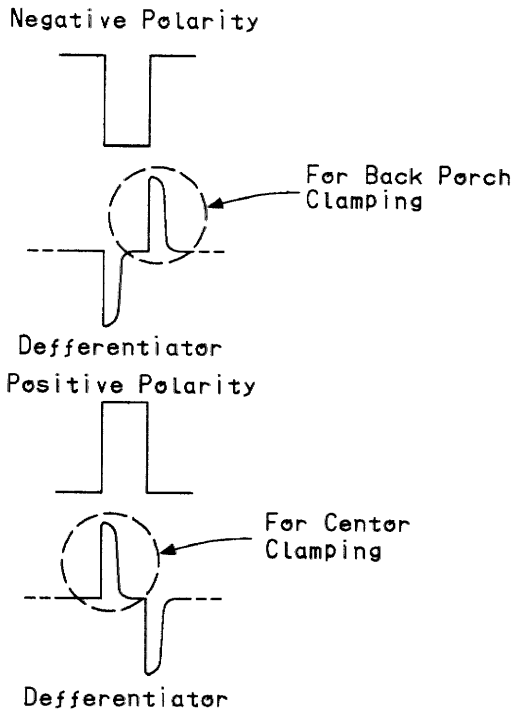


Fig. 40

(6) H-BLK and V-BLK pulse generation circuits

A. Function

Blanking is performed separately for the video (Y/C, LINE) mode and the RGB mode. Blanking pulses can also be adjusted individually as described below, so that corrections can be made within certain range by adjusting specified VR's if problems are encountered on the screen display due to input signal characteristics.

① For the video (Y/C, LINE) mode
H-BLK and V-BLK can be adjusted independently for the desired blanking position.
Note: Blanking width is fixed.
H-BLK position R618
V-BLK position . . . . . .R562 (NTSC)
R560 (PAL/SECAM)

② For RGB (RGB1, RGB2) mode
V-BLK pulse width is variable. H-BLK pulse width is fixed by the horizontal pulse since the operation of the H-BLK circuit is based on horizontal pulse.
V-BLK width control. . .R558

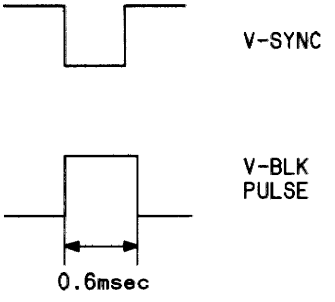


Fig. 41

Note: The factory adjusts the following, V-BLK pulse is set to 0.6 msec. V-BLK pulse width is variable, but never adjust it to less than 0.6 msec.
Doing so may cause retrace lines to appear to disable complete keystone correction.

H-BLK . . . . . .H-BLK is generated by the H-BLK circuit (a separate circuit) which uses the horizontal pulse (H.P), so that the H-BLK pulse width is determined by H.P. (5.5 μsec).

B. Circuit Operation

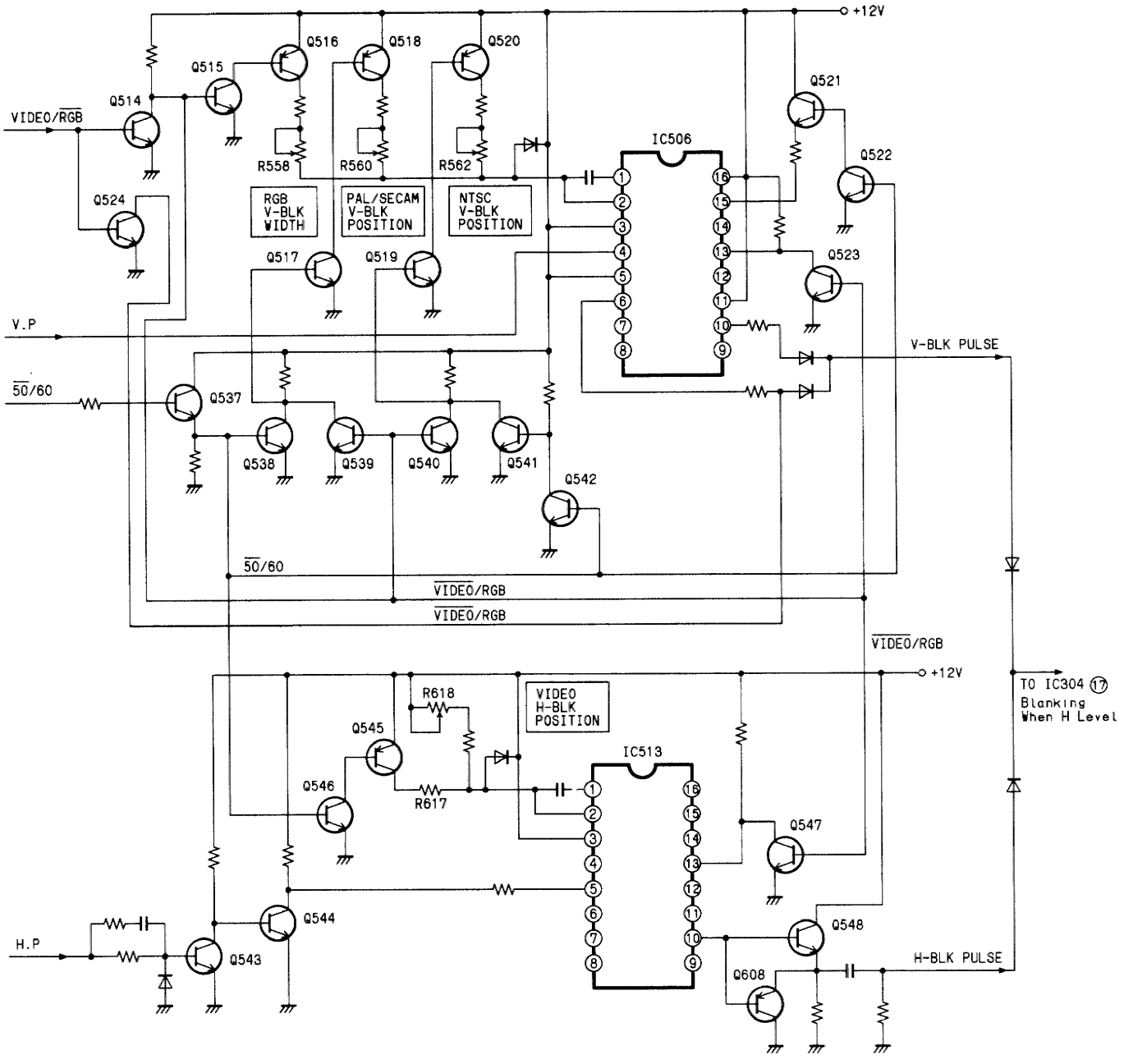


Fig. 42

The V-BLK pulse is generated by the circuit centered around IC506, and the H-BLK pulse is generated by the circuit centered around IC513. V-pulse is inputed to ④ and V-BLK pulse is outputed from ⑩ , both of IC506. H-pulse is applied to ⑤ and H-BLK is outputed from ⑩ , both of IC513.

The V-BLK pulse generating circuit adds the VIDEO/RGB and 50/60 control signals to the respective control transistors to switch ON/OFF these transistors for controlling the V-BLK pulses.

Similarly, the H-BLK pulses generating circuit controls the H-BLK pulse output using the VIDEO/RGB and 50/60 control signals. Frequency of the H-pulse depends on the input video signal, and Q545 is switched ON or OFF by the 50/60 control signal to either include or not include R617 in the circuit which enables the discrimination between the H-BLK pulses for PAL/SECAM and NTSC. In the RGB mode, horizontal blanking is done by switching Q361 (R), Q362 (R) and Q363 (R) by H-pulse.

(7) Blankout Circuit

A. Function

This circuit blanks out (darkens) the screen momentarily (approximately 1 second) when the signal input mode is switched and when the power switch is turned ON.

B. Circuit Operation

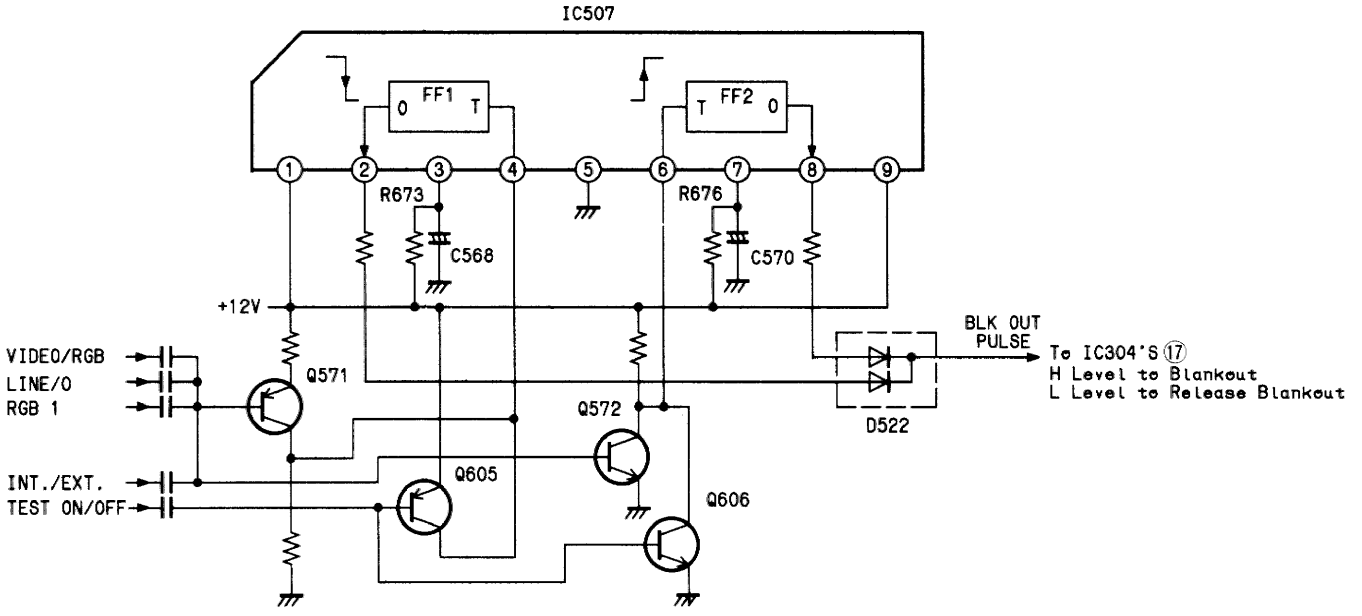


Fig. 43

IC507's FF1 triggers by the loading edge of the pulse and FF2 triggers by the trailing edge of the pulse respectively, of the input control signal. C568 and R673 or C570 and R676, whichever is applicable in a particular case, determines the blankout time (approximately 1 second).

(8) Cutoff Circuit

A. Function

This circuit cuts off CRT's G1 electrode to approximately −160V when deflection circuit stops in order to prevent CRT's burn out. It also cuts off the G1 electrode to approximately −160V when the power switch is turned OFF.

B. Circuit Operation

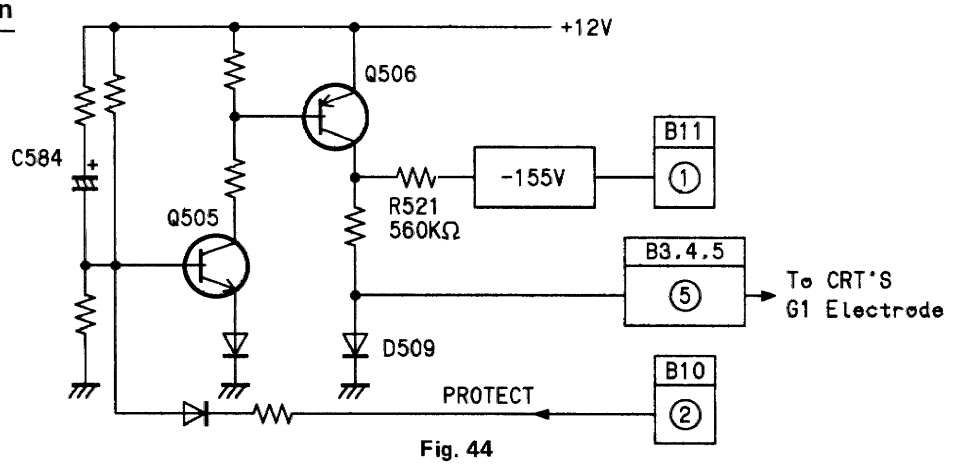


Fig. 44

Normally (when image or raster signals a displayed on the CRT screen), Q505 and Q506 are ON with the approximately 0V ~ 1V clamping voltage from D509 is added to the CRT's G1 electrode. When the deflection circuit is operating normally, a High level signal is being inputed from B10 connector's ② pin and Q505 and Q506 are ON.

When the deflection circuit stops, the signal from B10's ② changes to L level. When the power switch is turned OFF, C584 causes Q505's base voltage to drop to a negative value (L level). This causes Q505 and Q506 to be turned OFF and −155V to be applied to CRT's G1 electrode, resulting in the cutoff condition.

(9) ABL Circuit

A. Function

For PT-105, the method of controlling the contrast voltage (and not brightness control) is used to achieve ABL control. This circuit is set for a high ABL GAIN (sensitivity) to achieve a constant beam current level. Also by contrast voltage control, RGB drive voltage (in the video mode) and R, G and B drive voltages (in the RGB mode) are controlled.

Note: For the RGB mode, the drive voltages are set to lower levels than for the video mode (in order to produce well-modulated RGB signal images).

B. Circuit Operation

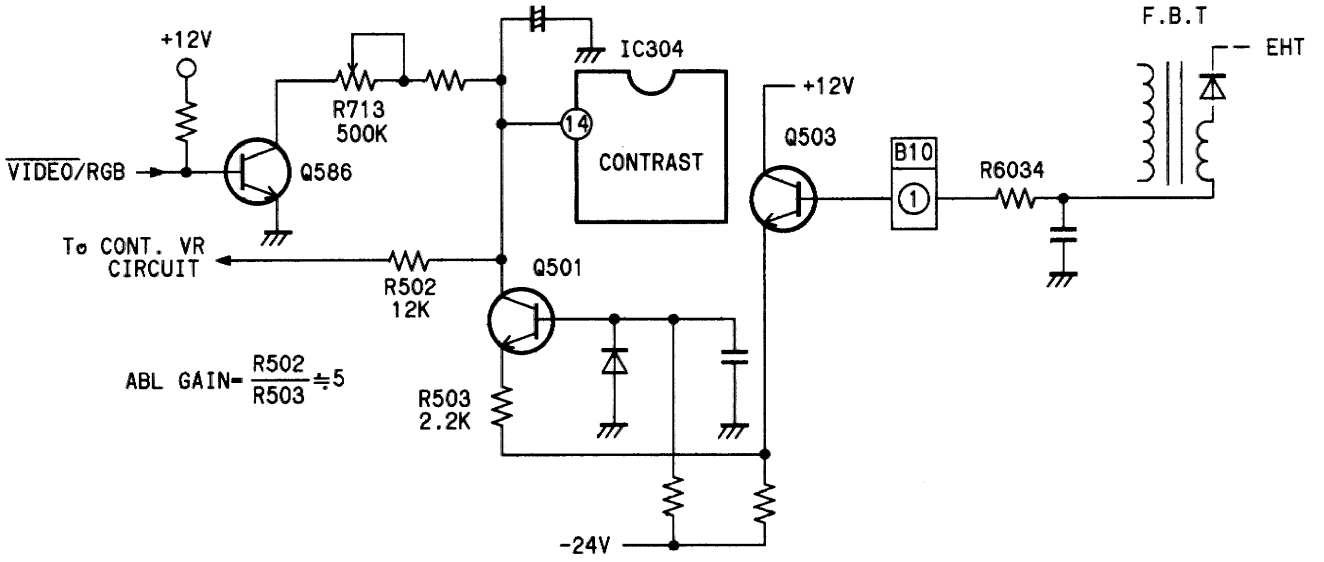


Fig. 45

Q503's base detects the beam voltage (current) to control Q501 for the purpose of controlling the contrast voltage at IC304's ⑭. The VIDEO/RGB control signal is used to switch Q586 ON and OFF, which determines whether or not to include R713 (500Ω) in the circuit. In the RGB mode, Q586 is ON so that R713 is included and therefore the contrast control voltage is lower than in the video mode. This causes R, G and B drive voltages to be lower, too.

III. VELOCITY MODULATION (VM) CIRCUIT

A. Function

In the video mode, the input signal (Y-signal) is differentiated to generate a signal that is added to the electron beam controlling velocity modulation (VM) coil (a new coil developed for PT-105). This controls the horizontal scanning speed to follow the brightness variation, improving sharpness of the screen displayed image.

Principle of VM

When a current that has the same waveform as the signal (b) obtained by differentiating the supplied image signal (a) is fed to the VM coil, a magnetic field described by (c) acts on the electron beam. This causes the scanning speed to vary as illustrated by (d) and the on-screen brightness to vary as illustrated by (e). In other words, the horizontal direction sharpness is improved.

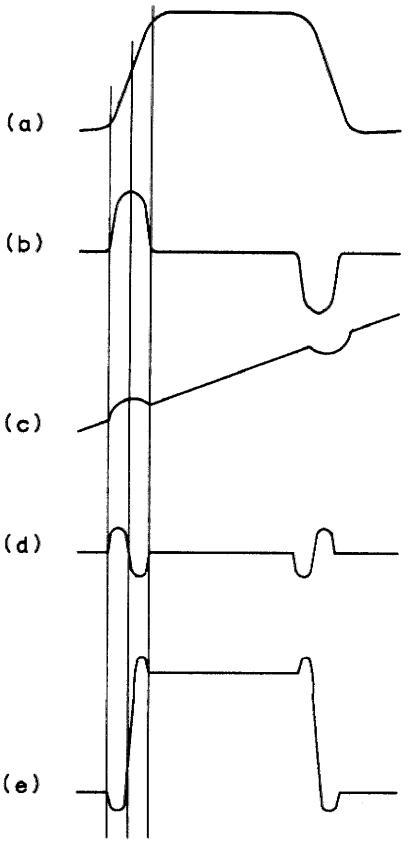


Fig. 46

B. Circuit

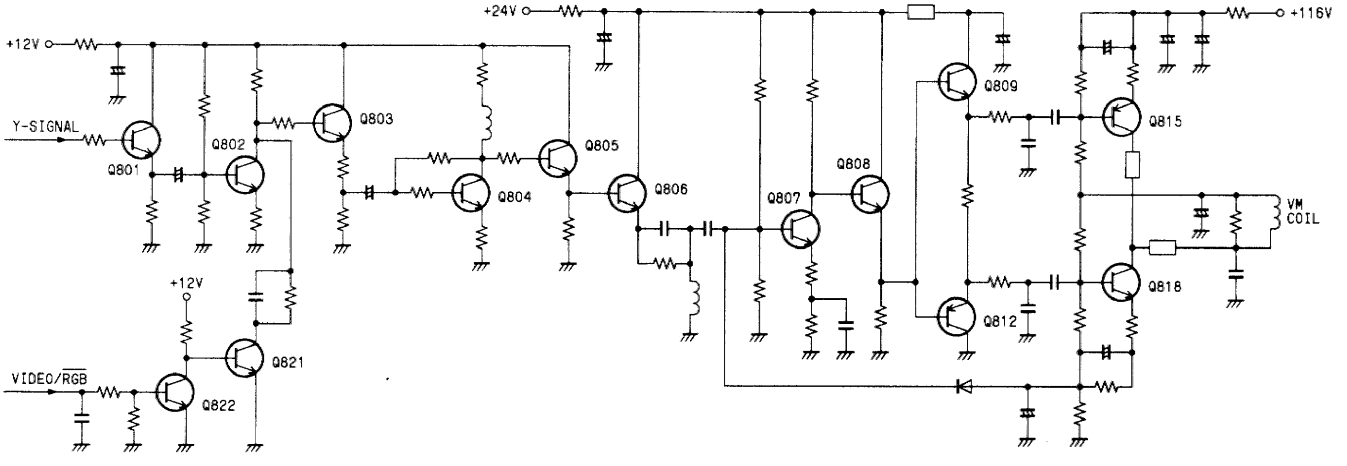


Fig. 47

IV. CONVERGENCE CIRCUIT (C-Board)

1. Convergence VRs and Their Locations

There are two major types of convergence VRs, namely convergence VRs (user controlled VR) and dynamic convergence VRs (installer adjusted VR). Fig. 48 shows the locations and types of convergence VRs used.

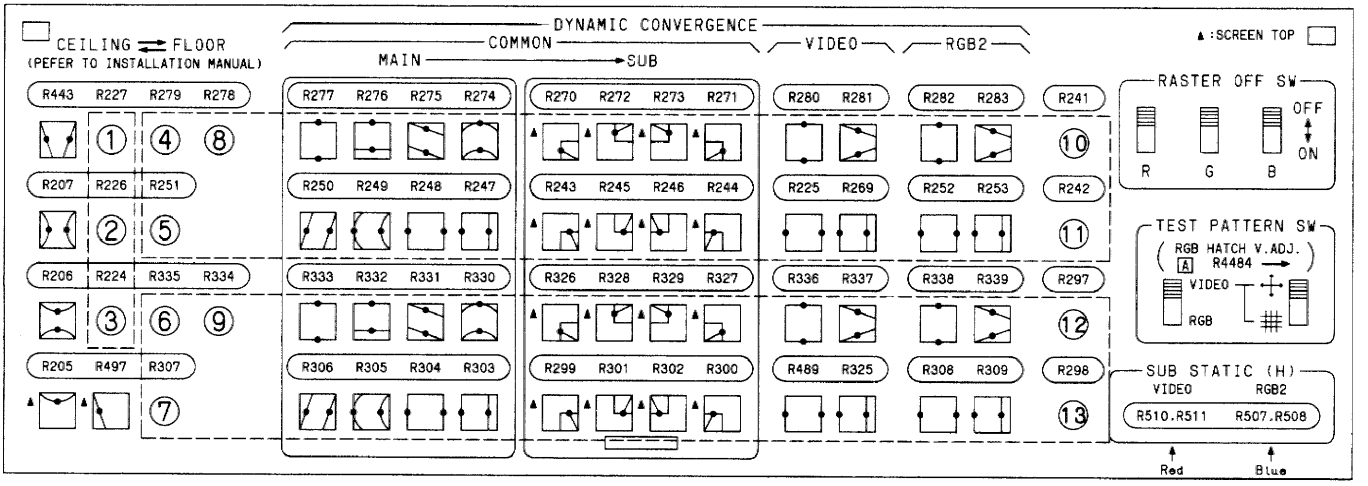


Fig. 48

Supplemental Explanation

- The group of VRs consisting of R280, R281, R225, R269, R336, R337, R489 and R325 the VRs R510 and R511 function only in the video input mode.
- The group of VRs consisting of R282, R283, R252, R253, R338, R339, R308 and R309 and the VRs R507 and R508 function only in the RGB2 input mode.
- Other VRs function in any mode.

2. Dynamic Convergence VRs and Their Functions

(1) Raster adjustment - - → Basically, R443, R207, R206, R205 and R497 shown in Fig. 48 are used for raster adjustment.

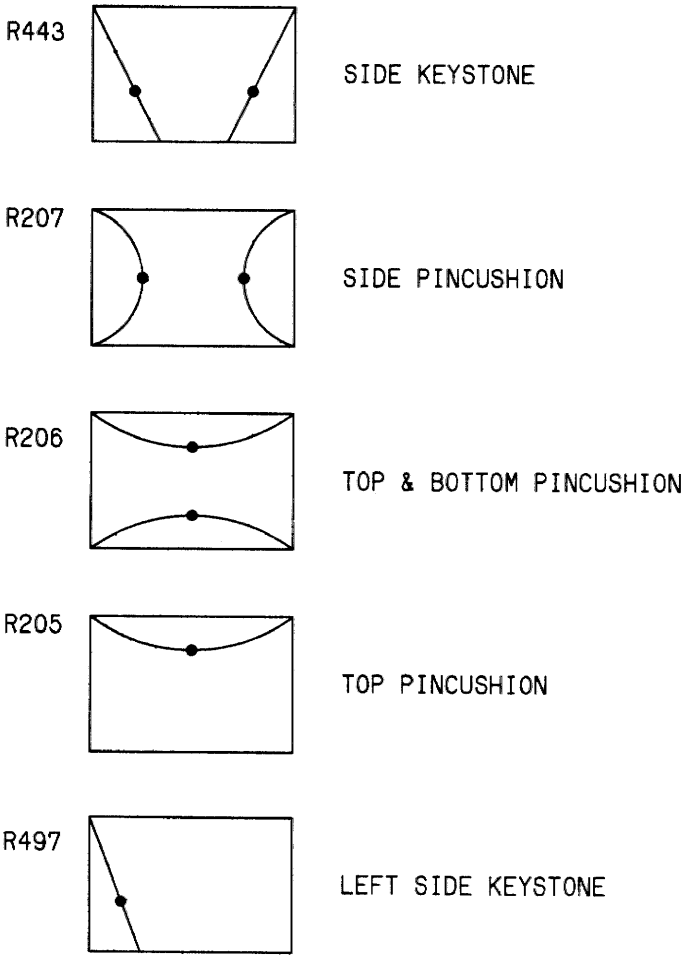


Fig. 49

(2) Auxiliary VRs for Signal Correction

Raster and dynamic convergence adjustments are made basically using the VRs shown in Fig. 48, but the following auxiliary VRs are provided as well (shown in Fig. 48) as ① through ⑬ :

Functions of Auxiliary VRs ① ~ ⑬

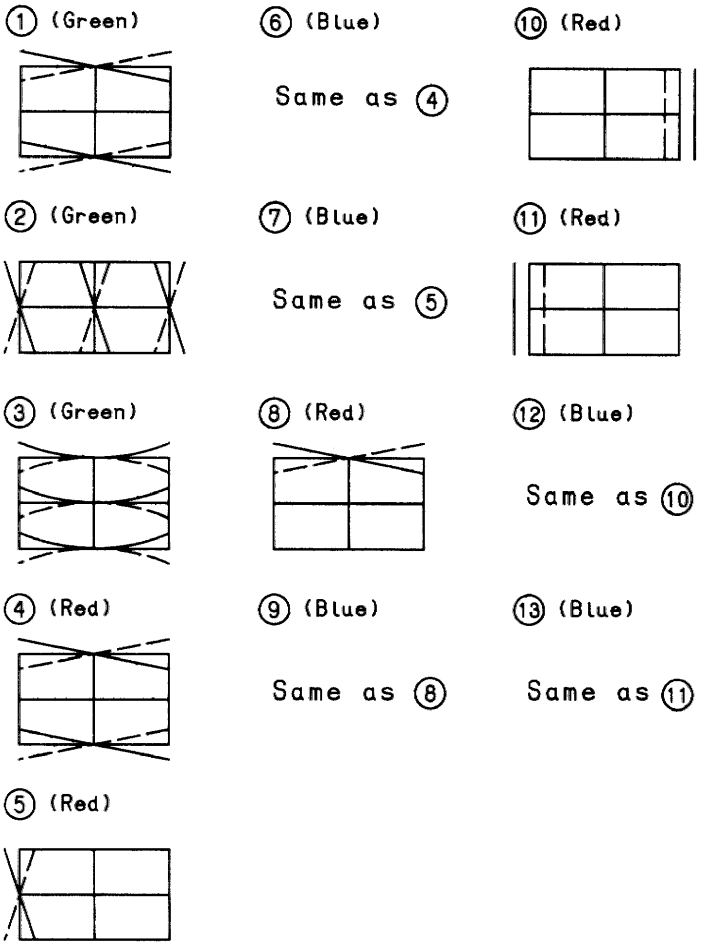


Fig. 50

3. Dynamic Convergence Adjustment Procedures

Dynamic convergence adjustment is performed in the sequence shown in the following table (for details, refer to the Installation Manual):

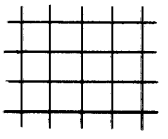
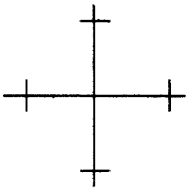
Adjusting Sequence	Signal input at adjusting time / Adjusting position	A	B	C	D	E	F	G
1	COMMON	RGB 1	RGB 1	RGB 1	RGB 2	RGB 1	RGB 2	VIDEO
2	RGB or VIDEO	RGB 2	RGB 2	VIDEO	VIDEO			
3	VIDEO	VIDEO						

4. Test Patterns for Convergence Adjustment

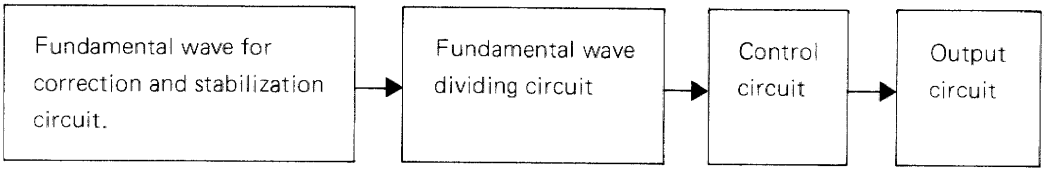
The following patterns are available for use in convergence adjustment:

① Cross hatch pattern by internal oscillator.
② Cross hairline pattern by internal oscillator.
③ Cross hatch pattern synchronized to any input signal.

The following table summarizes the purposes and regeneration methods for these test patterns:

		f_H, f_V	Regeneration method	Purposes
①	Cross hatch by internal oscillator	f_H = 15.75 kHz f_V = 60 Hz	(i) Test switch : ON (ii) TEST PATTERN switch: VIDEO 	① Can be used as convergence adjustment pattern for the video mode. ② Enables video mode convergence adjustment without video mode input source. ③ Enables verification of scanning direction.
②	Cross hairline by internal oscillator	f_H = 15.75 kHz f_V = 60 Hz	(i) TEST switch : ON (ii) TEST PATTERN switch: VIDEO 	① Can be used as static convergence adjusting pattern for the video mode.
③	Cross hatch synchronized to input signals	f_H and f_V are identical to the input signal frequencies	(i) TEST switch : ON (ii) TEST PATTERN switch : RGB	Enables convergence adjustment for each input mode (RGB1, RGB2, VIDEO, S-VIDEO) which is selected by the mode switching. (Input signal source must be connected.)

5. Configuration of Convergence Circuit (C-Board)



Fundamental wave generation and stabilization circuit:
This circuit generates the fundamental waves that is necessary for convergence correction.

Fundamental wave dividing circuit:
This circuit generates correction waveforms for the dynamic convergence adjustment VRs (MAIN, SUB (4 corners) and RASTER).

Control circuit:
This circuit receives divided waveforms from the fundamental wave dividing circuit and controls convergence. This circuit has a switching circuit that selects the control VRs that are functional for the input mode (VIDEO or RGB2) in effect.

6. Block Diagram of Convergence Correction Circuit

Fundamental Wave Generation and Stabilization

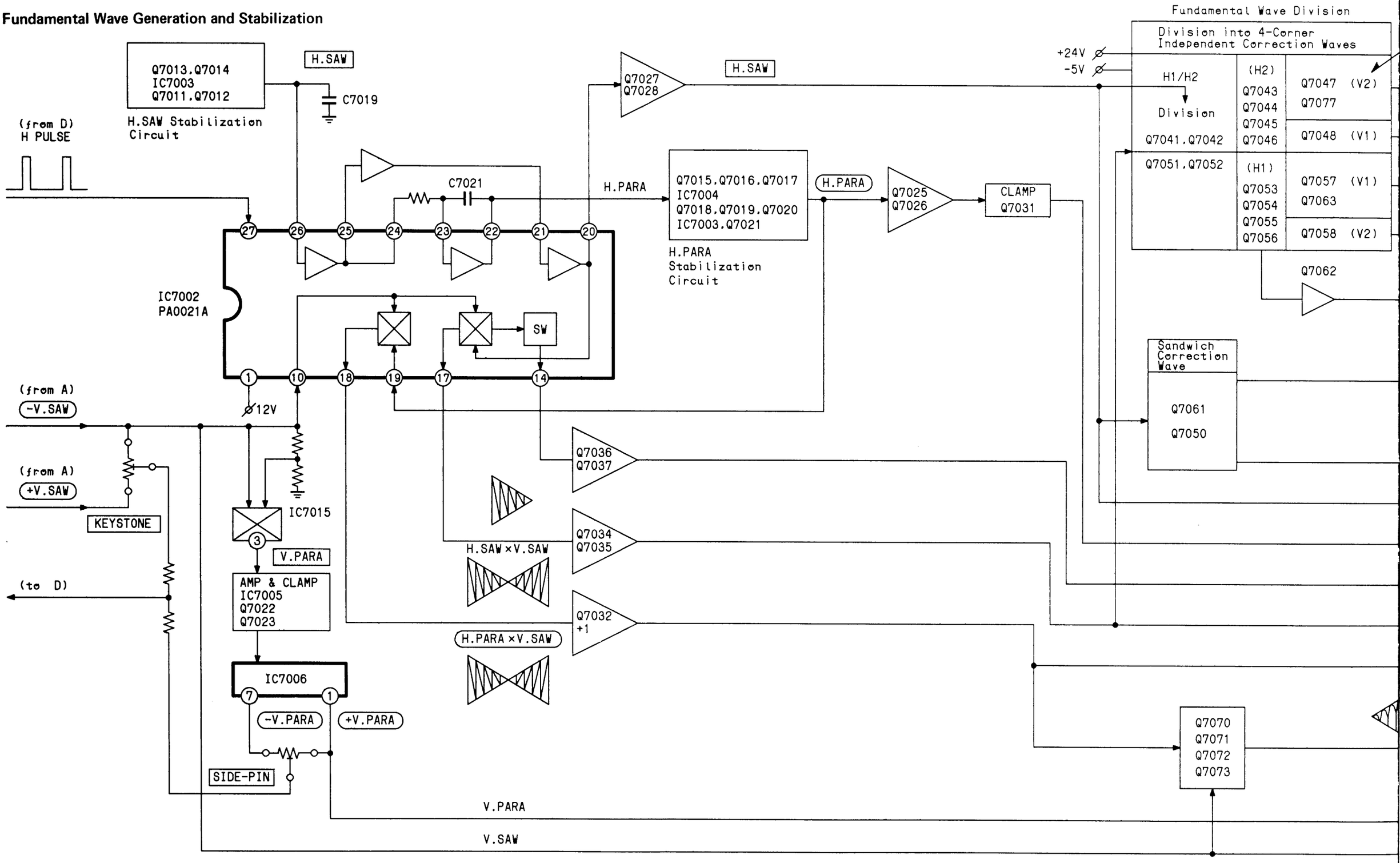


Fig. 51

Division
ner
ion Waves
Q7047 (V2)
Q7077
Q7048 (V1)
Q7057 (V1)
Q7063
Q7058 (V2)
Q7062
V1/V2
Division
H2V2
H2V1
H1V1
H1V2
H.SAW×V.SAW(H1)
SANDWICH RIGHT
SANDWICH LEFT
H.SAW
H.PARA
H.SAW×V.SAW(V1)
H.SAW×V.SAW
H.PARA×V.SAW
H.PARA×V.SAW(V1)
V.PARA
V.SAW
Control Section
COMMON
SUB
MAIN
ANAROG SW
IC7008,7009,
7014
VIDEO MODE
CONTROL VR
RGB 2 MODE
CONTROL VR
VIDEO
/RGB
RGB2
/OTHER
Q7078
(from B) VIDEO/RGB
Q7052
(from A) RGB1/OTHER
D7031
D7032
VIDEO/RGB
RGB2/OTHER
9V
STATIC CONVERGENCE
R R7344(H).R7350(V)
G R7343(H).R7349(V)
B R7345(H).R7351(V)
Q7081
Q7082
Q7079
Q7080
VIDEO SUB
STATIC CONV.
(H)
RGB2 SUB
STATIC CONV.
(H)
Output Section
+24V
-24V
C4
IC7010
R-H (D)
R-V (D&S)
CY(R)
H(D)
V(D&S)
H(S)
IC7011
R-H (S)
B-H (S)
CY(B)
H(S)
IC7012
B-H (D)
B-V (D&S)
V(D&S)
H(D)
C5
C6
IC7013
G-H (D&S)
G-V (D&S)
CY(G)
H(D&S)
V(D&S)

Fig. 51

7. Fundamental Wave Generation and Stabilization Circuit

Seven types of fundamental waveforms are necessary for convergence correction, and the following circuits, generate six out of the seven types.

Fundamental waveforms necessary for convergence correction:

① H. SAWTOOTH

② H. PARABOLA

③ H. SAW x V. SAW (V1)

④ H. SAW x V. SAW

⑤ H. PARA x V. SAW

⑥ V. PARABOLA

⑦ V. SAWTOOTH

Fig. 52

Note: V. SAWTOOTH is generated by the A-board (i.e., not by this circuit).

Circuit Operation

(H. SAW & H. PARA waveform generation and stabilization circuit)

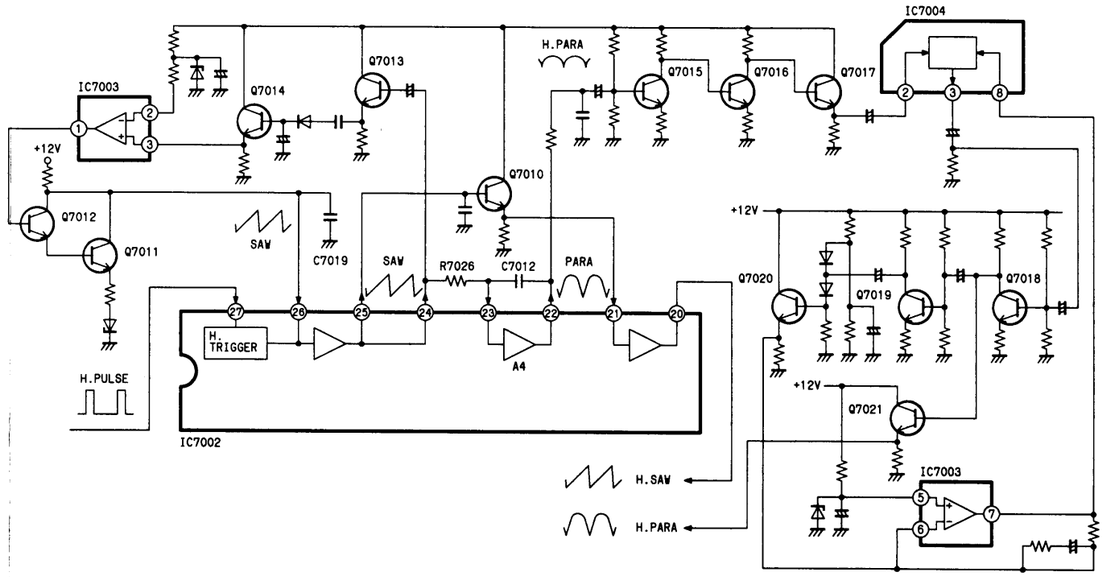


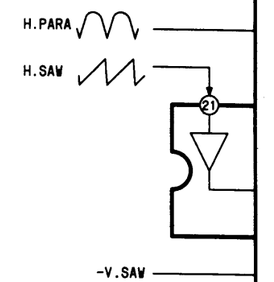
Fig. 53

H-pulse input goes to IC7002's ㉗ to charge or discharge C7019 to generate H. SAWTOOTH waveform (Q7012 and Q7011 make up a constant current circuit). Because fluctuation of the horizontal (H-pulse) frequency causes H. SAWTOOTH waveform's amplitude to fluctuate, feedback is applied from ㉔ via Q7013 ⟶ Q7014 ⟶ IC7003 ⟶ Q7012 ⟶ Q7011 so that the H. SAWTOOTH wave output from IC7002's ㉕ is stabilized at a constant amplitude. Q7013 and Q7014 detects and converts the sawtooth waveform output from ㉔ to DC voltage and adds the DC voltage to IC7003's ③. This DC voltage is compared with the reference voltage being inputed to IC7003's ②, and the difference is retrieved from ①. (IC7003 is a differential amplifier.) The voltage difference obtained from ① is used to control Q7012 and Q7011 which results in control of the constant current. This series of operation results in the generation of constant amplitude H. SAWTOOTH waveform, which is outputed through Q7010 ⟶ IC7002 ㉑, ⑳.

The H. SAWTOOTH waveform coming from R7026 is converted to H. PARABOLA waveform by the mirror integration circuit which is made up of C7021 and the A4 differential amp between IC7002's ㉓ and ㉒.

This parabolic waveform is unstable so that it is stabilized by the stabilization circuit made up of Q7015, Q7016, Q7017, IC7004, Q7018, Q7019, Q7020, IC7003 and Q7021. Operation of this stabilization circuit is essentially the same as that of sawtooth waveform stabilization circuit described above. The end result of this circuit is the stable H. PARABOLA waveform from Q7021's emitter.

Circuit Operation (bow



H. SAWTOOTH, H. PAR
waveforms are inputed to
tively, and converted to m
are outputed from ⑱, ⑰

Circuit Operation

(V. PARABOLA waveform

-V.SAW

IC7

IC7015 is a multiplier IC
waveform at ③ based on

Circuit Operation (bow waveform generation circuit)

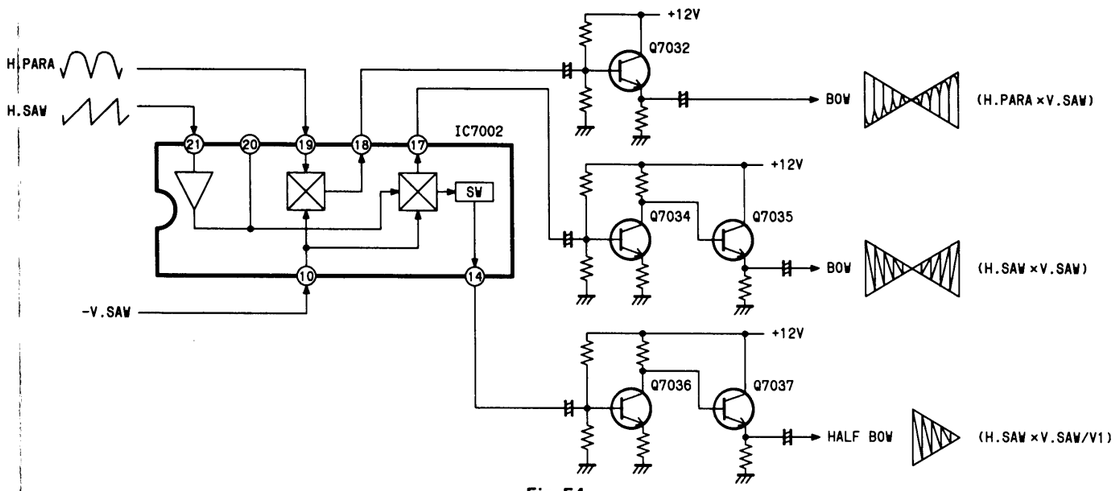


Fig. 54

H. SAWTOOTH, H. PARABOLA and −V. SAWTOOTH waveforms are inputed to IC7002's ㉑ , ⑲ and ⑩ , respectively, and converted to matrix waveform elements which are outputed from ⑱ , ⑰ and ⑭ , respectively. The −V. SAWTOOTH waveform input to ⑩ has been stabilized by the time it reaches this stage (because of A-board's stabilization function). Thus, there is no stabilization circuit within this portion of C-board.

Circuit Operation

(V. PARABOLA waveformgeneration circuit)

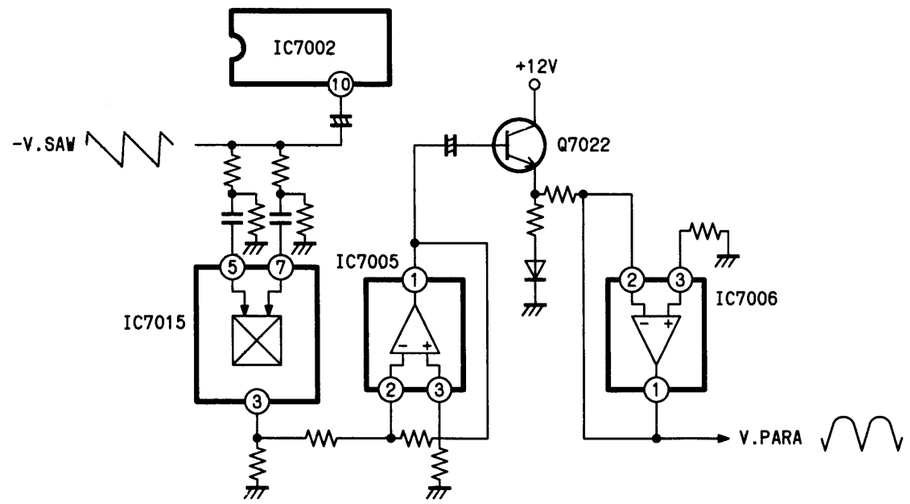


Fig. 55

IC7015 is a multiplier IC, and it generates a parabolic waveform at ③ based on the quadratic relationship between the V. SAWTOOTH waveforms having different levels input to ⑤ and ⑦.

8. Fundamental Wave Dividing Circuit

Division of the fundamental wave into the four corner independent correction waves is performed by a circuit made up of Q7041 ~ Q7048, Q7077, Q7051 ~ Q7058 and Q7063.

Circuit Operation

(4-corner independent correction wave dividing circuit)

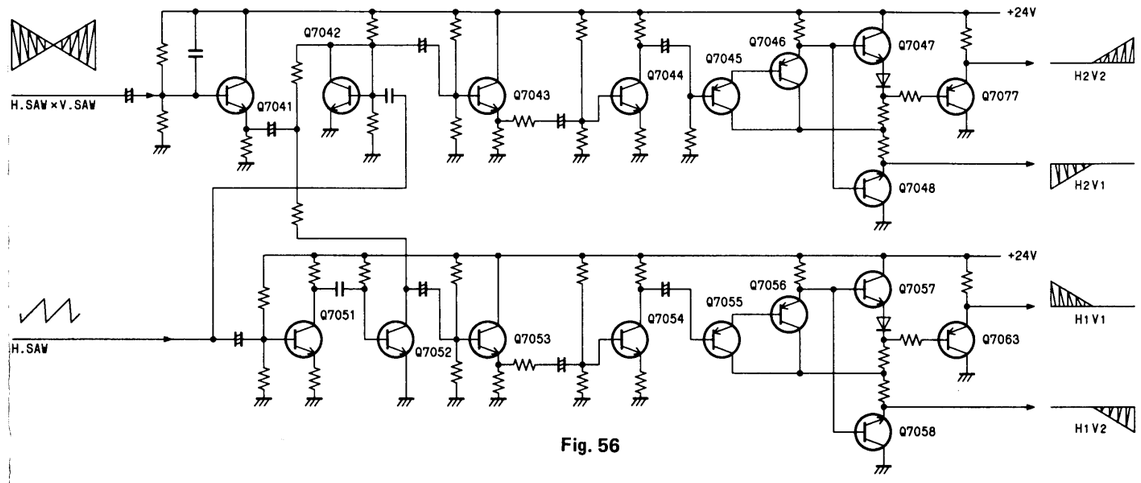


Fig. 56

Circuit Operation

(auxiliary VRs correction waveform dividing circuit)

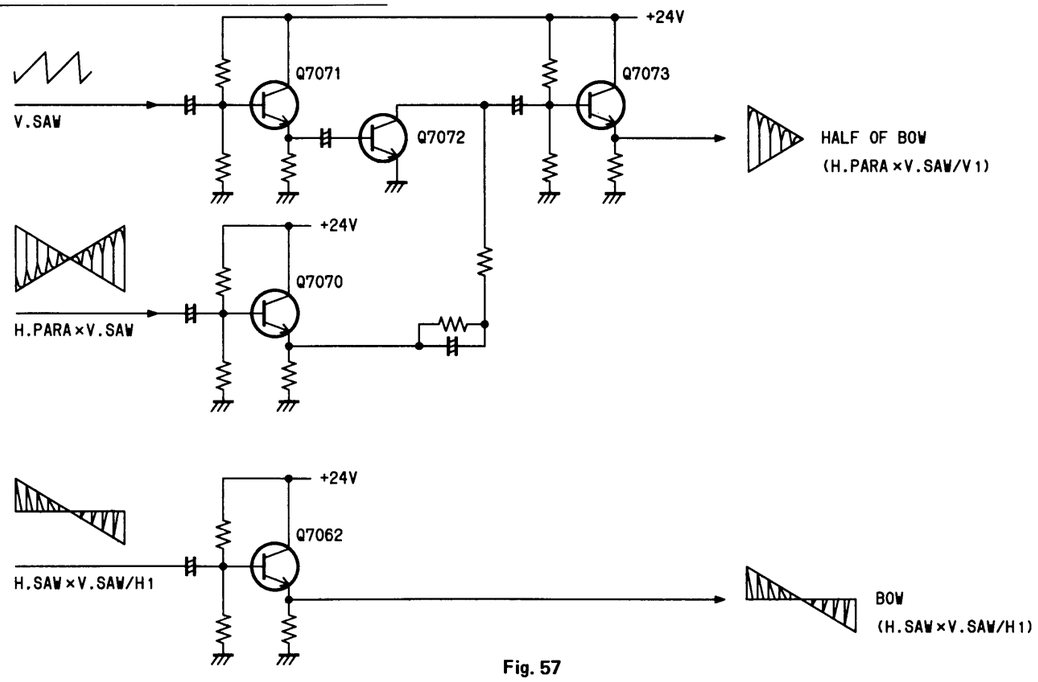


Fig. 57

MEMO

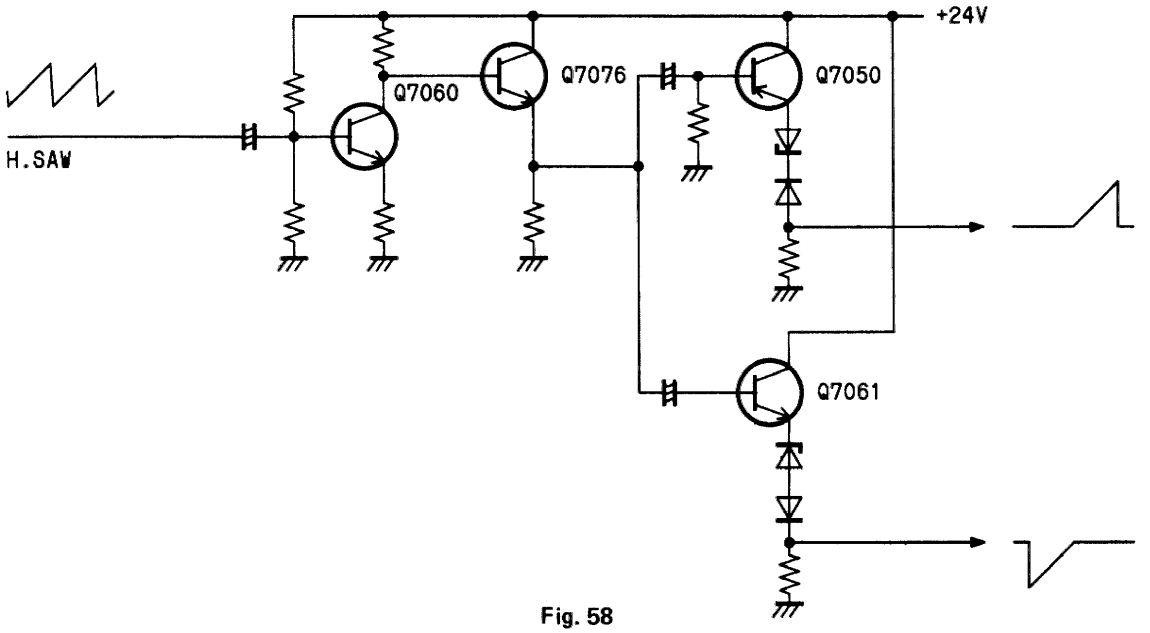


Fig. 58

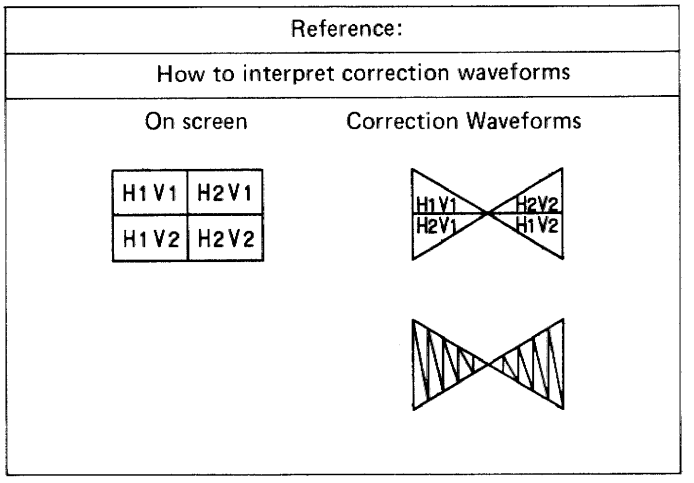


Fig. 59

9. Control Circuit

(1) ALL Mode

In the ALL Mode, the correction waveforms generated by the dividing circuit described above are inputed to and altered by variable resistance circuit (VRs).

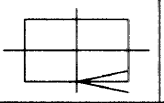
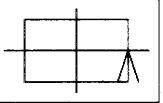
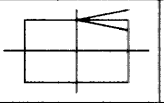
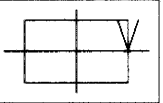
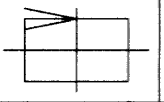
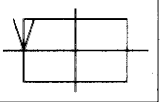
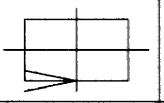
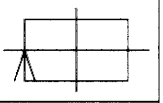
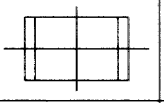
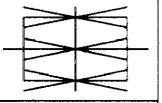
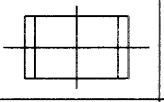
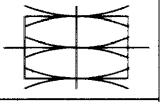
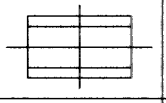
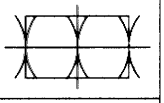
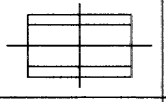
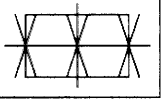
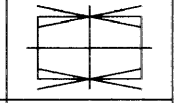
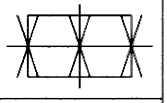
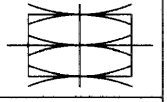
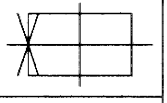
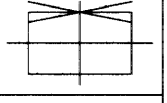
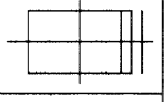
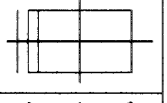
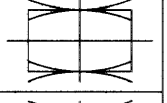
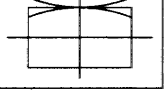
Input Correction Waveform	CONTROL VR	Correction Result	CONTROL VR	Correction Result	
	R270 R326		R243 R299		SUB
	R272 R328		R245 R301		
	R273 R329		R246 R302		
	R271 R327		R244 R300		
H.SAW	R248 R304		R275 R331		MAIN
H.PARA	R247 R303		R274 R330		
V.PARA	R276 R332		R249 R305		
V.SAW	R277 R333		R250 R306		
H.SAW×V.SAW	① R227 ④ R279 ⑥ R335				Auxiliary VRs
V.SAW	② R226				
H.PARA	③ R224				
H.SAW×V.SAW(H1)	⑤ R251 ⑦ R307				
V1	⑧ R278 ⑨ R334				
H2	⑩ R241 ⑫ R297				
H1	⑪ R242 ⑬ R298				
H.PARA×V.SAW	R206 (VIDEO) R1 (RGB1) R3 (RGB2)				Raster
V1	R205				

Fig. 60

(2) VIDEO Mode or RGB2 Mode

The VRs R280 ~ R283, R336 ~ R339, R225, R252, R253, R489, R325, R269 and R308, R309 are set in such a way that they function only in a certain (VIDEO or RGB2) input mode. Analog switches are operated by the input mode select control signal, and the appropriate correction waveforms for the specific input mode selector are added to these VRs.

Circuit Operation

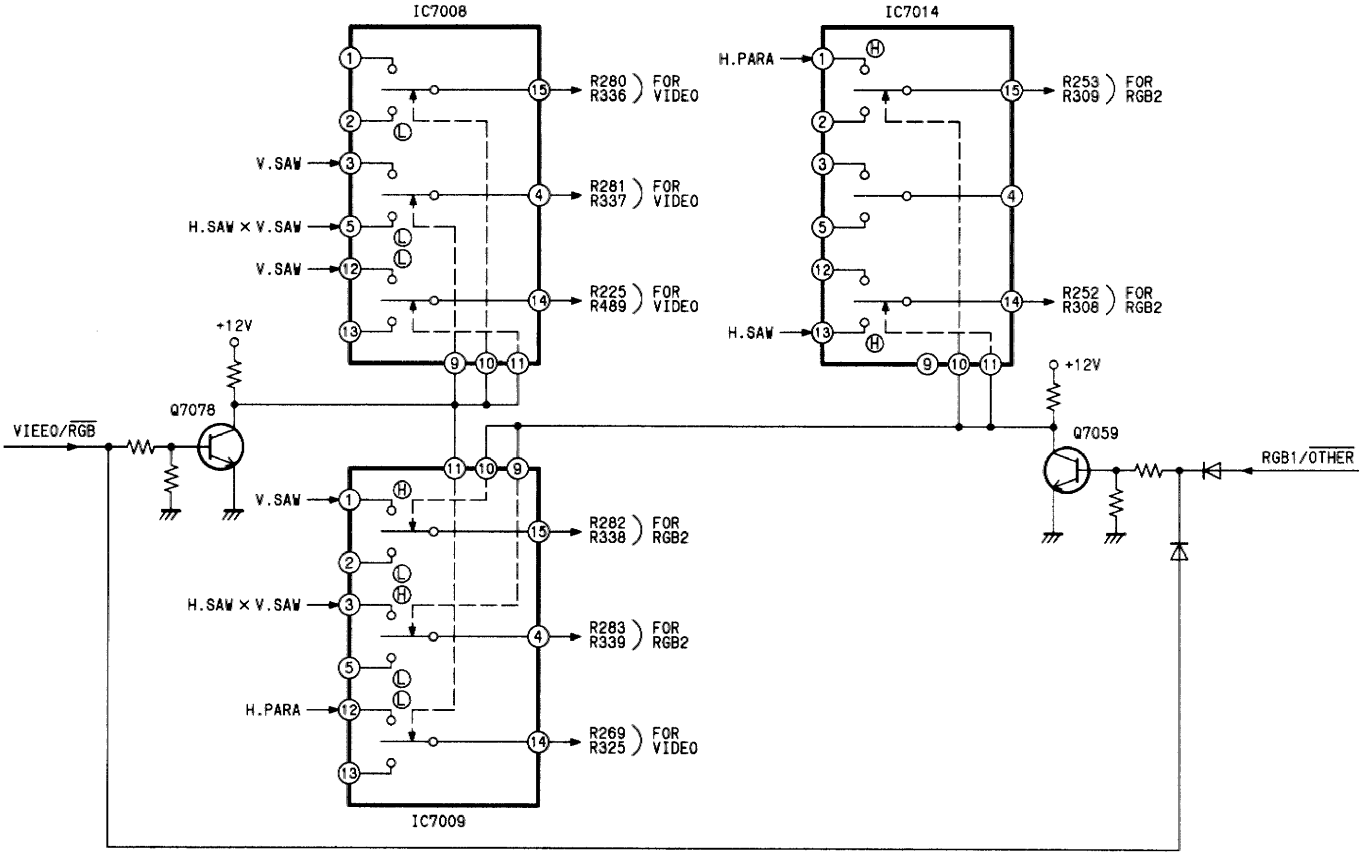


Fig. 61

In the VIDEO input mode, the input mode select control signal is at H level and added to the base of Q7078 and Q7059. This causes the collector to be at L level and all the analog switches are connected to the L side, so that the correction waveforms being inputed to IC7008, IC7009 and IC7014 are either outputed or not outputed, causing some of the convergence adjusting VRs to function or others, not to function as predetermined for the input mode. In the RGB2 input mode, the select control signal is added to Q7059 to operate analog switches to allow or stop the correction waveforms.

V. HORIZONTAL DEFLECTION CIRCUIT (D-Board)

1. Block Diagram

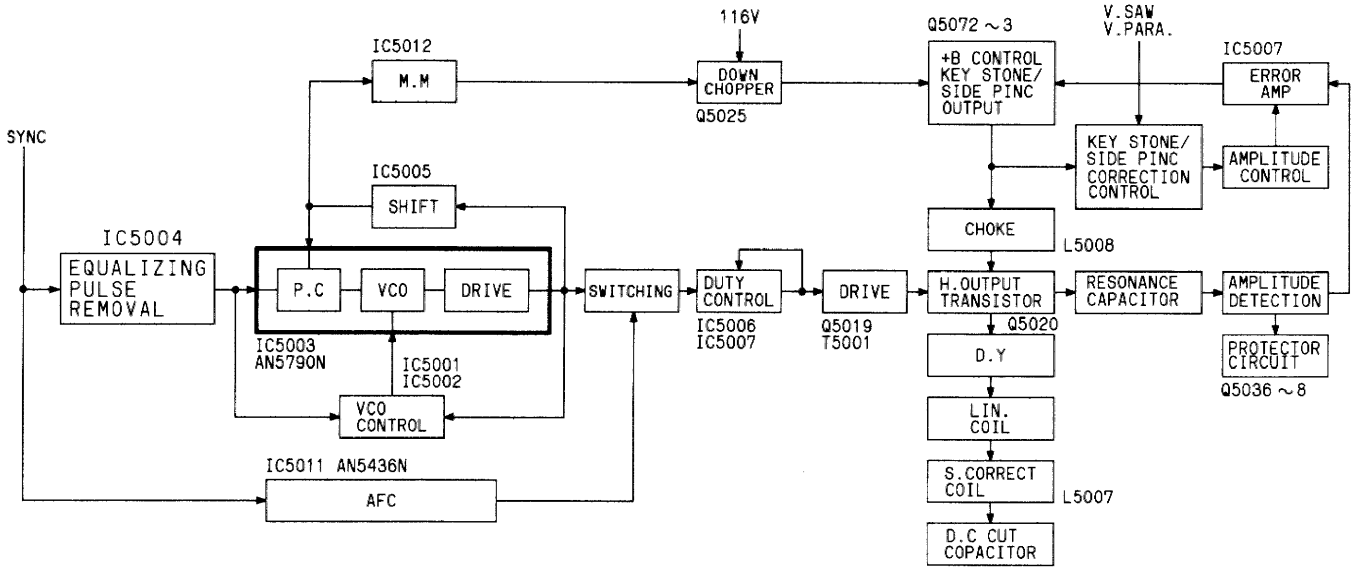


Fig. 62

2. Automatic Synchronization Circuit

(RGB1 & RGB2 Modes)

To enable interfacing computers, the RGB1 and RGB2 modes must include synchronization in a manner that follows the input horizontal frequency (f_H) (15 ~ 37 kHz). The lock-in range for the conventional television type AFC is only about ± 0.7 kHz that range is insufficient to work with computers. Therefore, an automatic synchronization circuit which incorporates not just AFC circuit but also VCO circuit is used in this model. This automatic synchronization circuit performs closed loop control to match the frequency of the H input SYNC to the frequency (oscillation frequency) at which the deflection coil is driven. A circuit that removes H. SYNC's equalizing pulses is provided immediately before the automatic synchronization circuit to support COMPOSITE SYNC as well.

Circuit Operation

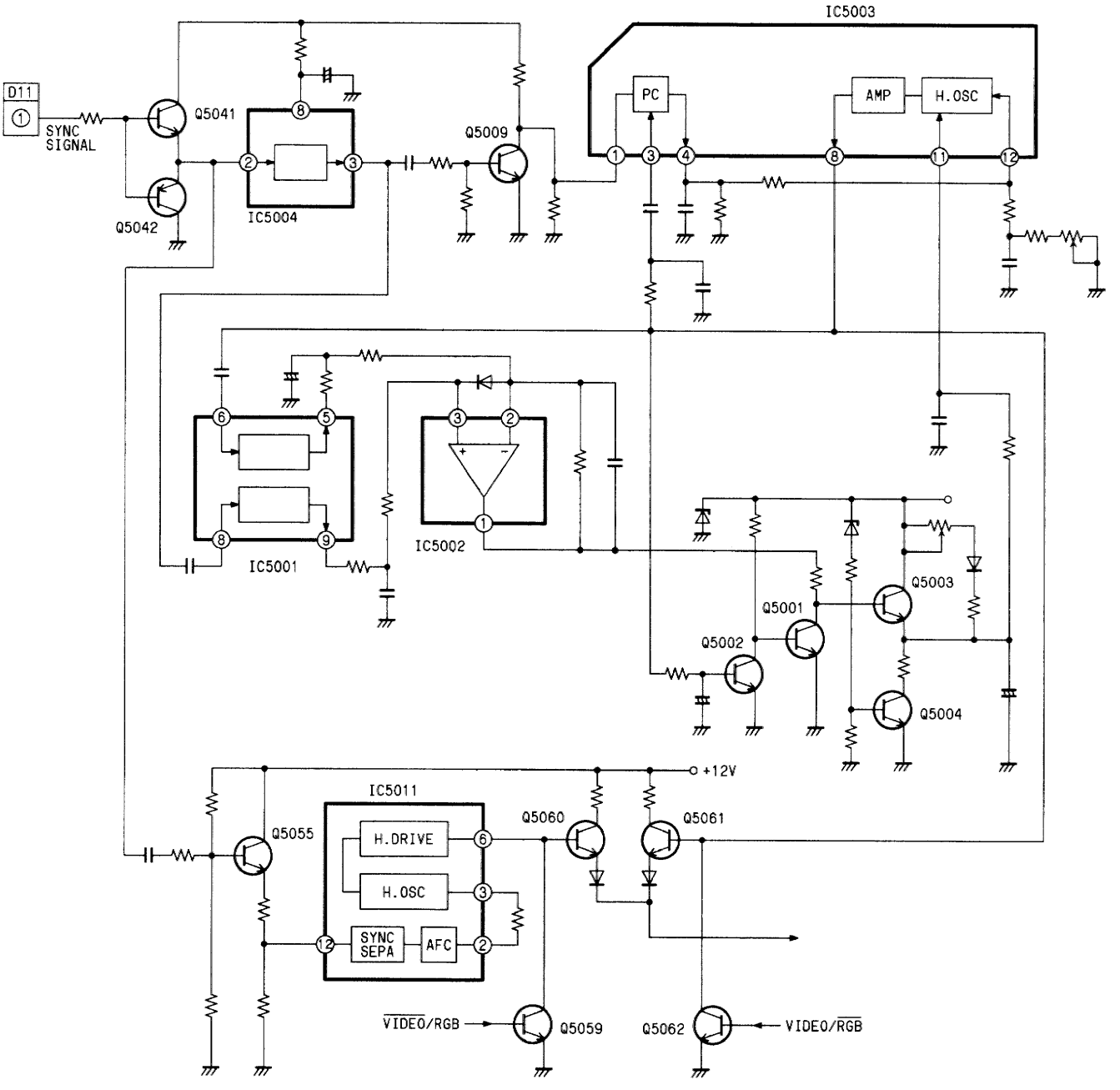


Fig. 63

The automatic synchronization circuit for the RGB mode consists of IC5004, IC5003, IC5001, IC5002, Q5001 ~ Q5004 and IC5011 is the AFC circuit for the VIDEO model. Q5059 ~ Q5062 switches between VIDEO and RGB modes and provides the deflection driver pulse waveform that is appropriate for the mode selected.

In the RGB mode, the H. SYNC control circit operates as follows: If the SYNC input from D11 ① is composite signal, IC5004, (H. SYNC equalizing pulse removal circuit) extracts and outputs only H. SYNC signal from ③. The H. SYNC signal outputed from IC5004's ③ is applied to IC5003 and is subjected to phase comparison with the oscillation frequency. IC5001 is a mono-multi circuit, and it adjusts the pulse input from ⑥ (pulse that has passed through IC5003) and the pulse input from ⑧ (pulse that has passed only through IC5004) to fixed width pulses by average value integration and output them to ⑤ and ⑨, respectively. IC5002 compares the two pulses mentioned above and obtains an error voltage between them. Q5001 ~ Q5004 make up a voltage control circuit, and its operation is based on the error voltage signal outputed from IC5002's ①. The ultimate result of this voltage control circuit is to control IC5003's ⑪ to output from IC5003's ⑧ an oscillation pulse signal that is synchronized to the input signal (H. SYNC).

In the VIDEO mode, the SYNC signal input from D11 ① passes through Q5041 and Q5042 and goes to IC5011's ⑫ via Q5055. IC5011 generates the convertional deflection oscillation and driving pulses.

3. Driving Circuit

This driving circuit is under closed loop control so that the driving pulse duty is kept constant regardless of the input frequency (f_H).

Circuit Operation

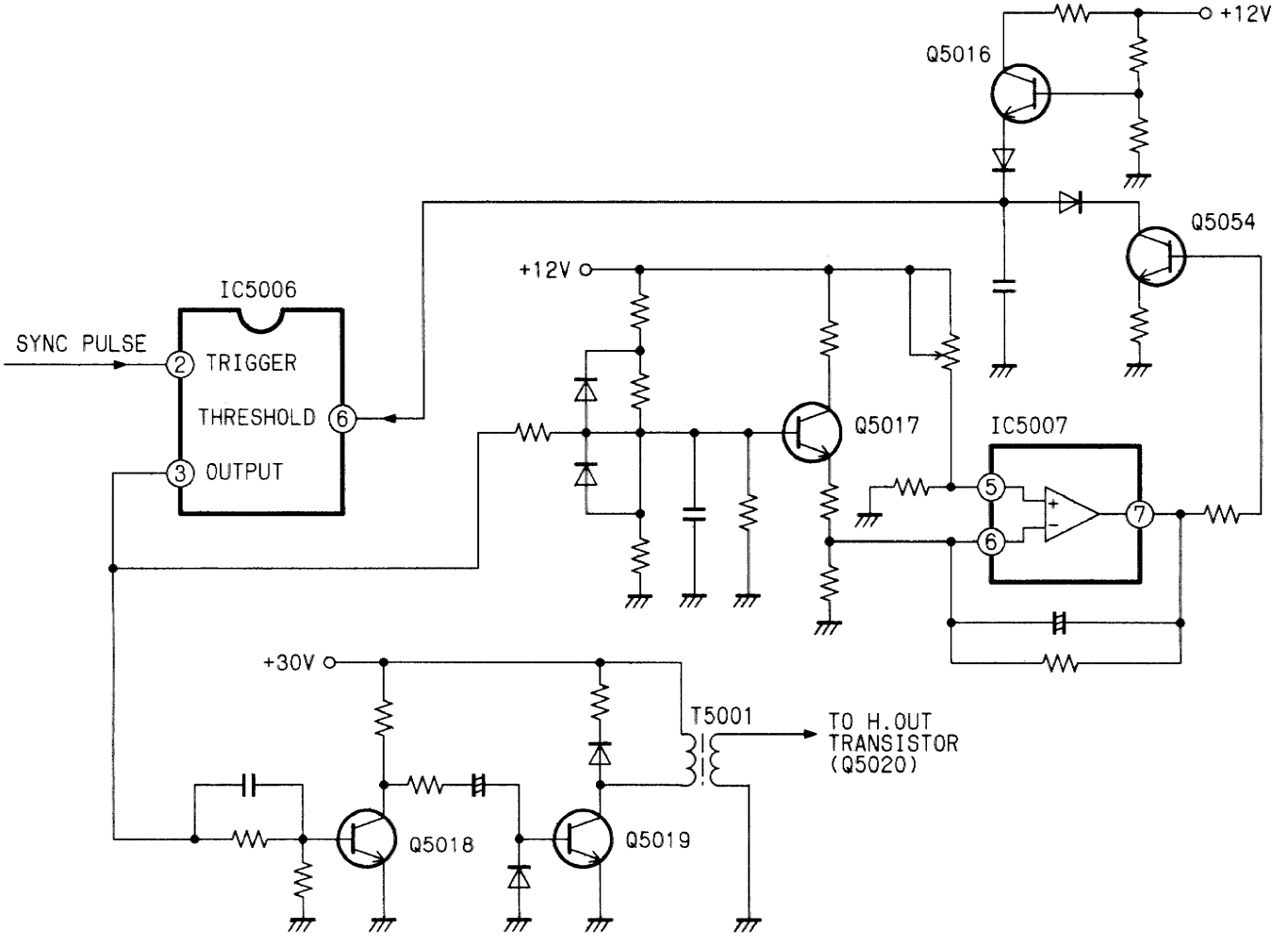


Fig. 64

IC5006 ③ →Q5017→IC5007→Q5054→IC5006 ⑥ make up a closed loop, and they control the driving transistor Q5019's driving pulse at a constant duty independent of the input frequency (f_H).

Driving pulse to Q5019 (driving transistor)

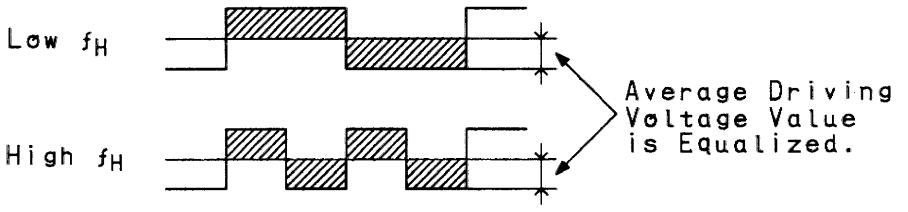


Fig. 65

4. Amplitude Control Circuit

This circuit controls the deflection current that flows in accordance with the input frequency (f_H) to maintain the screen display area almost constant even when f_H fluctuates. Two circuit elements are used to achieve this. One is a down chopper circuit which causes +B voltage that depends on f_H to be added to the choke coil or the horizontal transistor so that a nearly constant current flows through the deflection coil. The second element is an amplitude control circuit which stabilizes the +B voltage.

Notes:

*1. Deflection current = +B voltage (horizontal output collector voltage) / [deflection coil inductance (constant) x f_H]

Examples: If f_H = 15 kHz, +B ≒ 40V

If f_H = 37 kHz, +B ≒ 90V

*2. The figure below shows a sample deflection current waveform. When the deflection current is constant, the higher the frequency, the shorter is the display time as shown by t_s' (t_2 = t_1 = constant). In some causes, some display signals may not appear on the screen. Thus, the deflection current level must be varied in accordance with f_H.

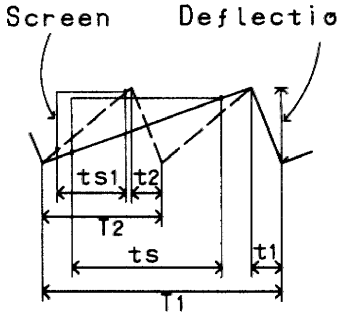


Fig. 66

t_1 = t_2 (constant)

T_1 = one cycle when f_H is low

T_2 = one cycle when f_H is high

ts1 and ts' are the signal display times, and their ratio is approximately 70% ~ 80% of the scanning line.

Circuit Operation

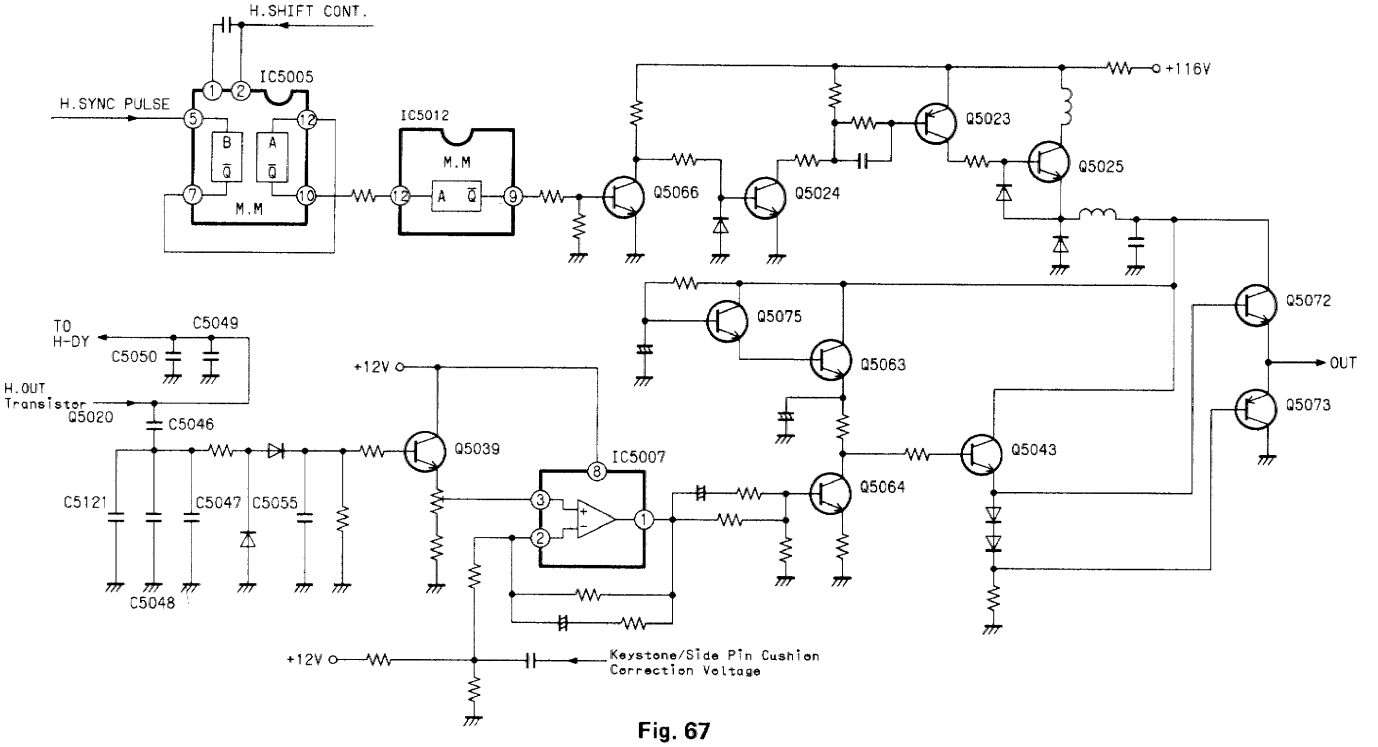
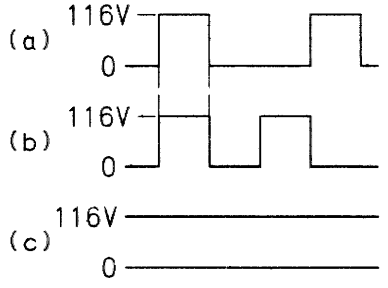


Fig. 67

The mono-multi vibrator circuit made up of IC5005 and IC5012 generates a pulse with constant width for driving the down chopper circuit. By maintaining the driving pulse width constant, the voltage control according to f_H can be performed efficiently. (IC5005 has the H. SHIFT function.)



Q5025's emitter voltage waveform

f_H (a) < f_H (b) < f_H (c)

Fig. 68

Q5072's collector voltage is varied within the range of approximately 40V to 90V according to f_H. Q5072 and Q5073 perform as the regulator transistor that controls the voltage supplied to the horizontal choke coil.

Horizontal pulse dividing capacitors (C5046 ~ C5048 and C5121) are provided on the collector side of H. OUT transistor (Q5020) to enable detection of the horizontal pulse amplitude. After peak hold and DC conversion by C5055, etc., the detection signal is added to ③ of IC5007 (differential amplifier for error detection). Then it is compared in IC5007 to the reference voltage that is applied to IC5007's ② to obtain the error voltage. Keystone correction and side pin correction voltages are added to the reference voltage. The error voltage is amplified by Q5064, and Q5043 drives the push-pull circuit made up of Q5072 and Q5073. The output of this push-pull circuit is supplied to the horizontal choke coil for horizontal amplitude, side pin cushion and keystone control.

5. Keystone Correction Circuit

Keystone correction level is controlled in such a way that Keystone distortion does not occur when f_H fluctuates. Amplitude control function controls the +B voltage in accordance with f_H' but the size of the V. SAWTOOTH waveform for Keystone distortion correction is controlled in a manner that follows the +B voltage fluctuation (i.e., the size of V. SAWTOOTH waveform added to the reference voltage is varied according to the level of +B voltage).

Circuit Operation

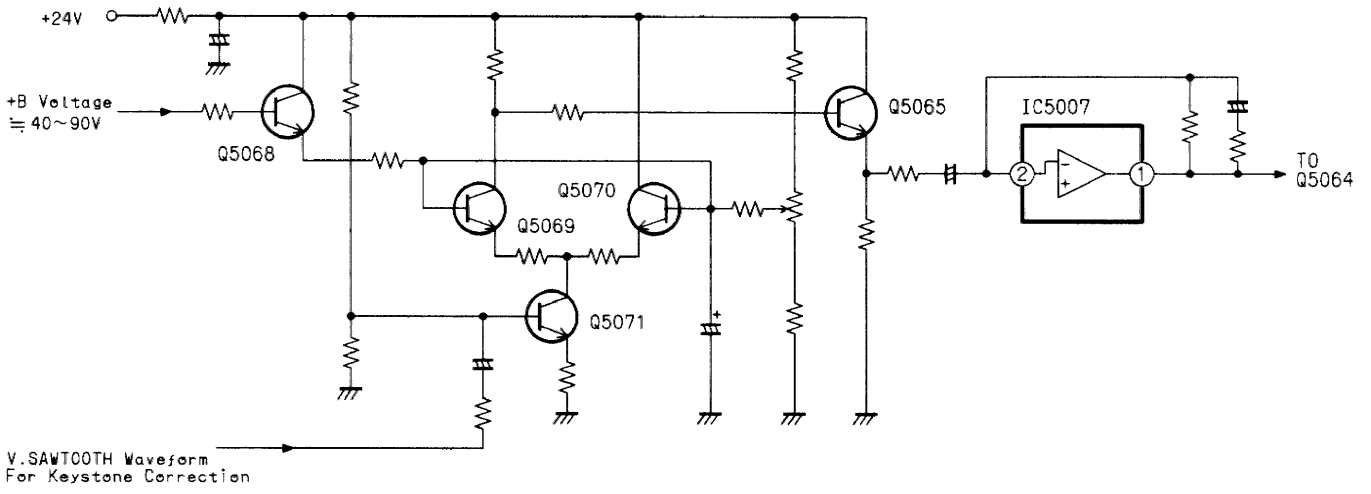


Fig. 69

With Q5057 base voltage becoming the reference voltage and Q5069 base voltage fluctuating in accordance with +B voltage fluctuations. Q5071's emitter potential fluctuates according to the V. SAWTOOTH waveform that is applied to Q5071's base, causing the voltage difference [V. SAW + (+B voltage)] in the differential amplifier made up of Q5069 and Q5070 to be retrieved from Q5069's collector and added to Q5065's base.

6. Horizontal Linearity Correction Circuit

A coil designed to cause inductance to change in accordance with current changes has been added to the conventional linearity correction coil to provide a linearity correction circuit that responds to f_H fluctuations.

Current/Inductance Converting Coil Characteristics

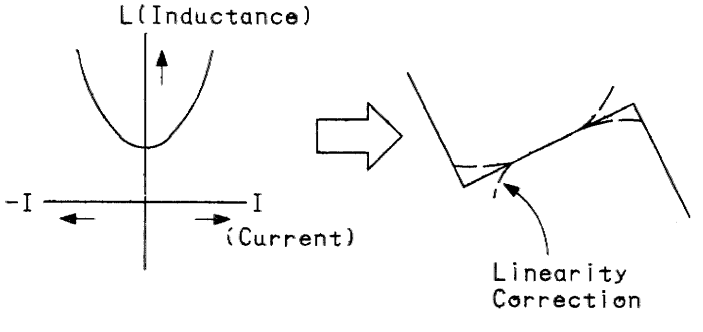


Fig. 70

Circuit Operation

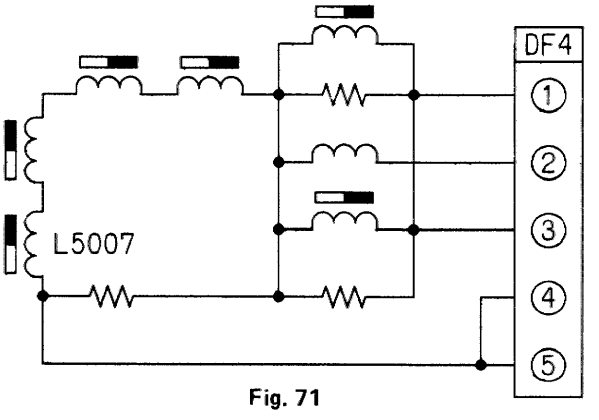


Fig. 71

Note: L5007 is the current/inductance converting coil.

7. Protection Circuit

D-board includes an abnormal condition detection circuit which is a part of the protection circuitry against abnormal operation. The abnormal conditions detected by this circuit are H. deflection and V. deflection circuit abnormalities.

Circuit Operation

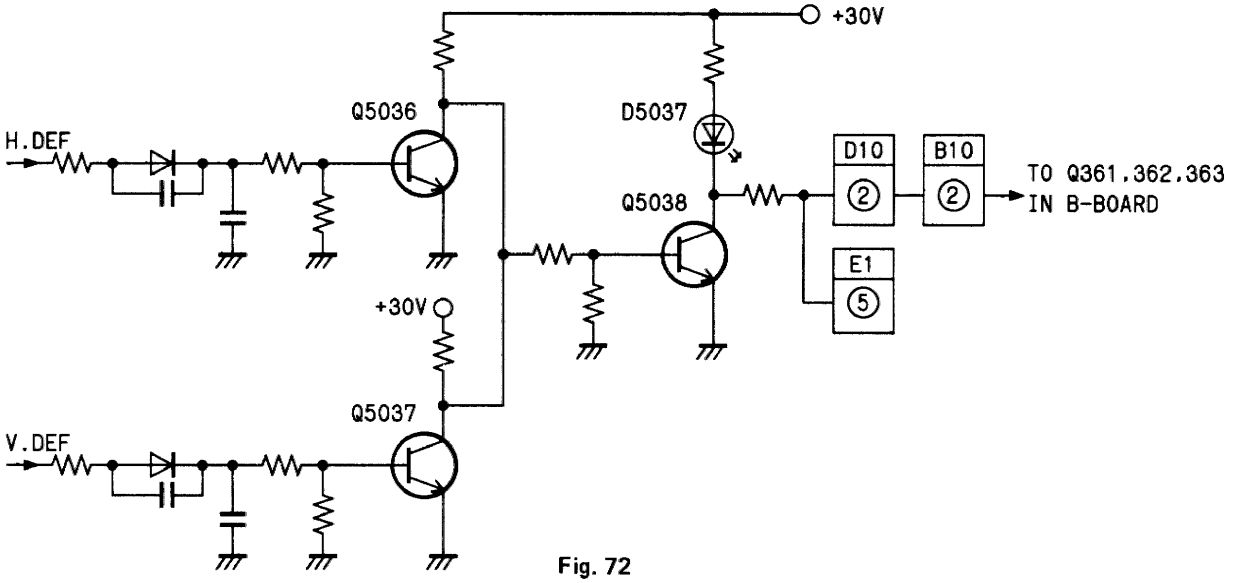


Fig. 72

Q5036 detects the horizontal amplitude and switches OFF when the amplitude drops to approximately 1/2. Q5037 detects the vertical amplitude and switches OFF when the amplitude drops to approximately 60%. Thus, Q5058 switches ON when either or both Q5036 and Q5037 switches OFF to detect an abnormal condition. When this occurs the LED D5037 turns ON.

8. Control VRs

The following table lists the adjusting VRs (for use by servicing personnel) in the H. deflection circuit:

Mode	Description	VR NO.
VIDEO	H. SIZE	R5116
RGB1	H. SIZE	R5113
RGB2	H. SIZE	R5120
NTSC	H. HOLD	R5220
PAL/SECAM	H. HOLD	R5221

VI. VERTICAL DEFLECTION CIRCUIT (A-Board)

1. Block Diagram

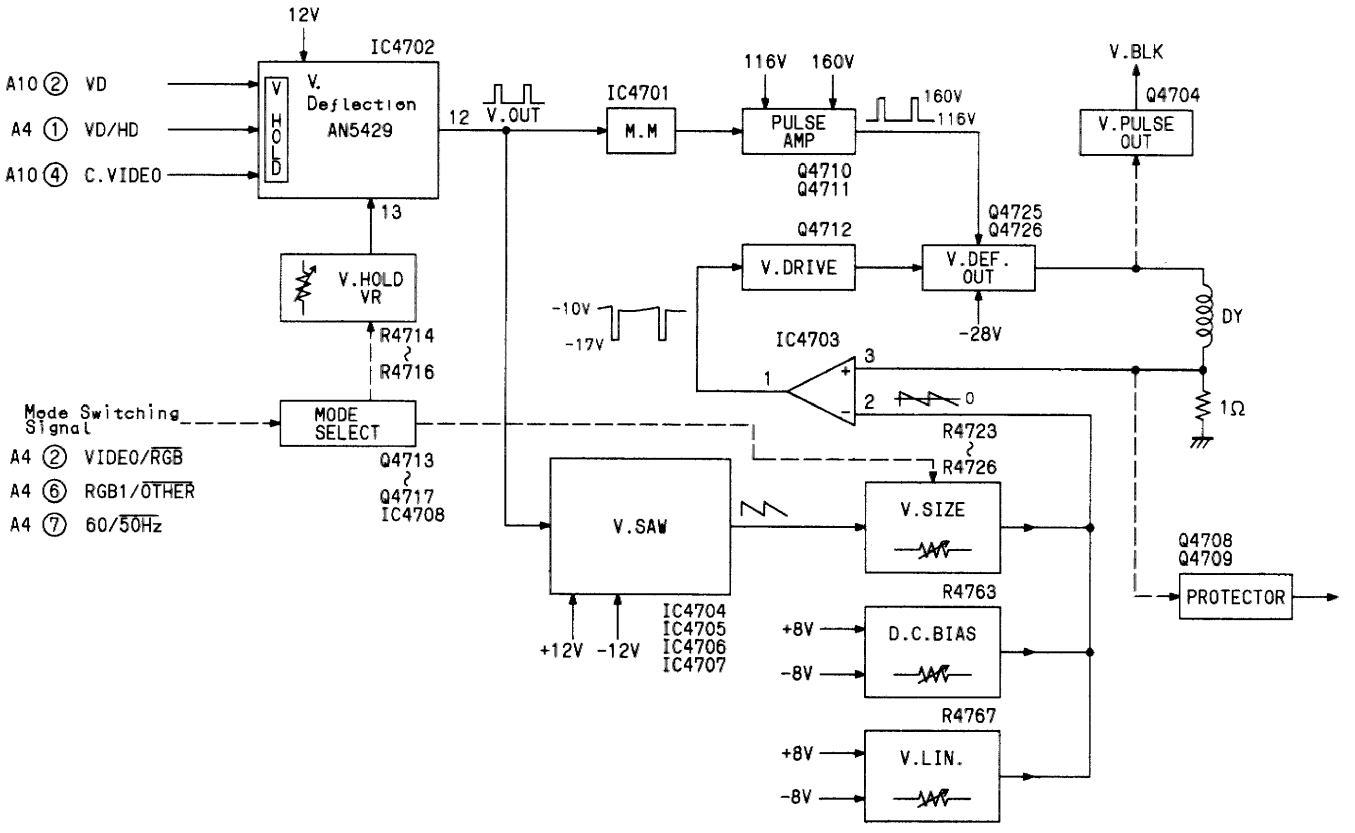


Fig. 73

2. SYNC Separation and Synchronization Circuits

A circuit configuration that can support the different inputs of separate V. SYNC and composite SYNC (H/V) in the RGB mode and composite video (H/V/SIGNAL) in the VIDEO mode is used.

The lock-in ranges on V. SYNC are as follows:

Separate SYNC . . . . . .50 ~ 100 Hz
Composite SYNC . . . . . .50 ~ 100 Hz
Composite VIDEO. . . . . .50 or 60 Hz

Circuit Operation

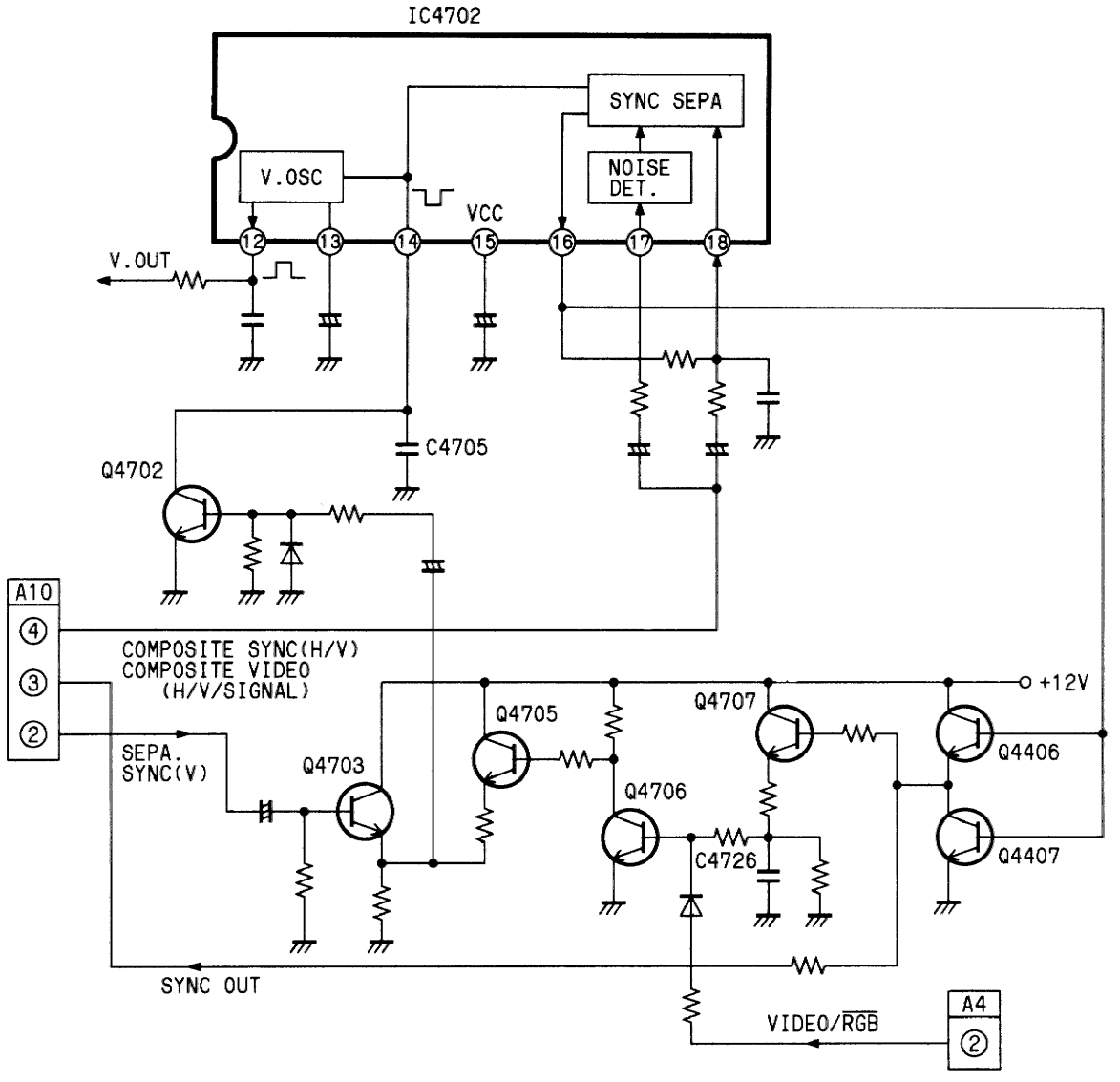


Fig. 74

In the case of separate SYNC, C4705 is discharged by ON/OFF operation of Q4703 and Q4702 to achieve V. synchronization. In the case of composite VIDEO (H/V/SIGNAL) mode, the input signal goes to IC4702's ⑱, passes through the SYNC separation circuit in IC4702, and the V. component discharges C4705 which is connected to ⑭ to achieve V. synchronization. In the case of composite SYNC (H/V), the input signal goes to ⑱, and SYNC (H/V) is outputed by the SYNC separation circuit to ⑯. The circuit segment made up of Q4705 ~ Q4707 is the H/V separation circuit, and it extracts only the V. SYNC component from the SYNC signal output from IC4702's ⑯. This V. SYNC signal travels via Q4702 to discharge C4705 and achieve V. synchronization.

VIDEO/RGB control signal is applied to Q4706's base to isolate the H/V separation circuit and the Q4702 circuit in the VIDEO mode.

Note: For the H/V separation circuit (Q4705 ~ Q4707), R4770 and C4726 serve as the V. SYNC extracting integration circuit.

3. Vertical Sawtooth Generation Circuit

The +V. and −V. SAWTOOTH waveforms for convergence corrections are also generated within the A-board. This is done using the V. OUT (V. SYNC) pulse output from IC4702's ⑫ . Constant amplitude (independent of f_V) V. SAWTOOTH waves are generated by maintaining constant V. SIZE by open loop circuit configuration.

Circuit Operation

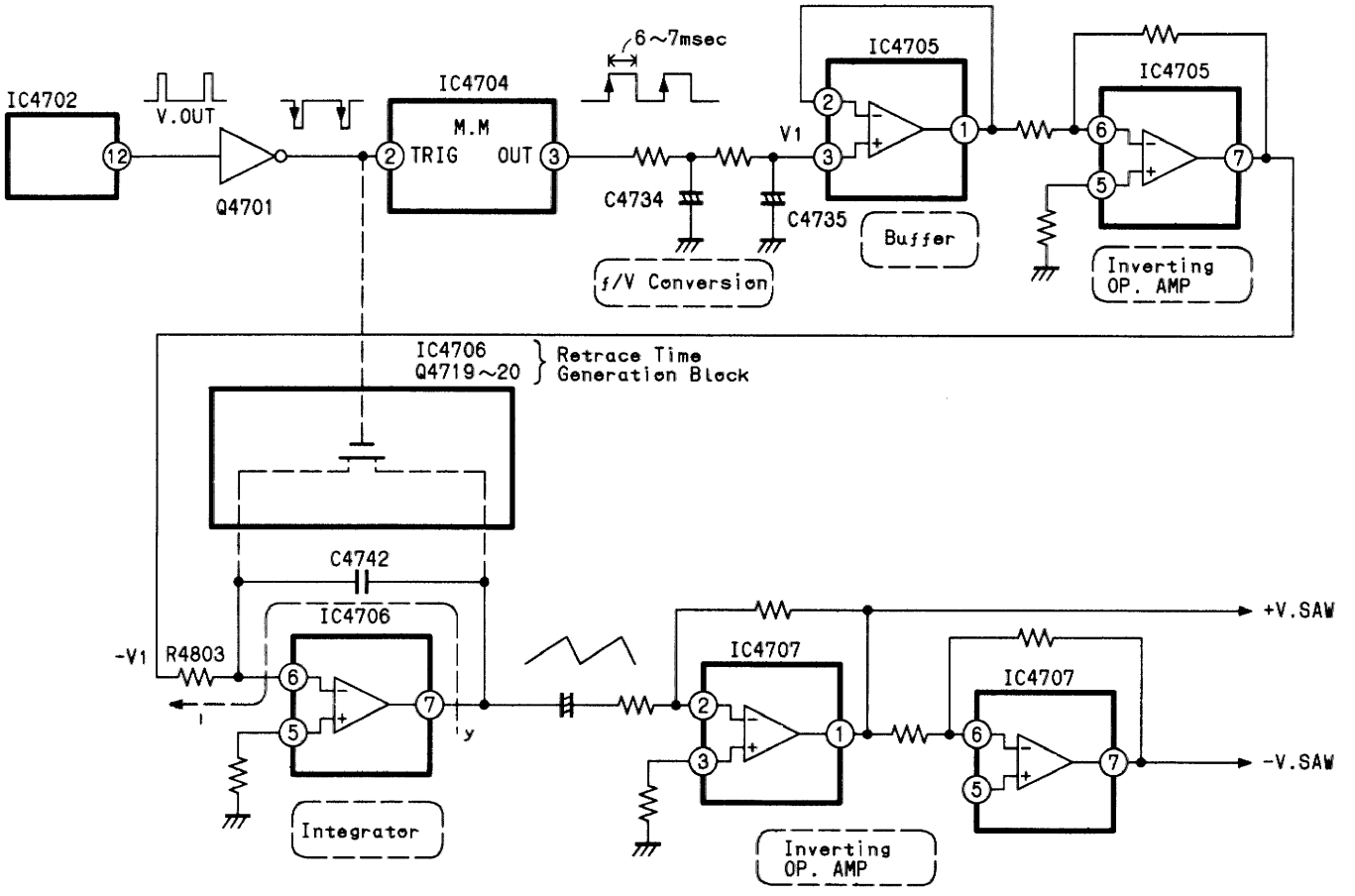


Fig. 75

The V. OUT signal outputed from IC4702's ⑫ goes to Q4701 and IC4704's ②. IC4704 is a mono-multi IC, and it generates constant width pulse (6 ~ 7 msec.) . This pulse signal is smoothed by C4734 and C4735, and then f_V to DC voltage conversion is performed to generate V_1. V_1 is inverted by IC4705's ⑤ ~ ⑦ to generate $0V_1$. Then, the integration circuit made up of R4803 and C4742 generates V. SAWTOOTH wave (scanning portion of V. deflection) (y). The circuit segment consisting of IC4706 and Q4719, Q4720 is the retrace time generation block, and it generates the retrace portion by discharging C4762 by the V. SYNC signal output from Q4701.

The signal from IC4706's ⑦ is inverted to output +V. SAWTOOTH and −V. SAWTOOTH waveforms.

Note: Constant V. SIZE operation = y

$y = (1/CR)\ (V_1T) = (1/CR)\ (V_1/f_V)$

f_1/f_V = constant ⟹ y = constant

* $T = 1/f_V$
* C = C4742
* R = R4803
* V_1 = function of f_V (Large if f_V is high; Small if f_V is low)

4. Vertical Pulse Amplification circuit

To shorten the retrace time for vertical deflection, the convertional single power supply (+B voltage) method was changed to the dual power supply method. The new method supplies +160V during retracing and +116V during scanning.

Circuit Operation

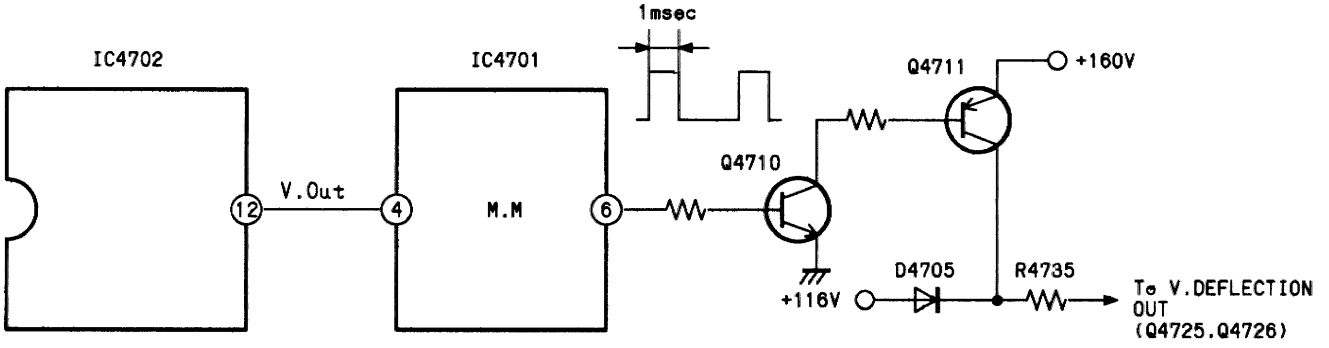


Fig. 76

The V. OUT signal from IC4702's ⑫ goes to IC4701 (mono-multi) to adjust the pulse width to the constant value (1 msec). This pulse width is used as the retrace time to turn Q4710 ON and cause +160V to be applied to R4735. The time when Q4710 is OFF is treated as the scanning time, and +116V is applied to R4735 during this time.

5. Vertical Deflection Output Circuit

This output circuit is a closed loop circuit that uses operational amplifier (differential amplifier) to control V. deflection according to the input signal (f_V) and installation condition (e.g., ceiling mounted, floor setting, etc.)

Circuit Operation

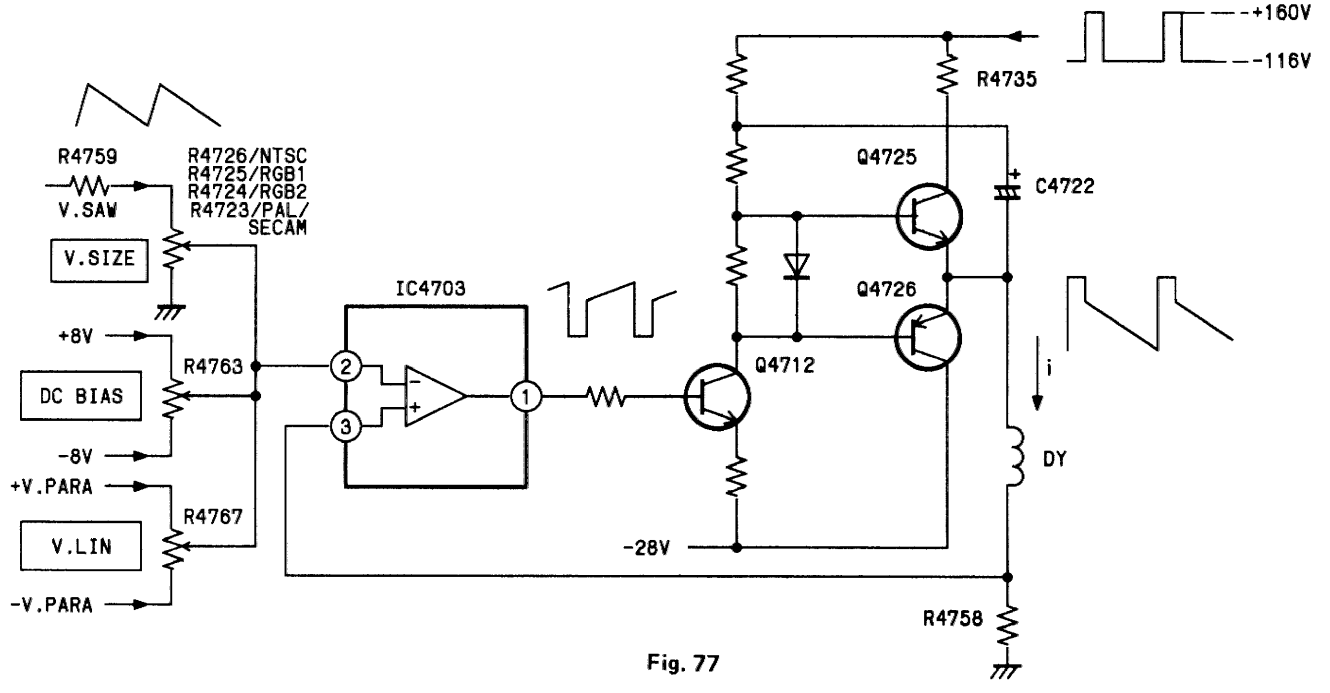


Fig. 77

Reference signal made up of V. SIZE, DC BIAS and V. LIN waveforms and voltage all superimposed on each other is applied to IC4703's ② and compared with the signal from the deflection current (input to ③) monitor resistor R4758. Loop control is performed to match ② and ③. C4722 is a boost trap capacitor to accelerate rise of DY application voltage during retrace time.

Note: i waveform (deflection current waveform)

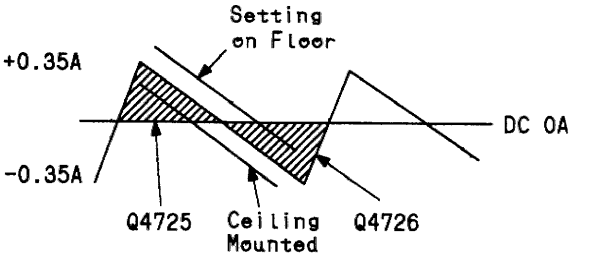


Fig. 78

6. Protection Circuit

An abnormal condition detection circuit is included in the A-board to stop high voltage application when vertical amplitude becomes too small to prevent burning the CRT.

The protector is sctivated when the V. SIZE drops to approximately 55%.

Circuit Operation

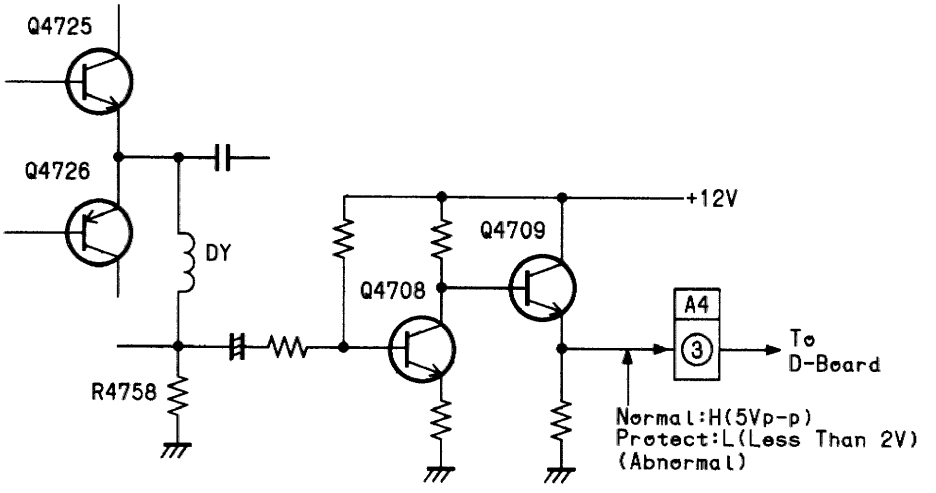


Fig. 79

VII. HIGH VOLTAGE CIRCUIT (E-Board)

1. Block Diagram

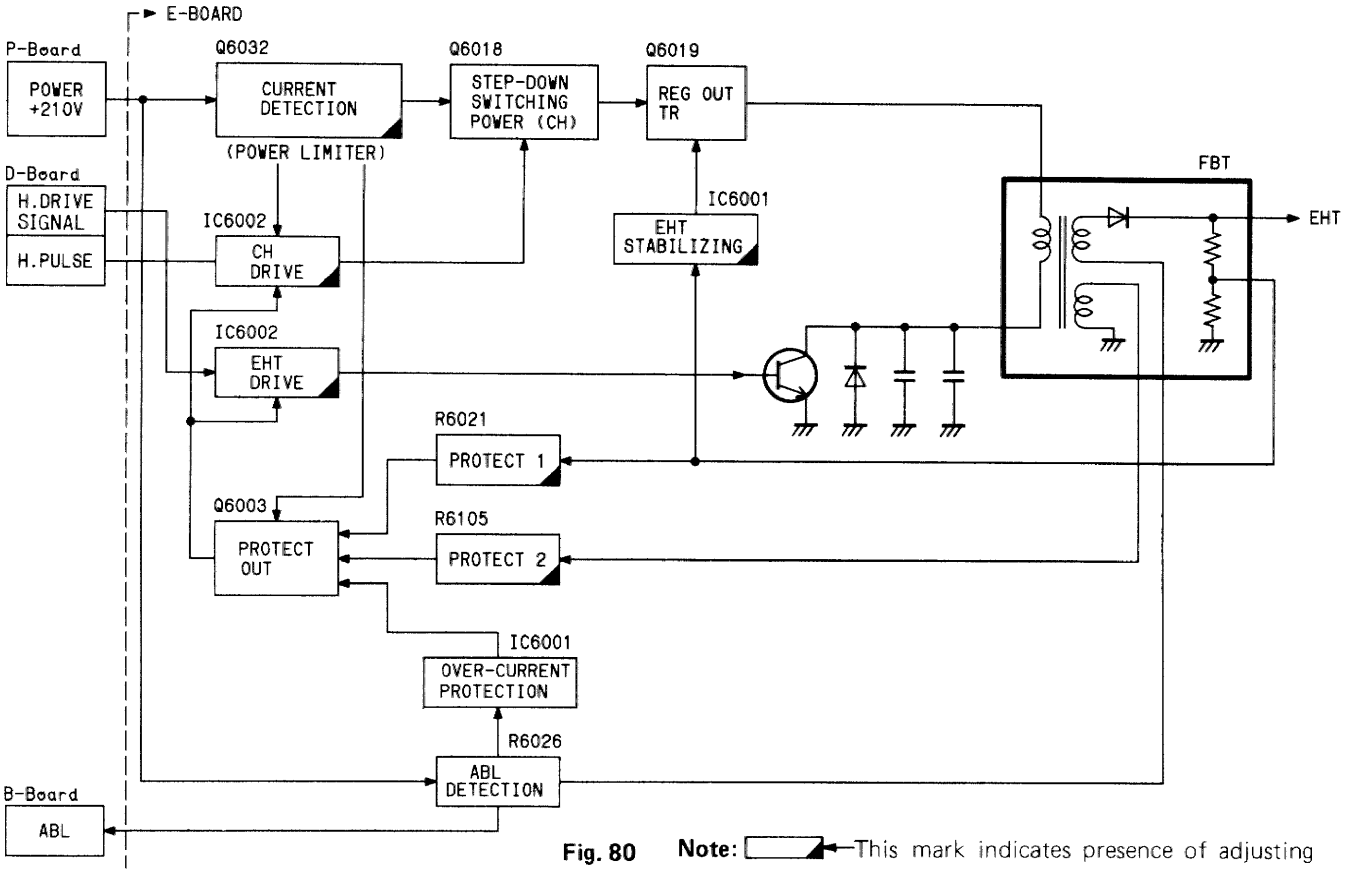


Fig. 80 **Note:** ▭◀ This mark indicates presence of adjusting VR for "factory adjustment only".

2. Overview of High Voltage Circuit

Differences from conventional high voltage circuit:

New features: ① Automatic adjustment to f_H in the range of 15 ~ 37 kHz. [F.B.T. switching pulse is used, but +B voltage is varied according to frequency to maintain constant high voltage (when +B voltage and F.B.T.'s L is kept constant, high voltage level drops if f_H rises).]

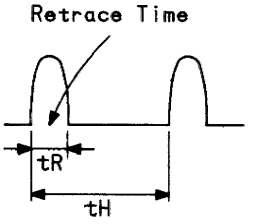


Fig. 81

② High voltage drive OFF time is maintained constant regardless of f_H value.

Note: Relation between high voltage and f_H:

$$\text{High voltage} \fallingdotseq \frac{+B \cdot \left(\frac{t_H}{t_R}\right)}{\sqrt{L.C}} \fallingdotseq \frac{+B \cdot \left(\frac{1}{f_H}\right)}{\sqrt{L.C}}$$

* Variable +B method is used.

Performance improvements:

① Improved dynamic regulation (raster distortion). [Implemented by changing high voltage capacitor from 1500pF to 5500pF and using a power limiter circuit.)

② Use of LED in protector circuit. (LED lights up when the protector is activated.

3. Power Limiter Circuit and Down Chopper Circuit

These circuits monitor and contol power consumption (beam current level) to a load factor within certain level so that raster distortion will not occur. The control method used is monitoring of current (on FBT's primary side) (by linked operation of the current detection circuit with a mono-multi circuit and down chopper circuit). Linked operation of the mono-multi circuit and the down chopper circuit also generates the +B voltage whose level is tied to f_H.

Circuit Operation

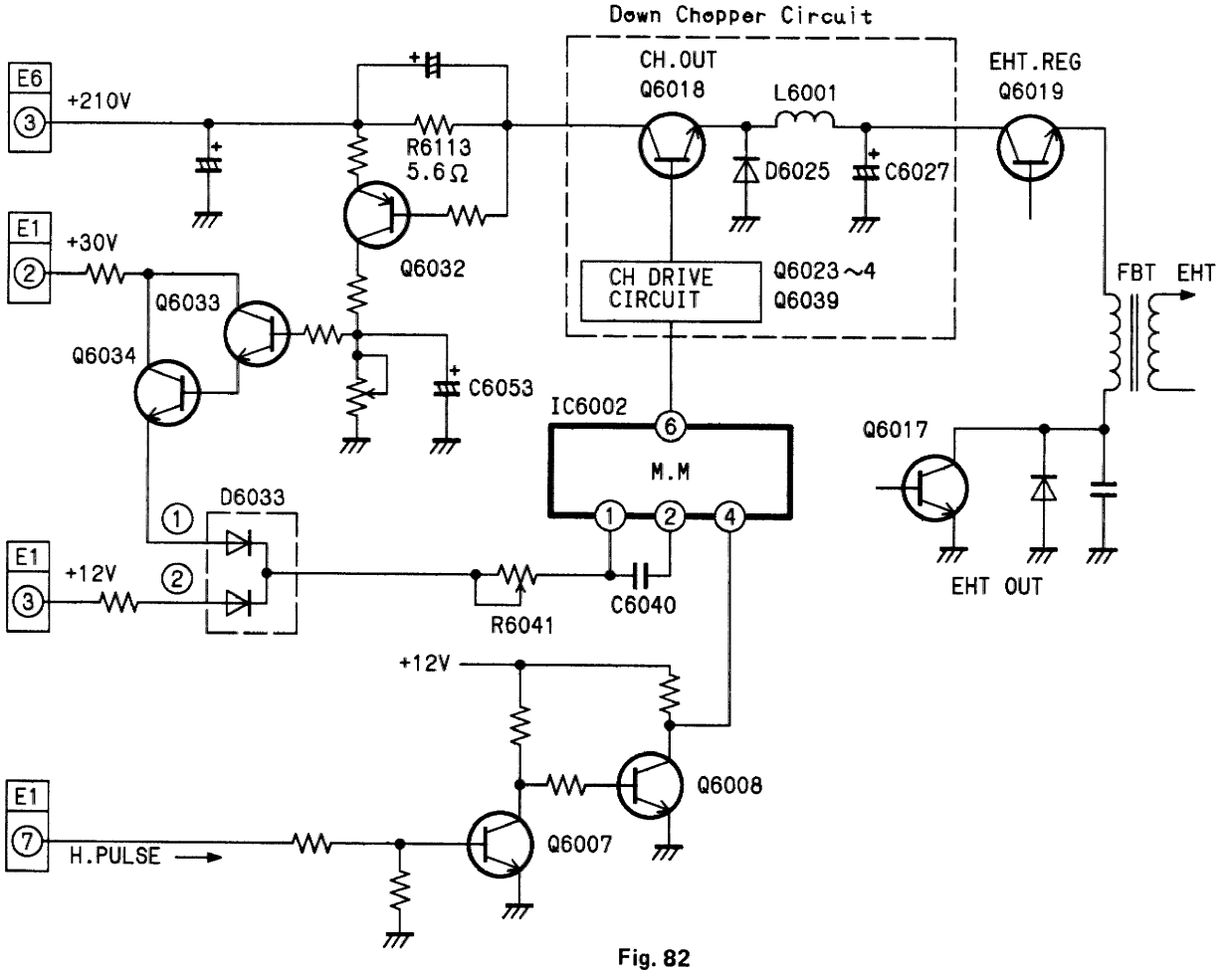
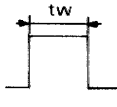


Fig. 82

- When the 210V P_W is small

The pulse width t_W () of output from ⑥ of IC6002 (mono-multi) is determined by D6033's ② side +B voltage and the time constant of R6041 and C6040. The period of the H-pulse that is input to IC6002's ② depends on f_H, but the width t_W of the pulse output from ⑥ is independent of f_H (period will be different). The down chopper circuit is driven by the pulse from IC6002's ⑥, and the output voltage is used as the +B voltage of the EHT regulator transistor. Therefore, the down chopper output voltage varies depending on the duty ratio of the output waveform from IC6002's ⑥.

t_W	Down chopper ON duty	Output voltage	
Broad	Large	Large	When f_H is constant and t_W fluctuates.
Narrow	Small	Small	
f_H	Down chopper ON duty	Output voltage	
High	Large	Large	When t_W is constant and f_H flucutates.
Low	Small	Small	

- When the +210V P_W reaches 90W (upper limiting power level) (current through R6113 reaches 0.43A)

The voltage waveform generated by the current flowing through the current detection resistor R6113 (5.6Ω) is amplified by Q6032 and then rectified by C6053. If P_W on the +210V line rises to 90W, the C6053 rectified voltage level rises and is supplied via Q6033 → Q6034 → D6033's① to R6041. This raises C6040's integration rate and shortens t_W (⊢tw⊣), causing the down chopper output voltage to fall which reduces power consumption loss through the EHT regulator. This results in reduction of P_W, thereby controlling P_W on the +210V line at no more than 90W (current through R6113 is controlled at 0.43A maximum).

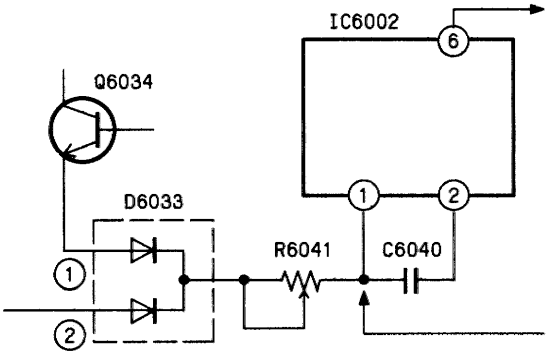


Fig. 83

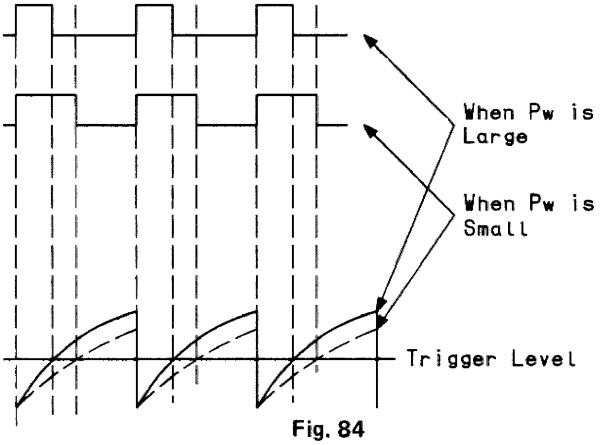


Fig. 84

How the power limiter circuit improves the raster distortion characteristic

1. Principle of raster distortion correction

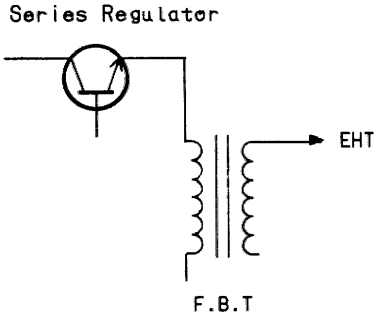


Fig. 85

As the beam current rises, high voltage output power rises and the high voltage level drops. At this point, the series regulator's emitter voltage goes up to raise the high voltage level to offset its fall and prevent raster spreading. The size of the series regulator's required emitter voltage rise is proportional to the high voltage output power up to the maximum collector voltage. Thus, the maximum high voltage output power value while still maintaining the high voltage level stability can be raised by raising the series regulator's $V_{C\text{-}E}$ voltage.

2. Why raster distortion still occurs when raster distortion correction is performed using a series regulator ?

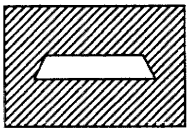


Fig. 86

In case of window pattern signal as illustrated at left involving an average beam current that is not large enough to activate the ABL circuit but the cathode driving is at maximum, the instantaneous high voltage output power for the brightness section becomes maximum and the series regulator's $V_{C\text{-}E}$ voltage becomes saturated, making it impossible to perform high voltage correction and causing the high voltage level to drop and raster to spread.

3. How the power limiter circuit improves raster distortion ?

Raster distortion on the window pattern described above can be improved by simply raising the series regulator's collector voltage, but that will increase the supply power level when the average beam current is at maximum because the series regulator's loss increases. The power limiter circuit improves the raster distortion problem without increasing the series regulator's loss. As described above, the series regulator's voltage is high, the average beam current is large and the series regulator's loss is large for a pattern that requires small average beam current and the series regulator's loss is small but raster distortion is significant. But, for a pattern that does not cause significant raster distortion, the series regulator's collector voltage drops (because the ABL circuit is activated and the cathode driving is suppressed) so that raster distortion can be corrected without having to increase the supply power level (to compensate for series regulator's loss).

VIII. POWER SUPPLY CIRCUITS (K-, P1-, P2-, P3-Board)

1. Block Diagram

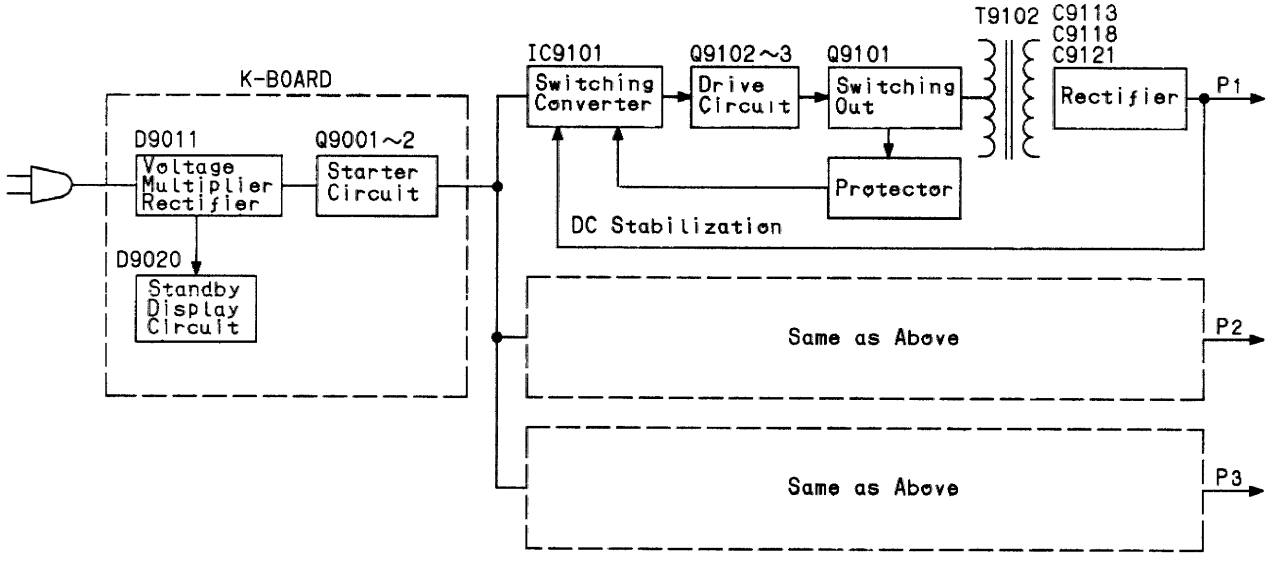


Fig. 87

2. Features

The basic circuitry is same as that used in the PT-101 series models. The differences are as follows:

① AC rectifying method. . . . .Voltage multiplying rectification

② Free-run (non-synchronized) method . . . . . .63 kHz switching frequency is raised to achieve compact design.

③ Three internal switching converters

④ Standby display and operating status display using 2-color LED unit.

– Standby display . . . . . .Red

– Operating status display. . . . . .Green

3. Switching Converter Circuit (IC9101)

① 63 kHz oscillation circuit

AN5905S in each of IC9101, IC9201 and IC9301 (THH11505AZ) has a PLL oscillator circuit built-in, and the resistance between ⑰ and Vcc is functionally trimmed within the IC to set the free-run frequency at 62.936 kHz.

The ㉒ terminal (trigger terminal) of IC9101 (as well as IC9201 and IC9301) is grounded to enable free-run operation.

② Soft start function

When the power switch is turned ON, the load is small so that application of broad width output pulse to the drive circuits and the output transistors (Q9102, Q9103, Q9101) could damage the transistors. Therefore, a 16V/10μF capacitor is connected to AN5905S's ②, and its charging process is used to narrow the output pulse's width (because charging voltage is low when the power switch is turned ON). After a certain length of time, this capacitor's charging voltage rises to a high level, and this voltage is used to maintain a constant width of the output pulse (normal operation time).

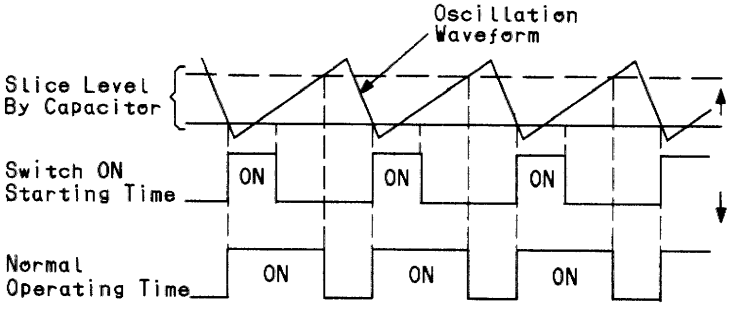


Fig. 88

4. Switching, Driving and Output Circuits

Measures are taken on these circuits, too, to avoid over-heating and under-driving of the output transistor when the voltage drops. When voltage drops, the secondary side will be exposed to a constant load so that the collector current increases. But, as long as the transistor's base current stays constant, under-driving occurs. Therefore, the base current must be varied.

Circuit Operation

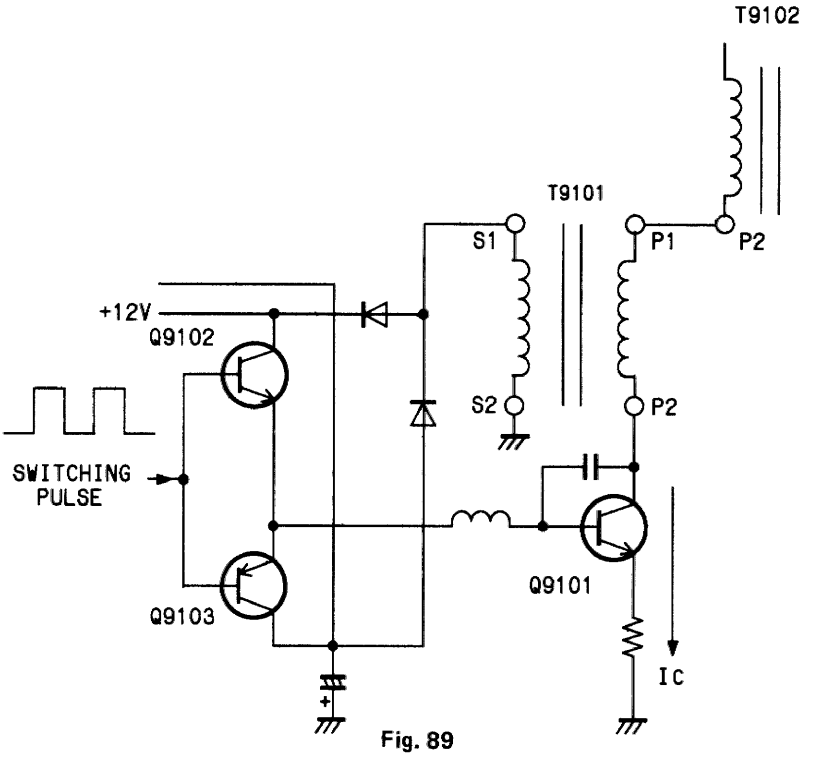


Fig. 89

The collector current that flows through the output transistor's Q9101 is detected by T9101 and feed back is applied to the base side of Q9101 via Q9102 and Q9103.

This increases Q9101's base current and makes the collector current to flow more easily, thereby preventing the transistor to overheat or becoming under-driven.

5. Protection Circuit

AN5905S in IC9101 (as well as IC9201 and IC9301) has tow types of protector circuit:

Protector 1: This circuit is activated for transient problems such as instantaneous over-loading.
It narrows the output pulse width and absorbs the abnormal voltage.

Protector 2: This circuit is activated for severe over-loading problems caused by load shorting, etc.
It stops the oscillation circuit for switching pulse generation. At the same time, it resets soft start (by discharging the capacitor for soft start).

Circuit Operation

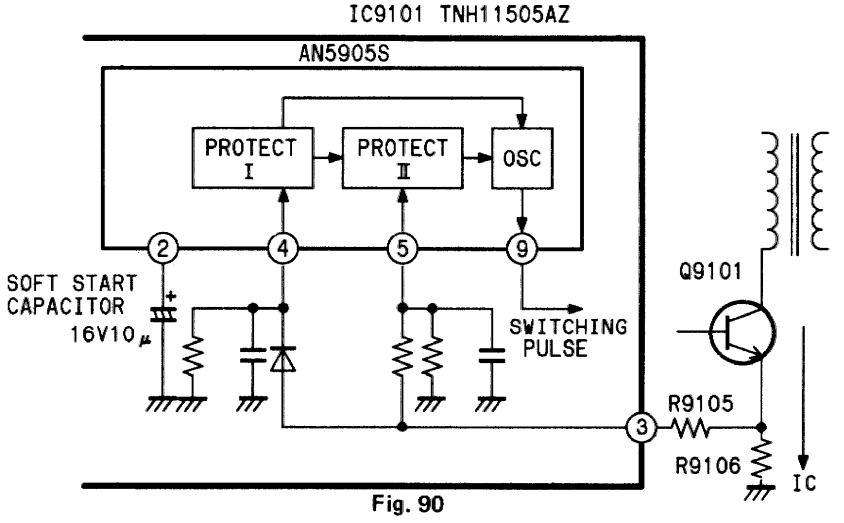


Fig. 90

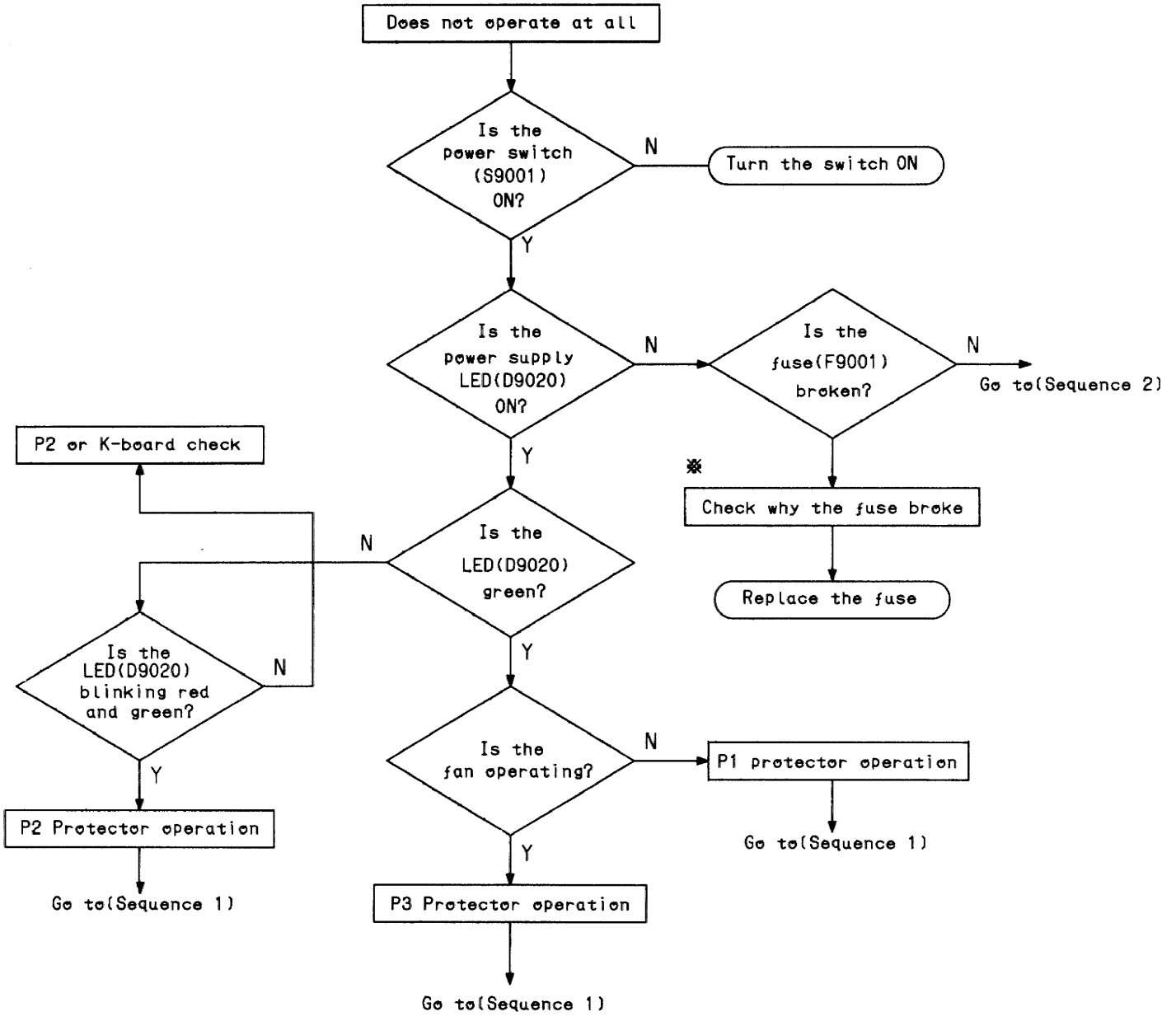
The collector current flowing through Q9101 is detected by R9106 to apply feedback to the IC9101 side to control AN5905S's oscillation circuit, thereby enabling the operations described above.

6. Listing of +B Line Voltages by Circuits

Circuit Name		P1 block	P2 block	P3 block
Horizontal deflection	Output			+116V
	Process		+15V	+30V
Vertical deflection	Output		+160V +116V	
	Process		+15V	+30V −28V +8V −9V
High voltage	Output	+210V		
	Process		+15V	+30V
Signal	4 system		+15V	
	RGB		+15V	+30V
	Output		+210V	
VM			+116V +15V	+30V
DF			+600V	+30V
Convergence				+30V −28V +8V −9V +15V
Other	Adj. lamp Fan (22) LED (green)	+16V +16V	+15V	
Maximum output power		101W	74W	114W

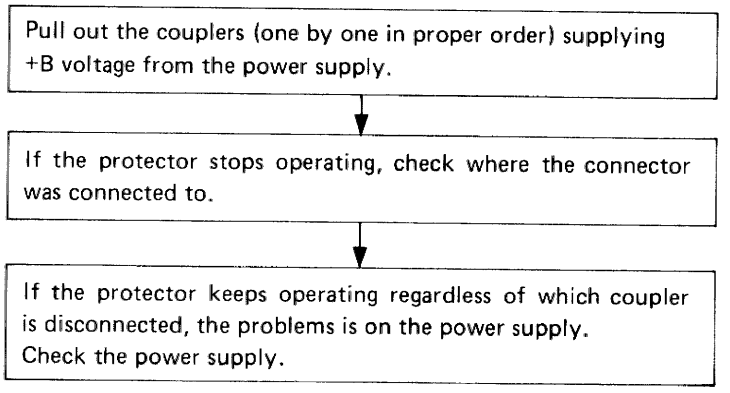
IX. FLOW CHART FOR TROUBLE SHOOTING

1. Power Supply

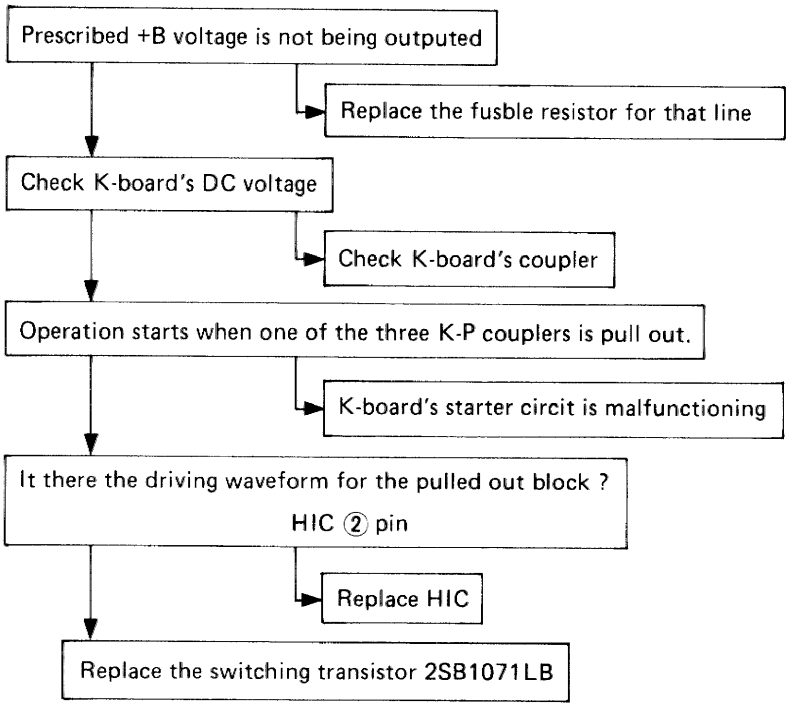


Possible cause of fuse broken
Q9101, Q9301 (Sw Tr.), Q9103, Q9303 short circuit.

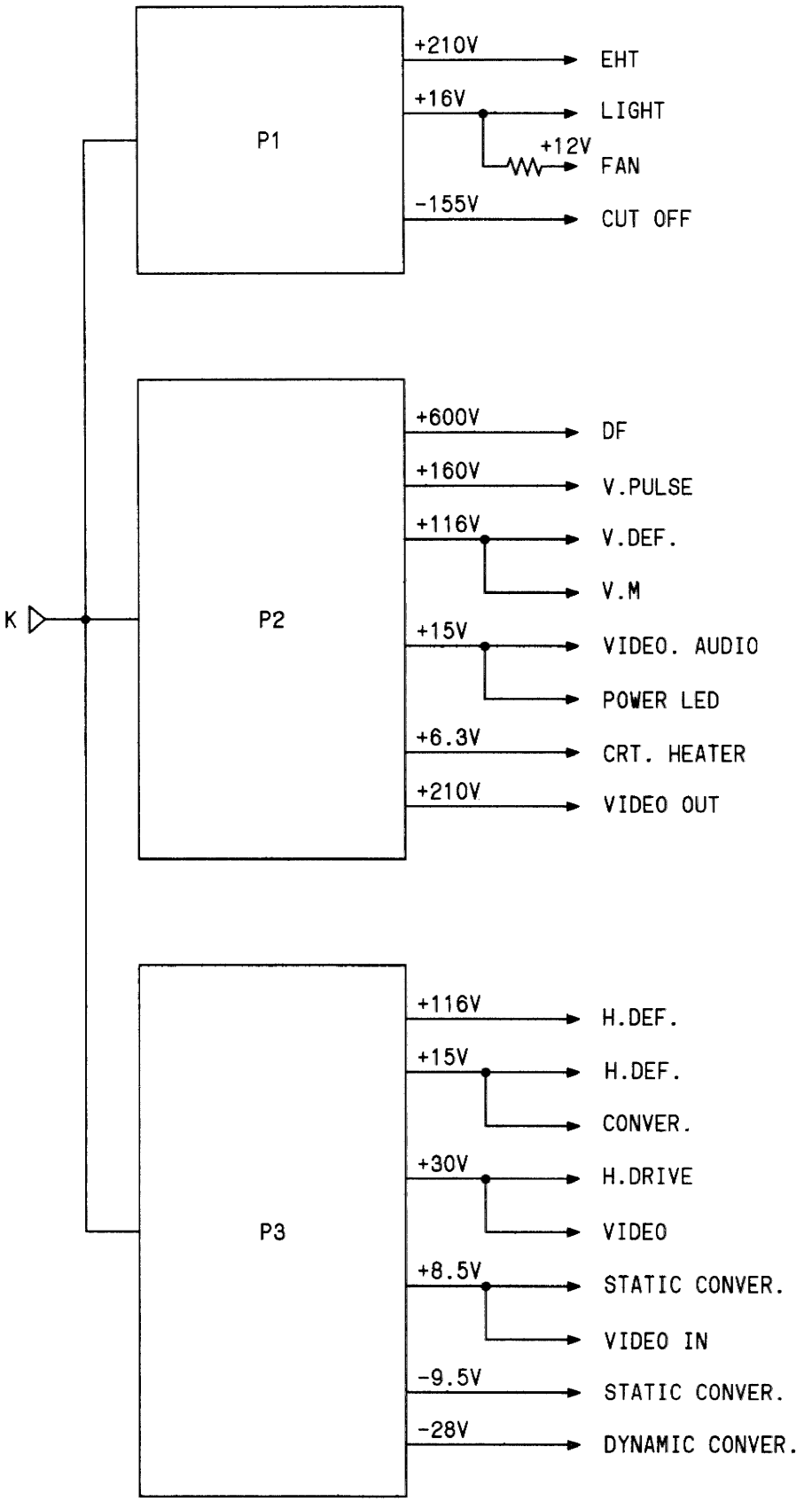
[Sequence 1]



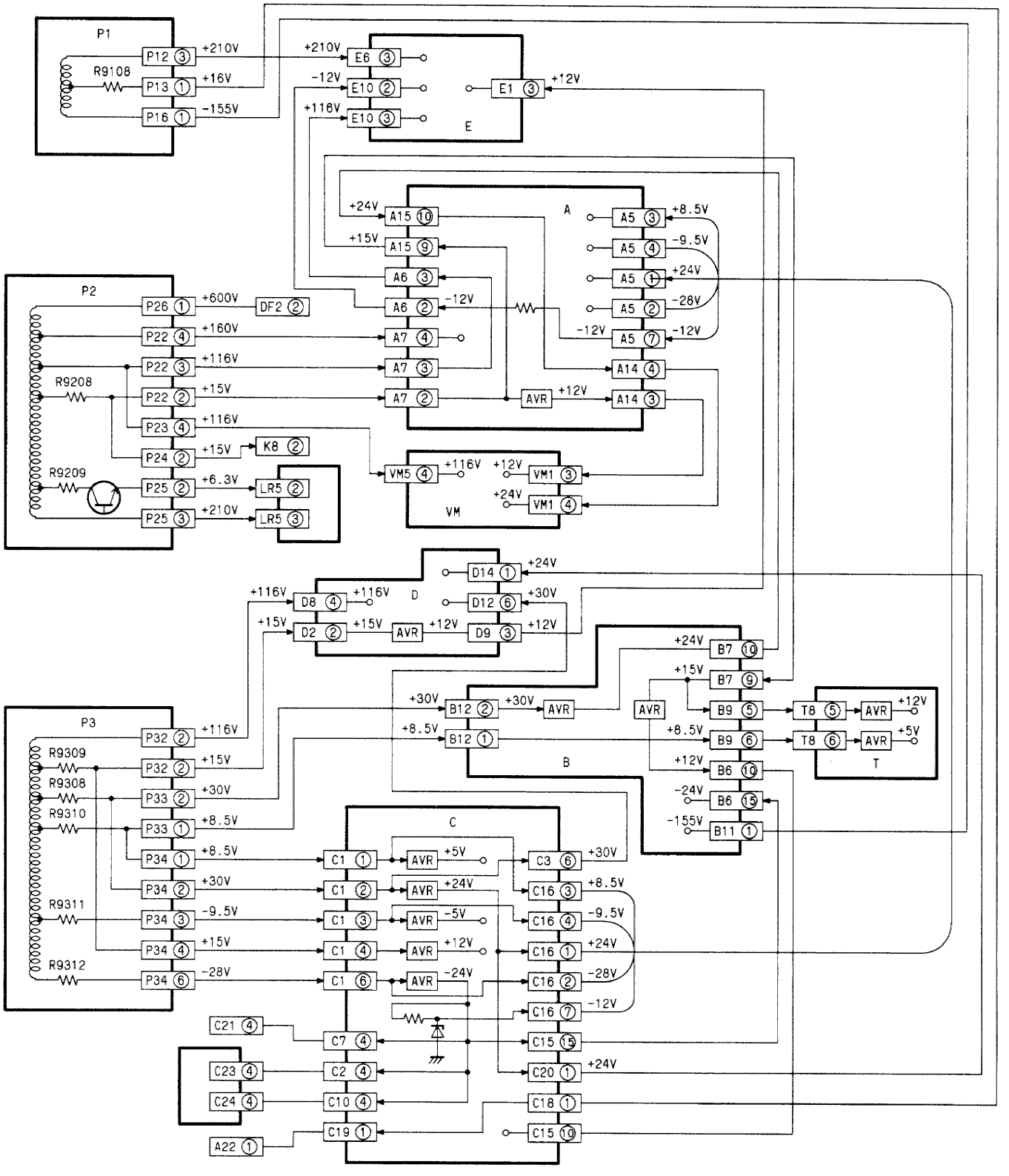
[Sequence 2]



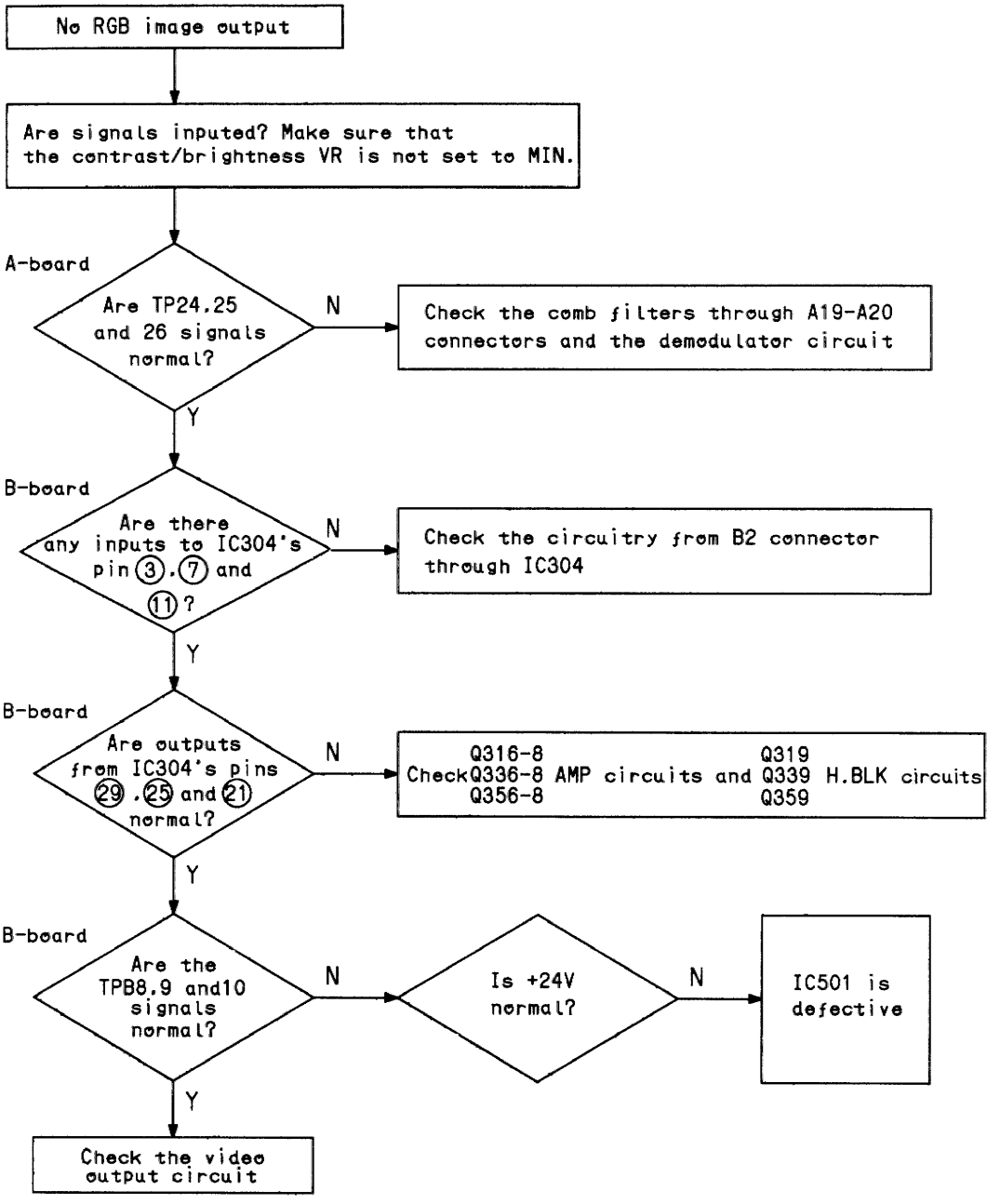
POWER SUPPLY CIRCUIT



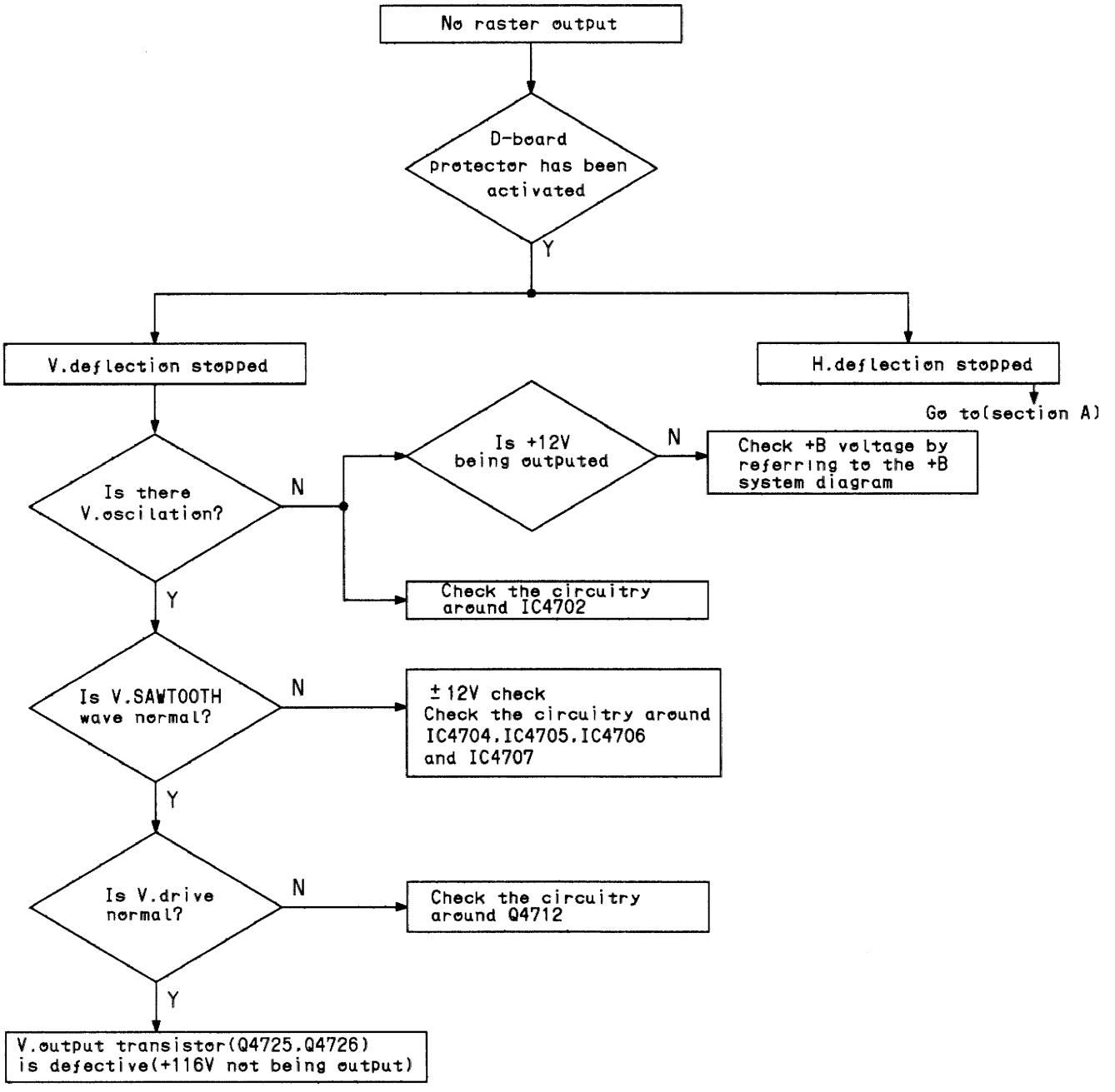
+B Voltage System Diagram



2. Signals

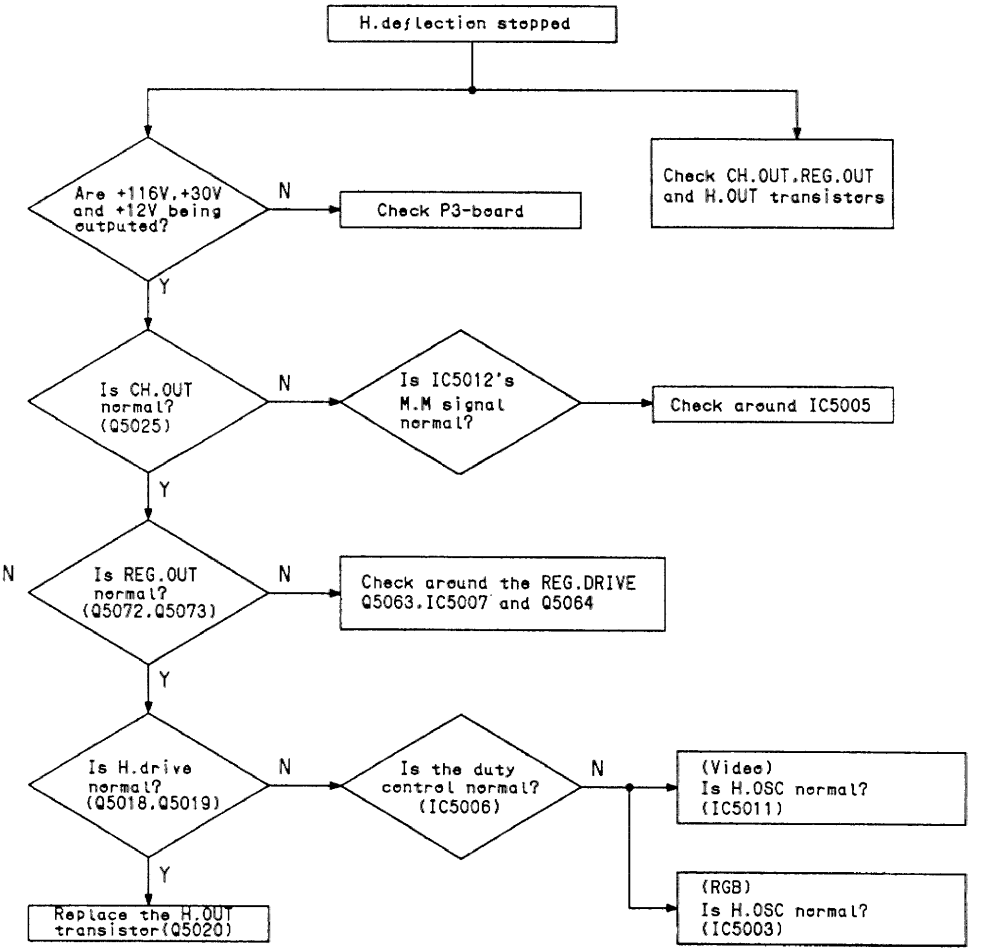

No RGB image output
Are signals inputed? Make sure that the contrast/brightness VR is not set to MIN.
A-board
Are TP24.25 and 26 signals normal?
N
Check the comb filters through A19-A20 connectors and the demodulator circuit
Y
B-board
Are there any inputs to IC304's pin ③, ⑦ and ⑪?
N
Check the circuitry from B2 connector through IC304
Y
B-board
Are outputs from IC304's pins ㉙, ㉕ and ㉑ normal?
N
Check Q316-8, Q336-8, Q356-8 AMP circuits and Q319, Q339, Q359 H.BLK circuits
Y
B-board
Are the TPB8.9 and10 signals normal?
N
Is +24V normal?
N
IC501 is defective
Y
Check the video output circuit

3. Horizontal and Vertical Deflections

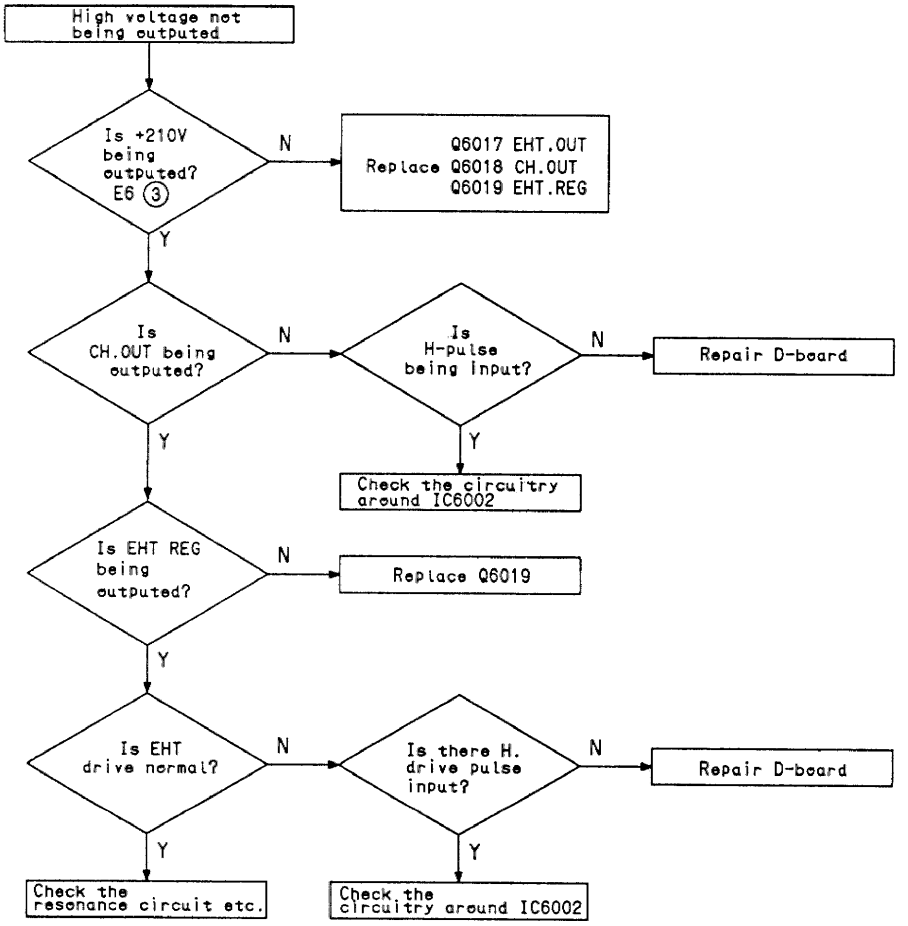


* Often, the vertical deflection problem involves the upper half portion not being outputed. This is almost always due to breakage of the 68Ω/3W fuse resistor R4735.

[Section A]



4. High Voltage



X. SCHEMATIC DIAGRAM

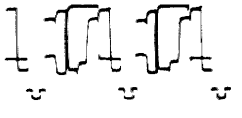
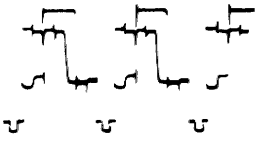
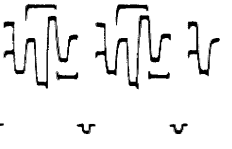
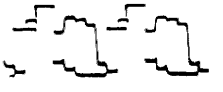
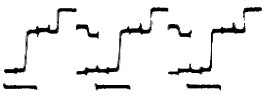
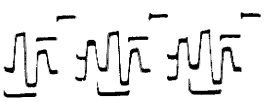
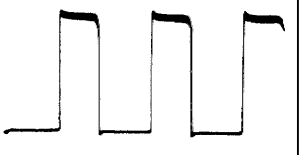
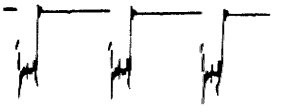
IMPORTANT SAFETY NOTICE

THE SHADED AREA ON THIS SCHEMATIC DIAGRAM INCORPORATES SPECIAL FEATURES IMPORTANT FOR PROTECTION FROM X-RADIATION, FIRE AND ELECTRICAL SHOCK HAZARDS. WHEN SERVICING, IT IS ESSENTIAL THAT ONLY MANUFACTURER'S SPECIFIED PARTS BE USED FOR THE CRITICAL COMPONENTS IN THE SHADED AREAS OF THE SCHEMATIC.

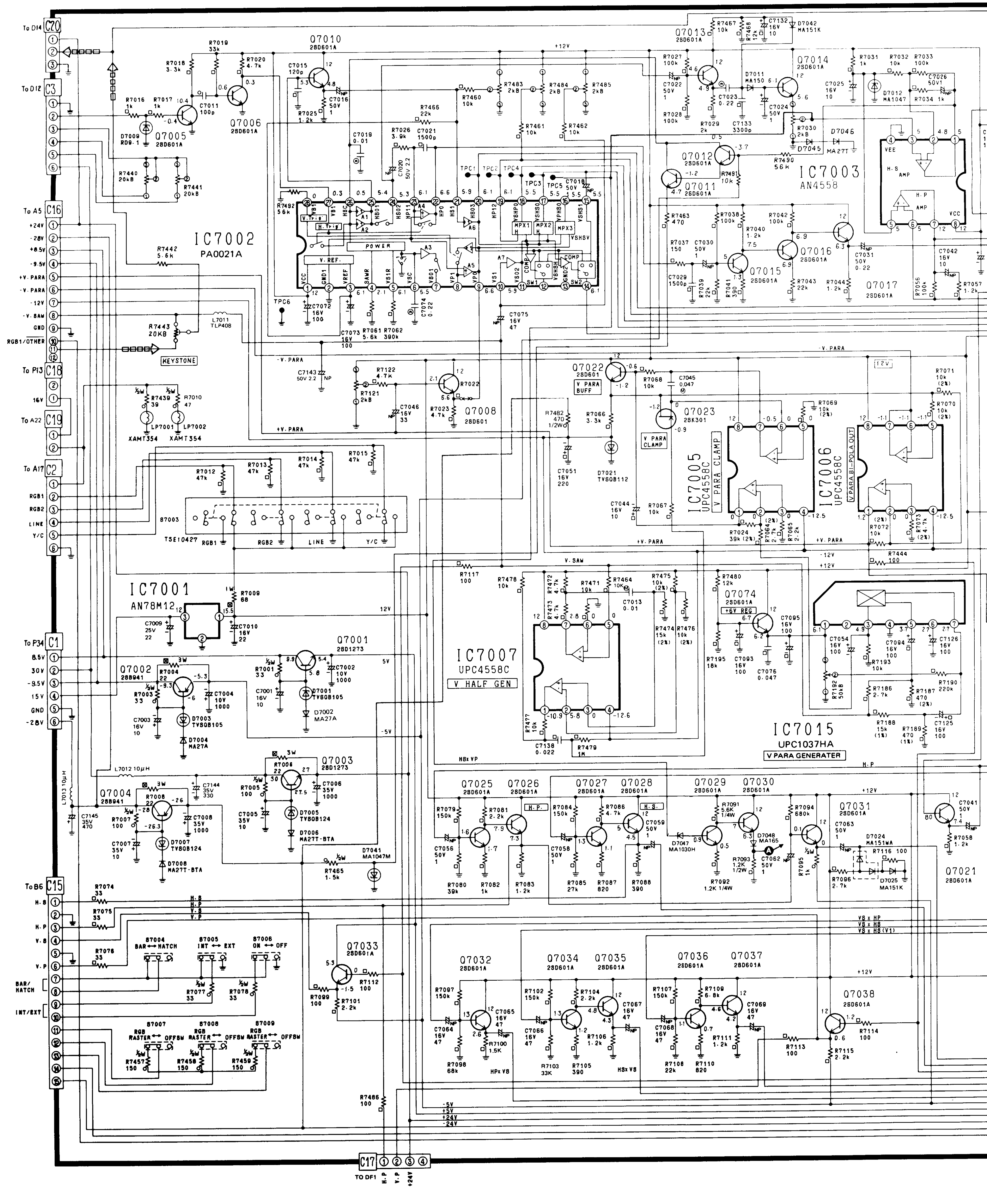
NOTE:

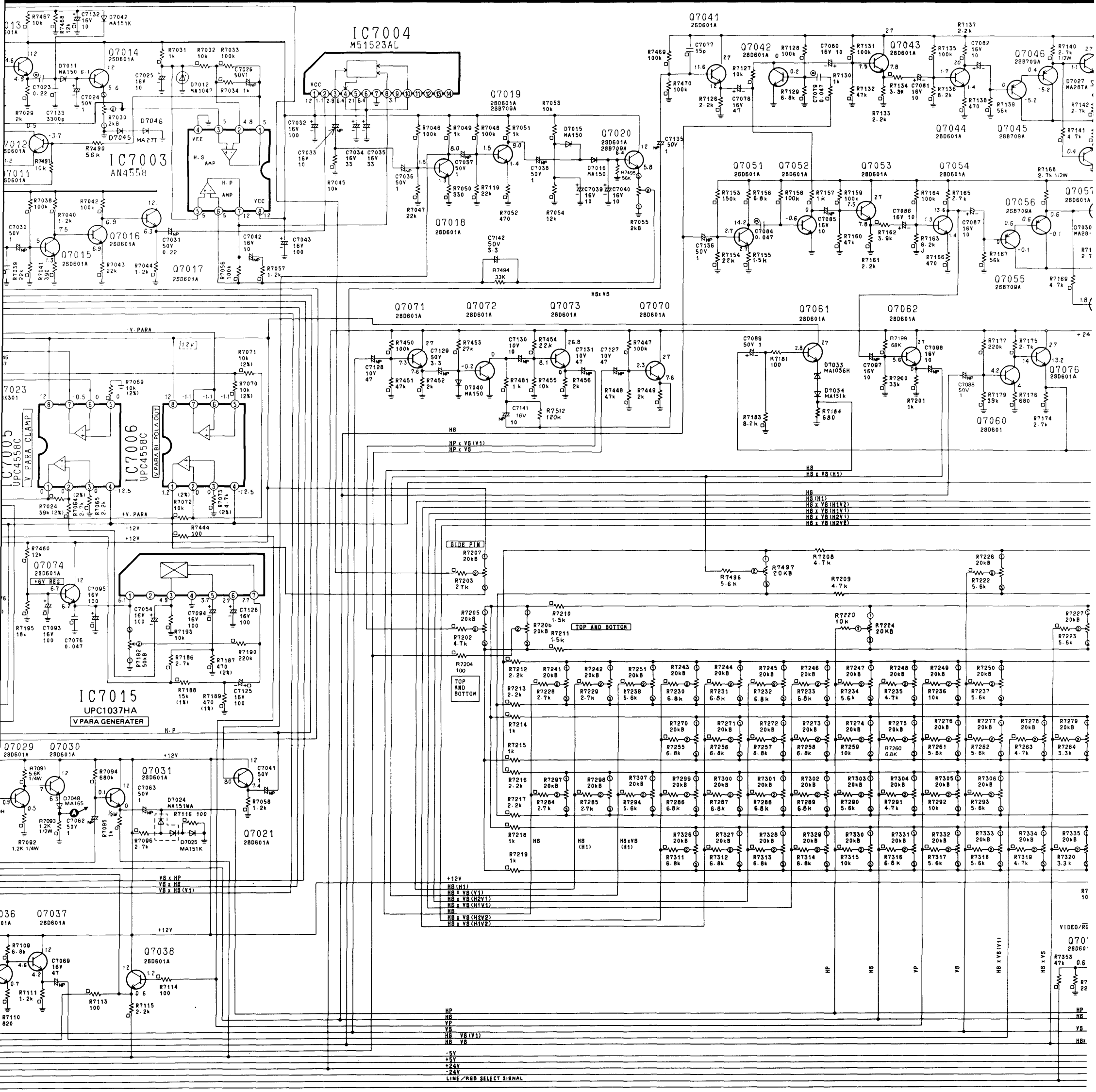
1. RESISTOR
   All resistors are carbon 1/8W resistor, unless otherwise noted the following marks.
   Unit of resistance is OHM (Ω), (K = 1,000, M = 1,000,000).
   - △ : Solid
   - □ : Wire Wound
   - Ⓕ : Non-Flamble
   - ◎ : Fixed Metal Film
   - ⊗ : Fuse
   - ● : Metal Oxide
   - Ⓛ : Lead Less Type
2. CAPACITOR
   All capacitors are ceramic 50V capacitor, unless otherwise noted the following marks.
   Unit of capacitance is μF, unless otherwise noted.
   - ⁺‖⁻ : Electrolytic
   - (NP) : Bipolar
   - Ⓩ : Z Type
   - Ⓣ : Dipped Tantalum
   - (TF) : TF Type
   - ◎ : Titanium Oxide
   - ● : Temperature Compensation
   - Ⓜ : Polyester
   - ⊠ : Polypropylene
   - ⊠ : Matalized Polyester
3. COIL
   Unit of inductance is μH.
4. TEST POINT
   - ● : Test point position
5. VOLTAGE MEASUREMENT
   Voltage is measured by a VTVM receiving colour bar signal, when all customer's controls are set to the maximum position.
6. When arrow mark (↗) is found, connection is easily found along with the direction of an arrow.
7. When schematic diagram of a board is described in more than two places, they are encircled with dotted line.....
8. ⟹ Video Signal
   ➡ R, G, B Signal
   ▭▭▭▷ H/V, H, V Pulse
9. This schematic diagram is the latest at the time of printing and subject to change without notice.

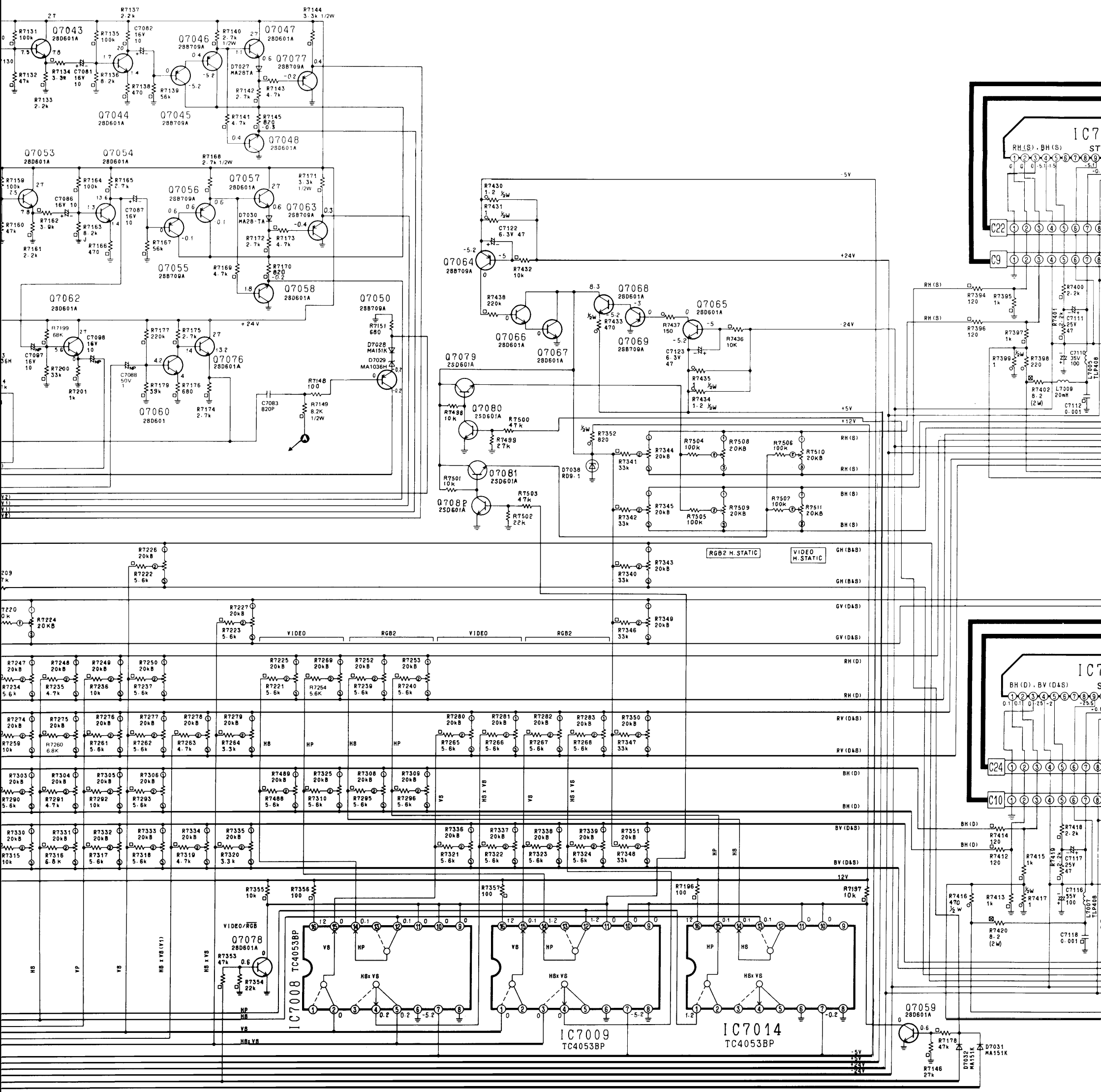
WAVEFORM PATTERN TABLE

①  TPB 8 6.4Vp-p 20μsec	②  TPB 9 6.4Vp-p 20μsec	③  TPB10 6.4Vp-p 20μsec	④  TPLR 125Vp-p 20μsec
⑤  TPLG 140Vp-p 20μsec	⑥  TPLB 140Vp-p 20μsec	⑦  TPE 6 220Vp-p 20μsec	⑧  TPE 9 7.2Vp-p 20μsec

C-BOARD Section




IC7004
M51523AL
IC7003
AN4558
IC7005
UPC4558C
V PARA CLAMP
IC7006
UPC4558C
V PARA BI-POLA OUT
IC7015
UPC1037HA
V PARA GENERATER
Q7041
Q7042
Q7043
Q7044
Q7045
Q7046
Q7047
Q7048
Q7049
Q7050
Q7051
Q7052
Q7053
Q7054
Q7055
Q7056
Q7057
Q7060
Q7061
Q7062
Q7070
Q7071
Q7072
Q7073
Q7074
Q7076
Q7014
Q7015
Q7016
Q7017
Q7018
Q7019
Q7020
Q7021
Q7029
Q7030
Q7031
Q7036
Q7037
Q7038
2SD601A
2SB709A
+V. PARA
-12V
+12V
+6V REG
H.P
H.S
VEE
VCC
SIDE PIN
TOP AND BOTTOM
HS x VS
HP x VS(V1)
HP x VS
HS
HS x VS(H1)
HS (H1)
HS x VS(H1V2)
HS x VS(H1V1)
HS x VS(H2V1)
HS x VS(H2V2)
VS x HP
VS x HS
VS x HS(V1)
+24V
-5V
+5V
-24V
LINE/RGB SELECT SIGNAL
VIDEO/RGB
HP
HS
VP
VS
HS x VS(V1)
HS x VS


Q7043 2SD601A
Q7044 2SD601A
Q7045 2SB709A
Q7046 2SB709A
Q7047 2SD601A
Q7048 2SD601A
Q7053 2SD601A
Q7054 2SD601A
Q7055 2SB709A
Q7056 2SB709A
Q7057 2SD601A
Q7058 2SD601A
Q7062 2SD601A
Q7063 2SB709A
Q7064 2SB709A
Q7065 2SD601A
Q7066 2SD601A
Q7067 2SD601A
Q7068 2SD601A
Q7069 2SB709A
Q7076 2SD601A
Q7077 2SB709A
Q7078 2SD601A
Q7079 2SD601A
Q7080 2SD601A
Q7081 2SD601A
Q7082P 2SD601A
Q7050 2SB709A
Q7059 2SD601A
Q7060 2SD601
D7027 MA28TA
D7028 MA151K
D7029 MA1036H
D7030 MA28-TA
D7031 MA151K
D7032 MA151K
D7038 RD9.1
IC7008 TC4053BP
IC7009 TC4053BP
IC7014 TC4053BP
VIDEO/RGB
RGB2 H.STATIC
VIDEO H.STATIC
VIDEO
RGB2
HS
VP
VS
HS x VS(Y1)
HS x VS
HP
HB
VB
HBx VB
+24V
-5V
+5V
+12V
-24V
RH(S)
BH(S)
GH(B&S)
GV(D&S)
RH(D)
RV(D&S)
BH(D)
BV(D&S)
12V
IC7
C22
C9
C24
C10
L7005
L7006
L7008

C-BOARD
TNP100741AZ

C2-BOARD
TNP100742AZ

C3-BOARD
TNP100785AZ

IC7011 RH(S), BH(S) STK4112MK2

IC7010 RH(D), RV(D&S) STK4112MK2

IC7012 BH(D), BV(D&S) STK4112MK2

IC7013 GH(D&S), GV(D&S) STK4112MK2

IC7014 TC4053BP

RGB2 H.STATIC

VIDEO H.STATIC

07068 2SD601A

07065 2SD601A

07069 2SB709A

07059 2SD601A

D7032 MA151K

D7031 MA151K

CY(R)

CY(G)

CY(B)

C4

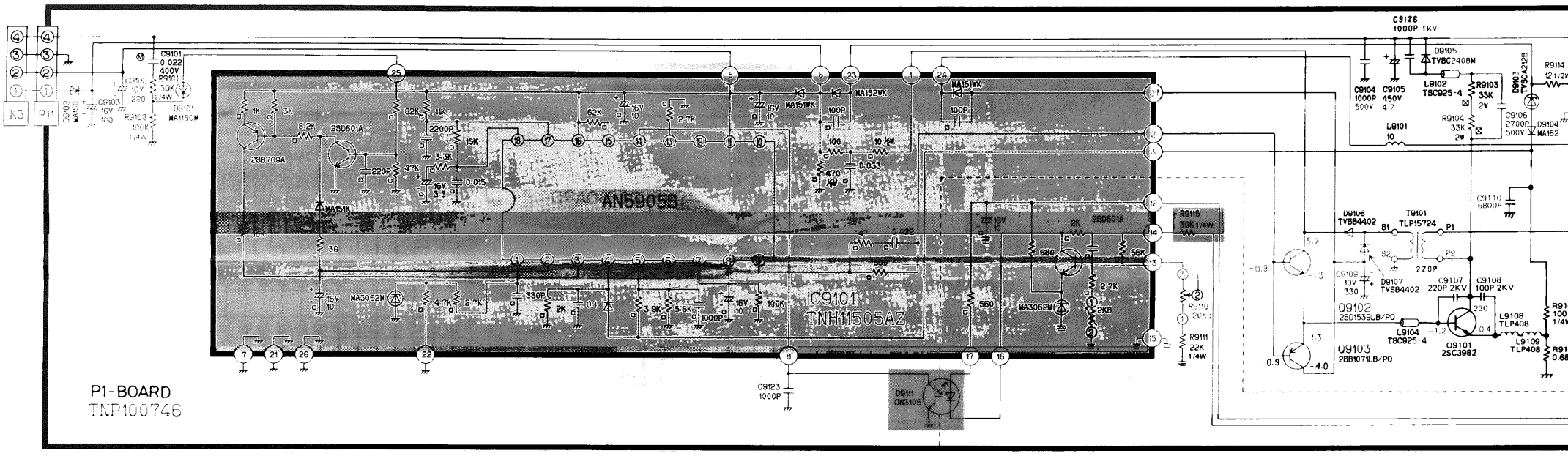
C5

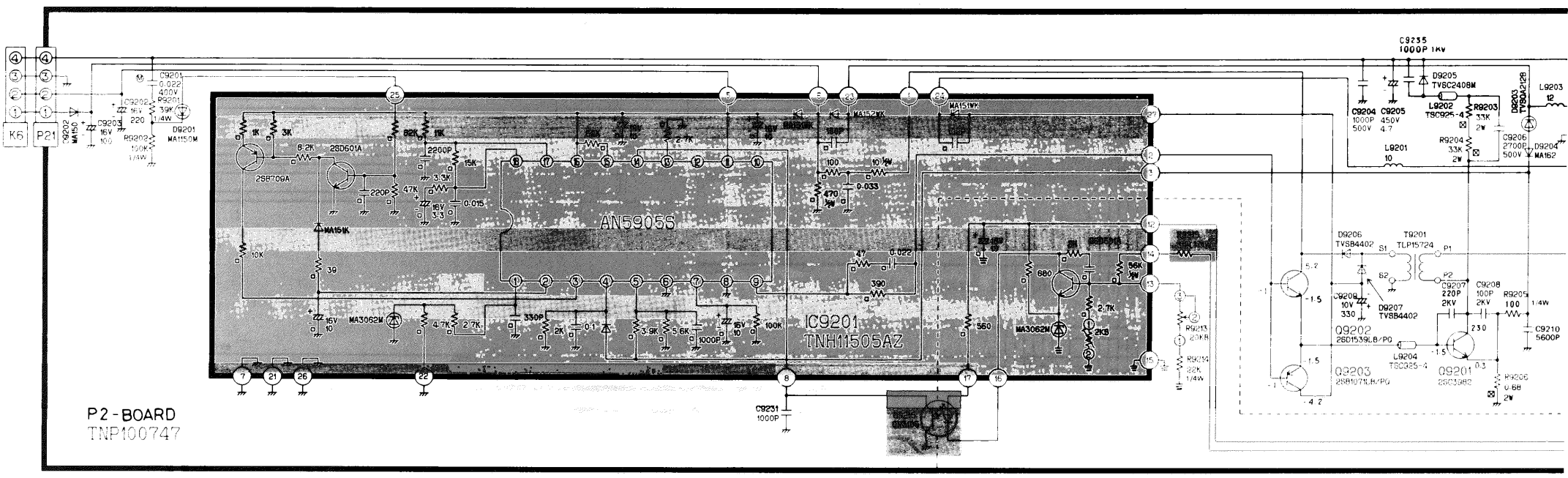
C6

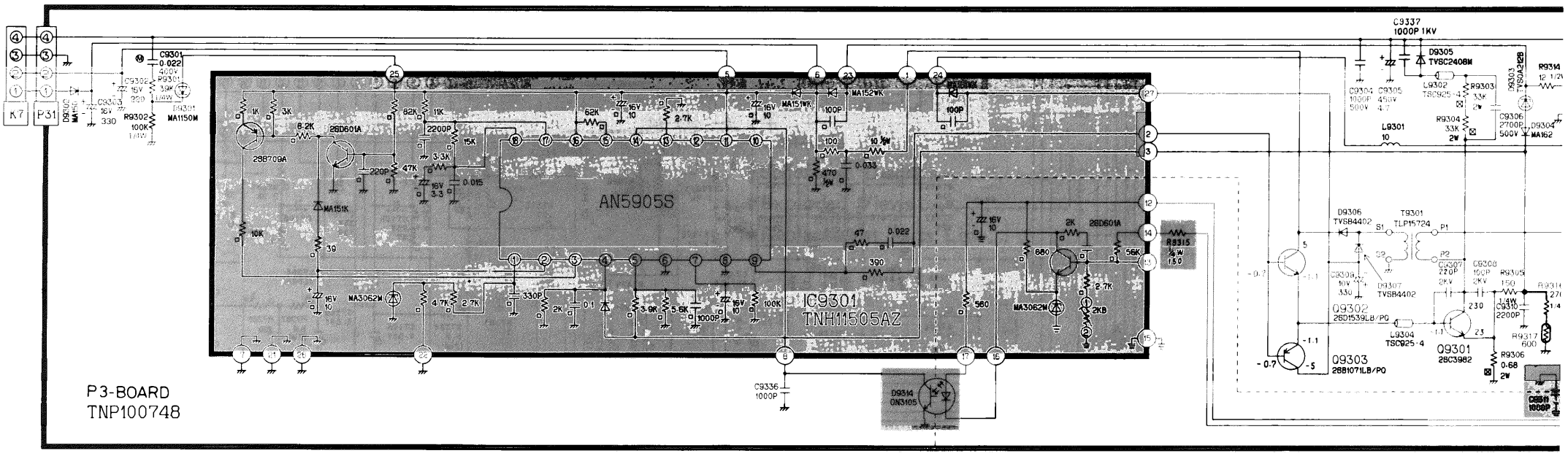
— 76 —

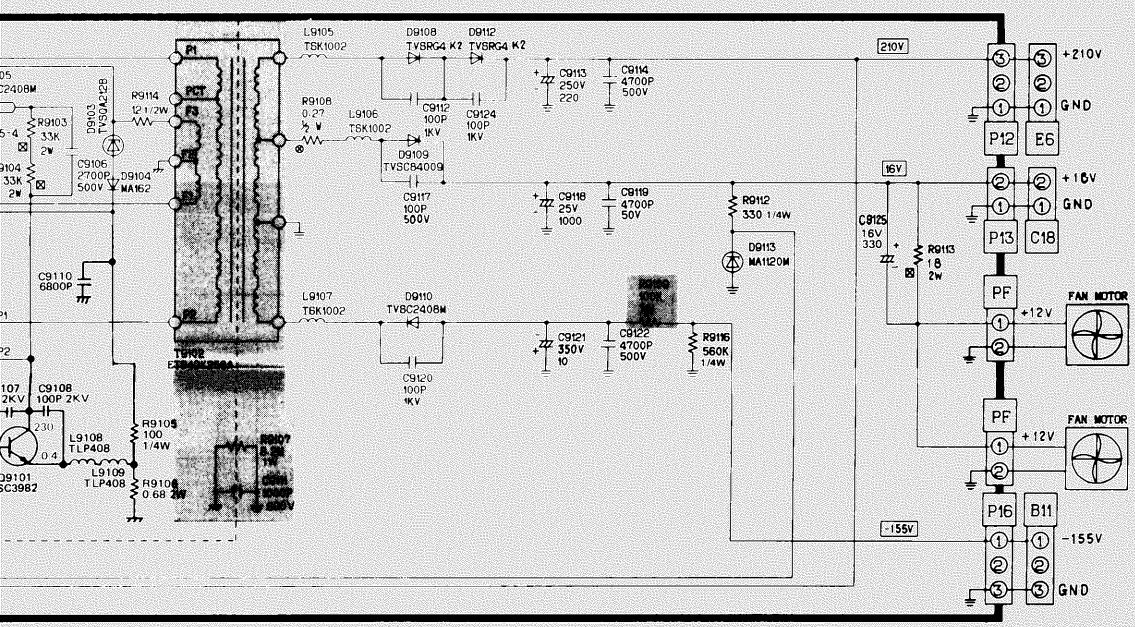
— 77 —

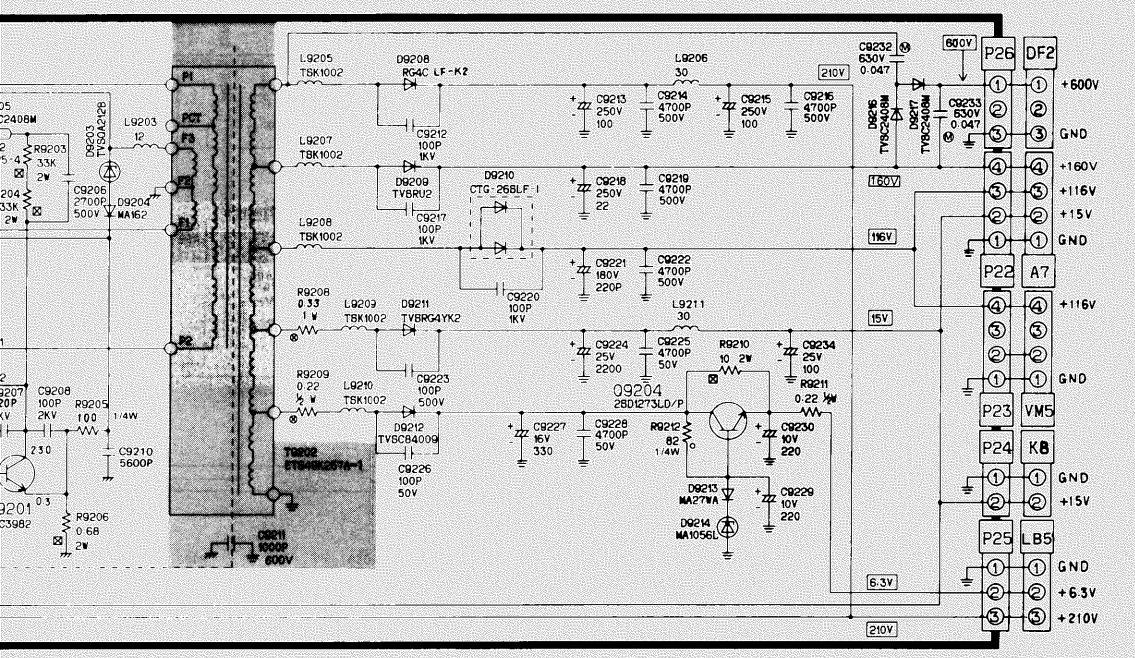
P1/P2/P3-BOARD Sections

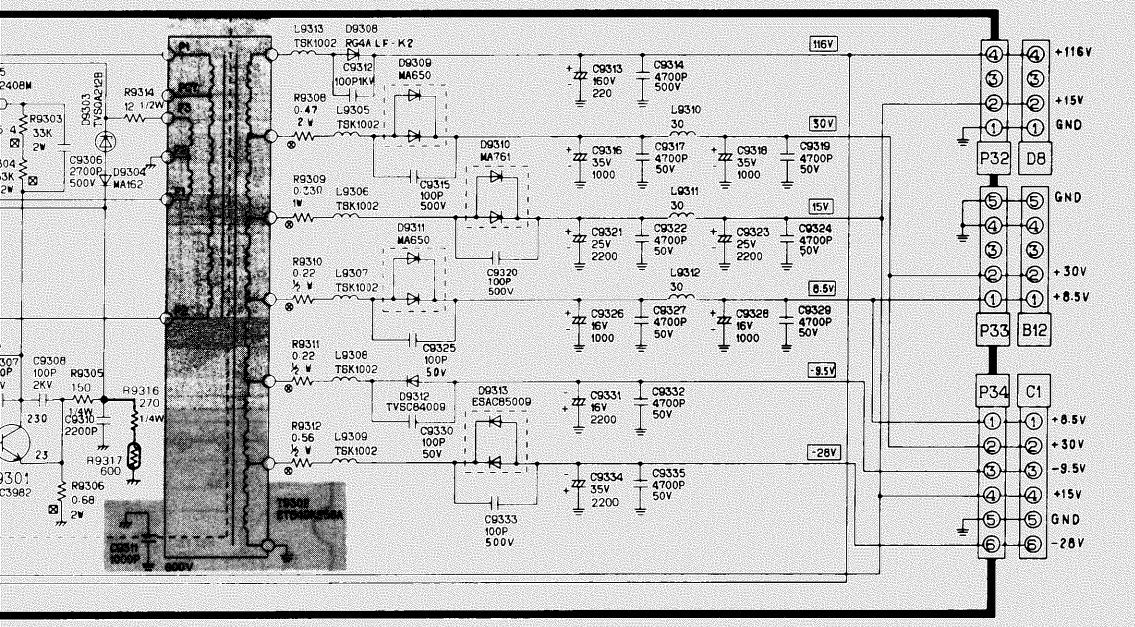




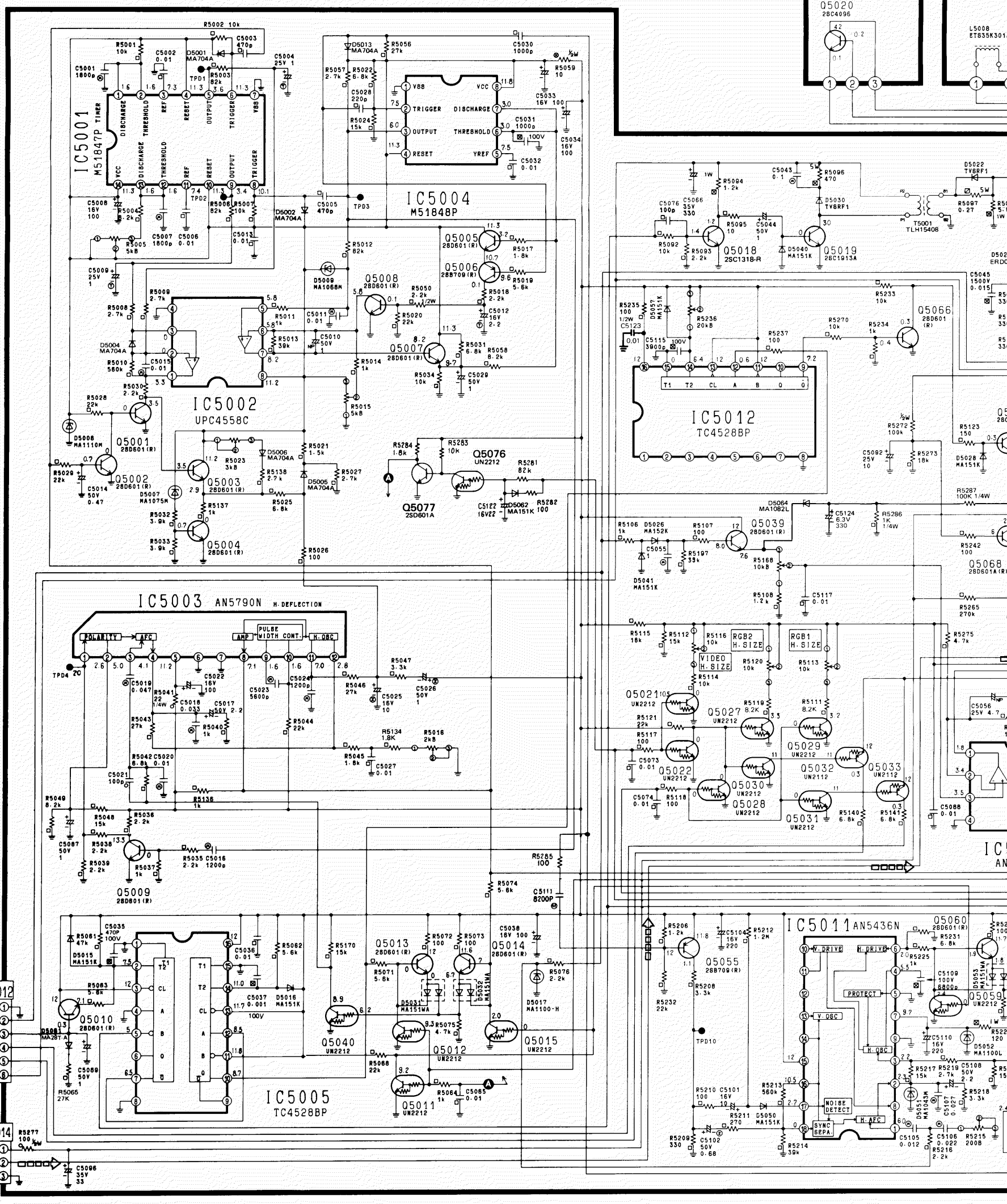


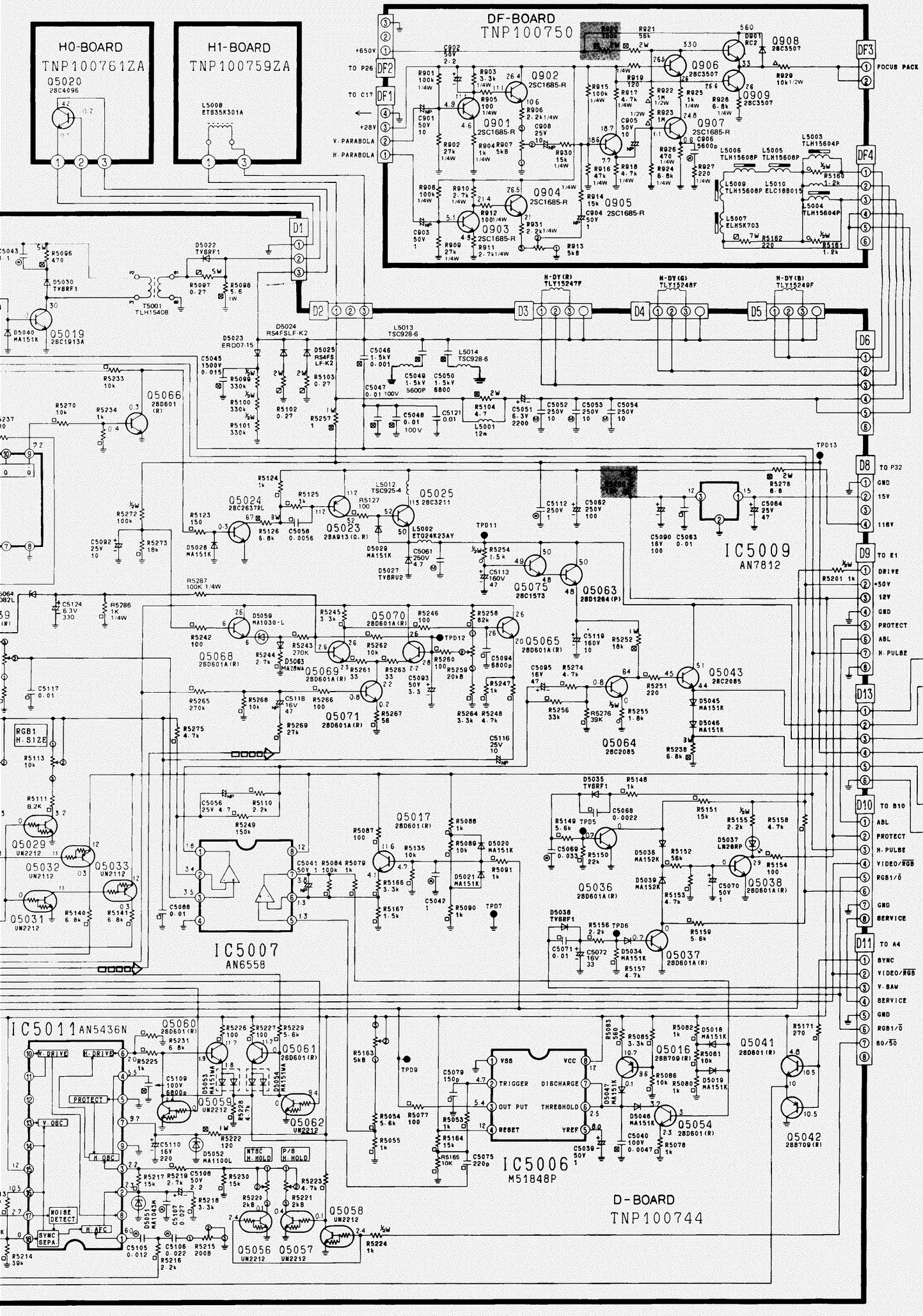

L9105 TSK1002
D9108 TVBRG4 K2
D9112 TVBRG4 K2
C9113 250V 220
C9114 4700P 500V
R9108 0.27 ½ W
L9106 TSK1002
C9112 100P 1KV
C9124 100P 1KV
D9109 TVSC84009
C9117 100P 500V
C9118 25V 1000
C9119 4700P 50V
R9112 330 1/4W
D9113 MA1120M
C9125 16V 330
R9113 18 2W
C9110 6800P
L9107 TSK1002
D9110 TVBC2408M
C9120 100P 1KV
C9121 350V 10
C9122 4700P 500V
R9116 560K 1/4W
C9108 100P 2KV
L9108 TLP408
L9109 TLP408
R9105 100 1/4W
R9106 0.68 2W
210V
16V
-155V
+12V
FAN MOTOR
+210V
GND
+16V
P12
E6
P13
C18
PF
P16
B11
-155V


L9205 TSK1002
D9208 RG4C LF-K2
L9206 30
C9212 100P 1KV
C9213 250V 100
C9214 4700P 500V
C9215 250V 100
C9216 4700P 500V
C9232 630V 0.047
C9233 630V 0.047
D9216 TVBC2408M
D9217 TVBC2408M
600V
L9207 TSK1002
D9209 TVBRU2
D9210 CTG-268LF-1
C9217 100P 1KV
C9218 250V 22
C9219 4700P 500V
160V
L9208 TSK1002
C9220 100P 1KV
C9221 180V 220P
C9222 4700P 500V
116V
L9203 12
R9208 0.33 1 W
L9209 TSK1002
D9211 TVBRG4YK2
L9211 30
15V
C9224 25V 2200
C9225 4700P 50V
R9210 10 2W
C9234 25V 100
R9211 0.22 ½W
R9209 0.22 ½ W
L9210 TSK1002
C9223 100P 500V
D9212 TVBC84009
C9226 100P 50V
C9227 16V 330
C9228 4700P 50V
R9212 82 1/4W
C9230 10V 220
D9213 MA27WA
D9214 MA1056L
C9229 10V 220
09204
28D1273LD/P
C9203 2KV
C9206 2700P 500V
D9204 MA162
C9208 100P 2KV
R9205 100 1/4W
C9210 5600P
R9206 0.68 2W
C9211 1000P 600V
6.3V
210V
+600V
GND
+160V
+116V
+15V
P26
DF2
P22
A7
P23
VM5
P24
KB
P25
LB5
+6.3V

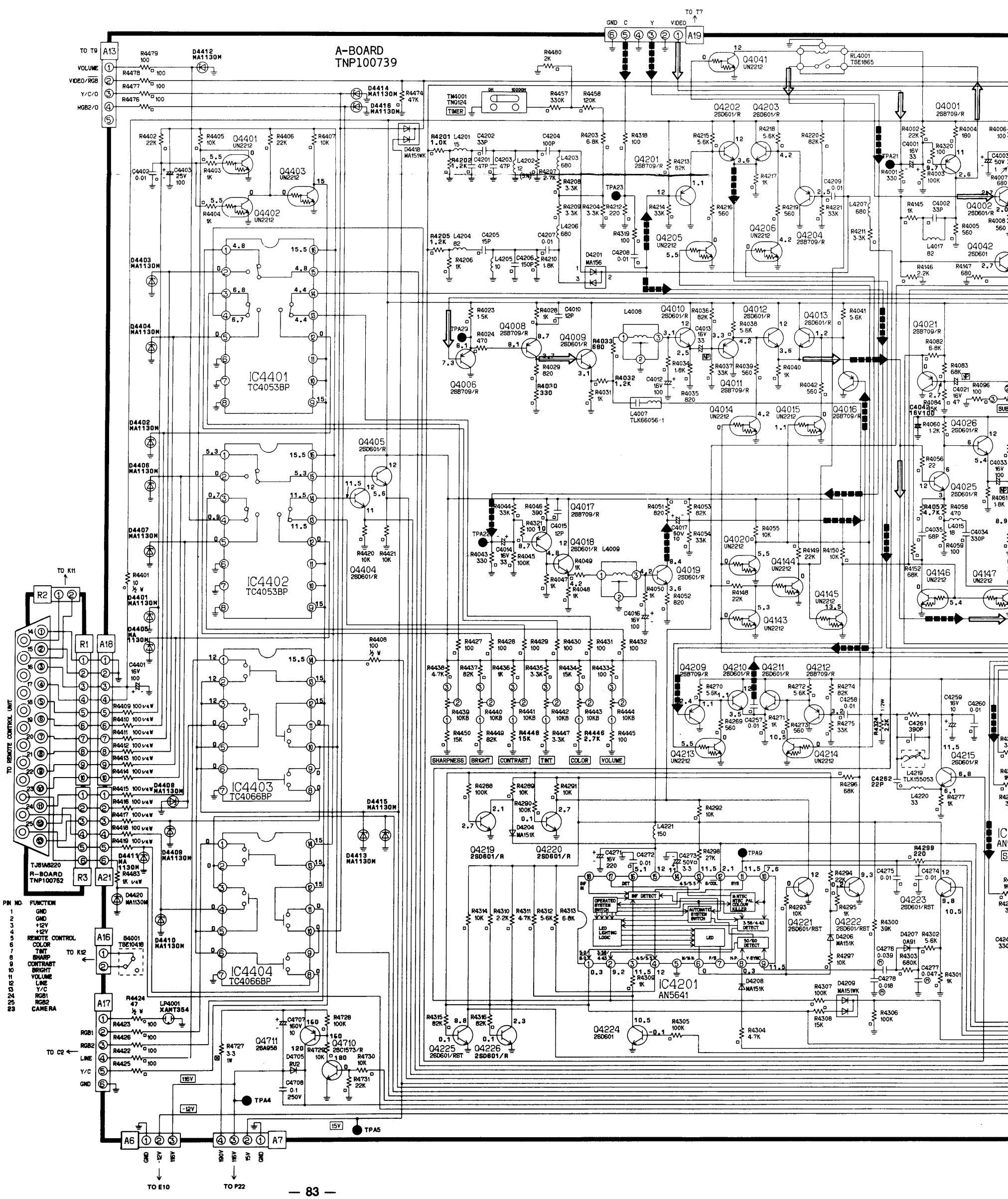

L9313 TSK1002
D9308 RG4A LF-K2
C9312 100P 1KV
D9309 MA650
R9308 0.47 2 W
L9305 TSK1002
D9310 MA761
C9315 100P 500V
R9309 0.330 1W
L9306 TSK1002
D9311 MA650
C9320 100P 500V
R9310 0.22 ½ W
L9307 TSK1002
C9325 100P 50V
R9311 0.22 ½ W
L9308 TSK1002
D9312 TVSC84009
D9313 ESAC85009
C9330 100P 50V
R9312 0.56 ½ W
L9309 TSK1002
C9333 100P 500V
C9313 160V 220
C9314 4700P 500V
C9316 35V 1000
C9317 4700P 50V
C9318 35V 1000
C9319 4700P 50V
C9321 25V 2200
C9322 4700P 50V
C9323 25V 2200
C9324 4700P 50V
C9326 16V 1000
C9327 4700P 50V
C9328 16V 1000
C9329 4700P 50V
C9331 16V 2200
C9332 4700P 50V
C9334 35V 2200
C9335 4700P 50V
C9303 2KV
C9306 2700P 500V
D9304 MA162
C9308 100P 2KV
R9305 150
C9310 2200P
R9316 270 1/4W
R9317 600
R9306 0.68 2W
C9309 1000P 600V
116V
30V
15V
6.5V
-9.5V
-28V
+116V
+15V
GND
P32
D8
+30V
+8.5V
P33
B12
P34
C1
-9.5V
-28V

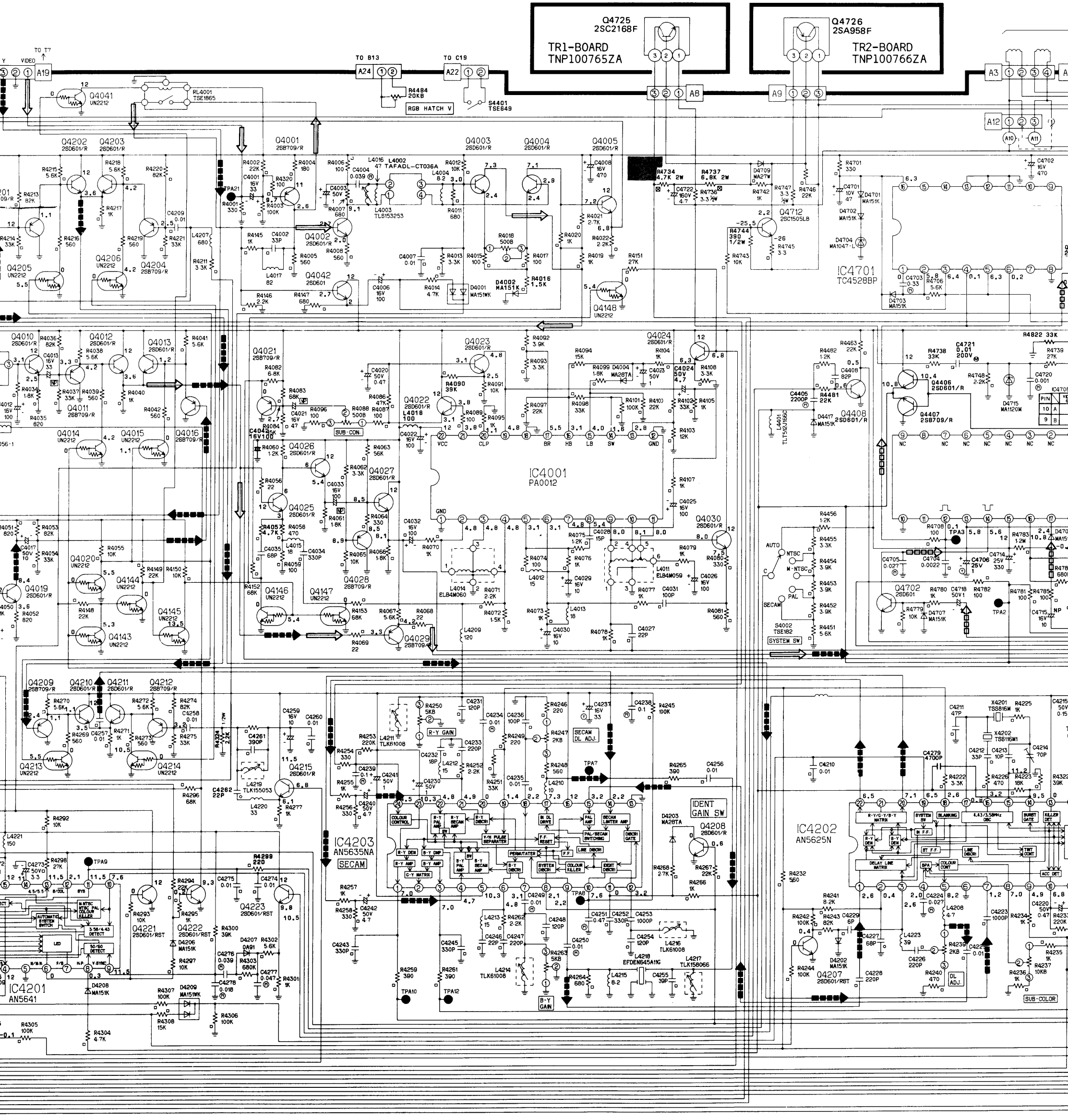
D/DF/DR1/DR2/HO/HI-BOARD Sections

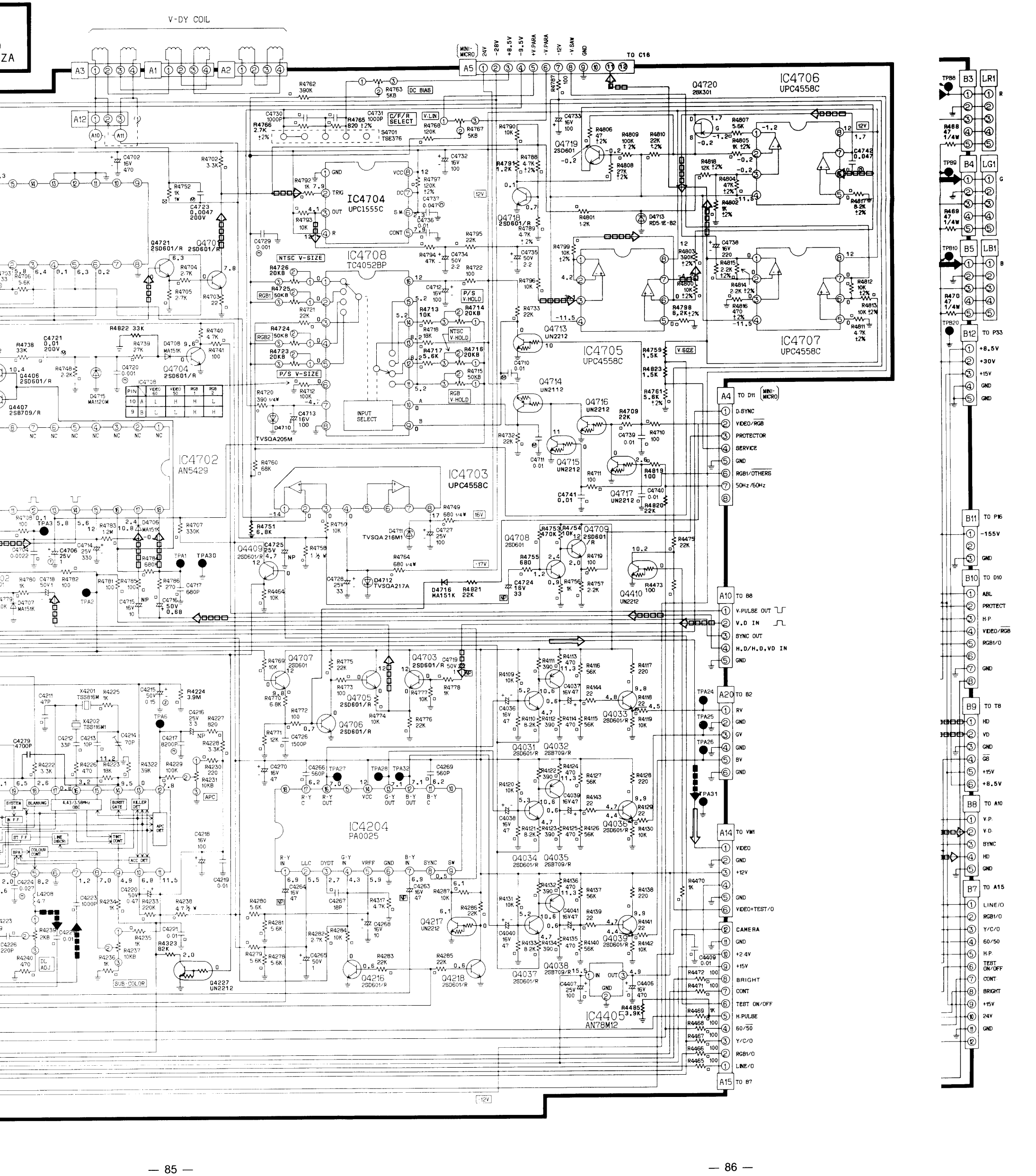



H0-BOARD
TNP100761ZA
H1-BOARD
TNP100759ZA
DF-BOARD
TNP100750
D-BOARD
TNP100744
DR1-BOARD
TNP101167ZA
DR2-BOARD
TNP101173ZA
IC5007
AN6558
IC5009
AN7812
IC5011 AN5436N
IC5006
M51848P
FOCUS PACK
TO P26
TO C17
+650V
+28V
V-PARABOLA
H-PARABOLA
TO P32
TO E1
TO B10
TO A4
RGB1
H-SIZE
PROTECT
V-OSC
H-OSC
H-AFC
NOISE DETECT
SYNC SEPA
NTSC H-HOLD
P/S H-HOLD

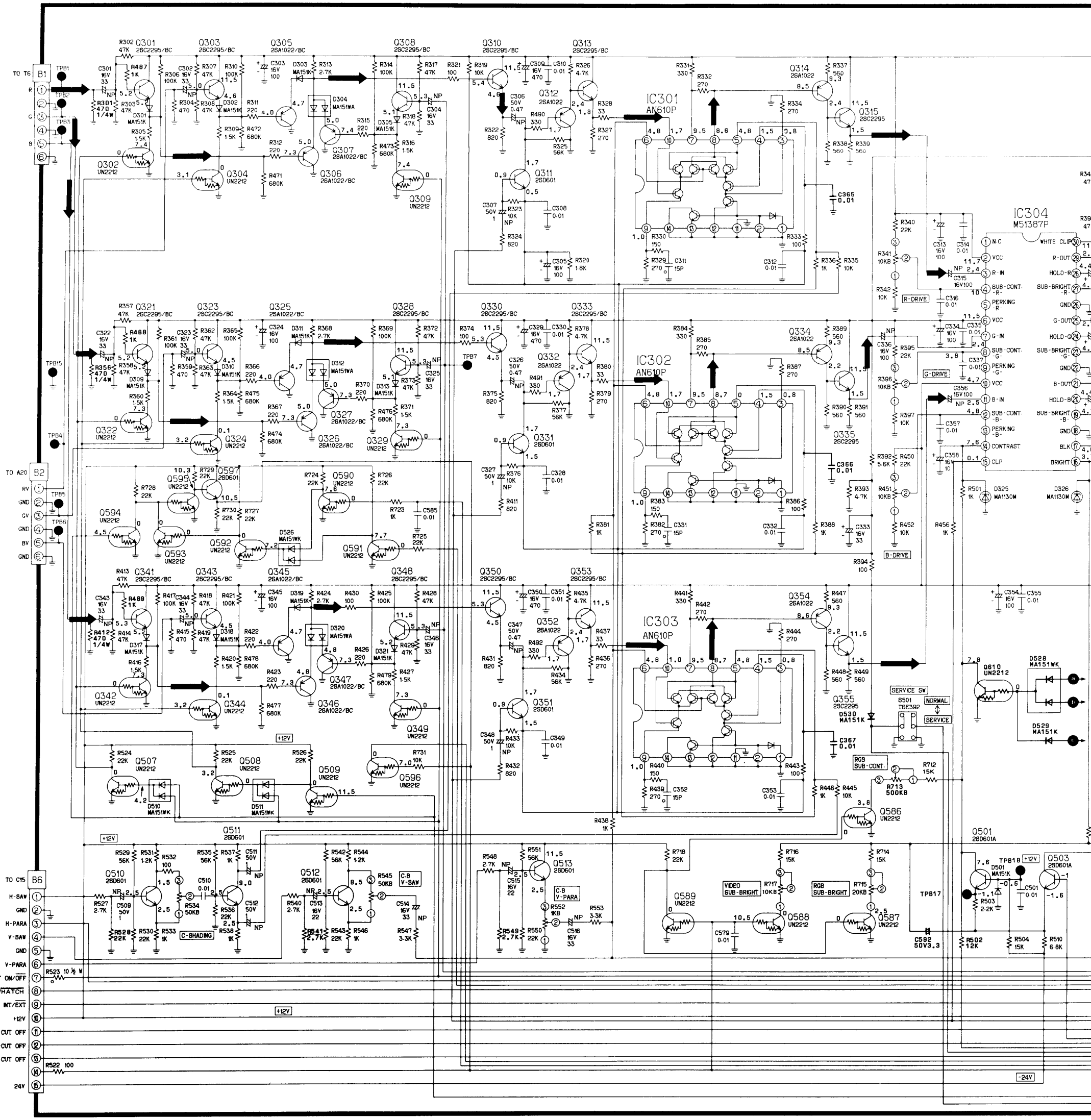
A/R/TR1/TR2-BOARD Sections

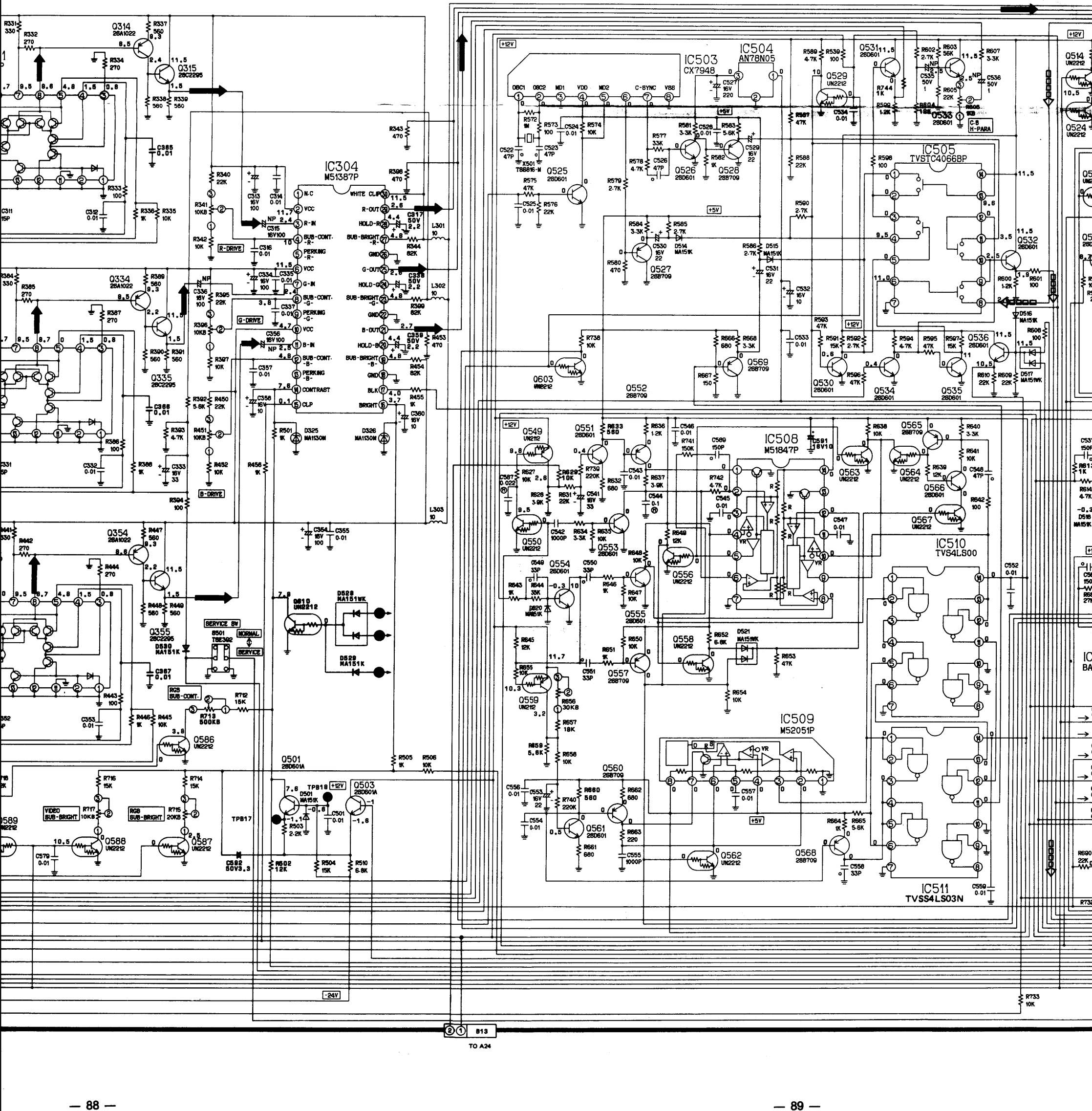



Q4725
2SC2168F
TR1-BOARD
TNP100765ZA
Q4726
2SA958F
TR2-BOARD
TNP100766ZA
TO T7
TO B13
TO C19
RL4001
TSE1865
R4484
20KB
RGB HATCH V
S4401
TSE649
Q4041
UN2212
IC4001
PA0012
IC4201
AN5641
IC4202
AN5625N
IC4203
AN5635NA
SECAM
IC4701
TC4528BP
Q4712
2SC1505LB
Q4148
UN2212
IDENT
GAIN SW
SYSTEM SW
S4002
TSE182
R-Y GAIN
SECAM
DL ADJ.
B-Y
GAIN
SUB-COLOR

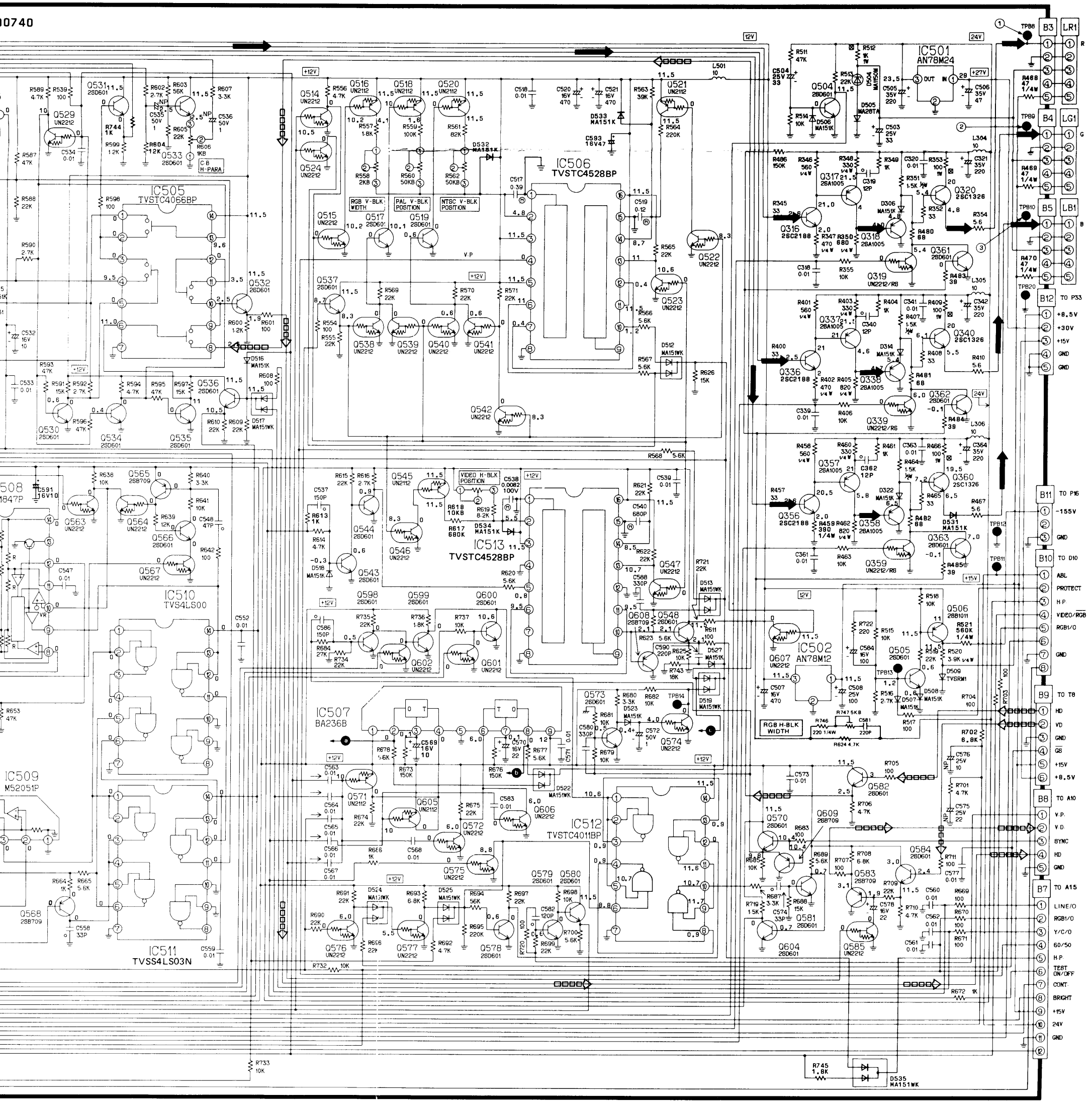

V-DY COIL
IC4704 UPC1555C
IC4708 TC4052BP
IC4706 UPC4558C
IC4707 UPC4558C
IC4705 UPC4558C
IC4703 UPC4558C
IC4702 AN5429
IC4204 PA0025
IC4405 AN78M12
Q4720 2SK301
Q4719 2SD601
Q4718 2SD601/R
Q4721 2SD601/R
Q4702 2SD601/R
Q4704 2SD601/R
Q4406 2SD601/R
Q4407 2SB709/R
Q4713 UN2212
Q4714 UN2112
Q4716 UN2212
Q4715 UN2212
Q4717 UN2212
Q4410 UN2212
Q4707 2SD601
Q4705 2SD601/R
Q4706 2SD601/R
Q4703 2SD601/R
Q4708 2SD601
Q4709 2SD601/R
Q4409 2SD601/R
Q4227 UN2212
Q4216 2SD601/R
Q4217 UN2212
Q4218 2SD601/R
Q4031 2SD601/R
Q4032 2SB709/R
Q4033 2SD601/R
Q4034 2SD601/R
Q4035 2SB709/R
Q4036 2SD601/R
Q4037 2SD601/R
Q4038 2SB709/R
Q4039 2SD601/R
D4713 RD5.1E-B2
D4708 MA151K
D4715 MA1120M
D4707 MA151K
D4706 MA151K
D4716 MA151K
D4710 TVSQA205M
D4711 TVSQA 216M1
D4712 TVSQA217A
S4701 TSE376
X4201 TSS815M
X4202 TSS116M1
MINI-MICRO
24V
+28V
+8.5V
-9.5V
+V.PARA
-V.PARA
-12V
-V.SAW
GND
TO C16
DC BIAS
C/F/R SELECT
V.LIN
NTSC V-SIZE
P/S V-SIZE
P/S V.HOLD
RGB1 V.HOLD
NTSC V.HOLD
RGB V.HOLD
INPUT SELECT
V.SIZE
APC
APC DET
ACC DET
BURST GATE
KILLER DET
BLANKING
SYSTEM SW
SUB-COLOR
DL ADJ
TPA1
TPA2
TPA3
TPA5
TPA6
TPA10
TPA24
TPA25
TPA26
TPA27
TPA28
TPA31
TPA32
A4 TO D11 (MINI-MICRO)
D.SYNC
VIDEO/RGB
PROTECTOR
SERVICE
GND
RGB1/OTHERS
50Hz/60Hz
A10 TO B8
V.PULSE OUT
V.D IN
SYNC OUT
H.D/H.D,VD IN
GND
A20 TO B2
RV
GND
GV
GND
BV
GND
A14 TO VM1
VIDEO
GND
+12V
GND
VIDEO+TEST/O
CAMERA
GND
+2.4V
+15V
BRIGHT
CONT
TEST ON/OFF
H.PULSE
60/50
Y/C/O
RGB1/O
LINE/O
A15 TO B7
B3 LR1
B4 LG1
B5 LB1
B12 TO P33
+8.5V
+30V
+15V
GND
GND
B11 TO P16
-155V
GND
B10 TO D10
ABL
PROTECT
H.P.
VIDEO/RGB
RGB1/O
GND
B9 TO T8
HD
VD
GND
G8
+15V
+8.5V
B8 TO A10
V.P.
V.D.
SYNC
HD
GND
B7 TO A15
LINE/O
RGB1/O
Y/C/O
60/50
H.P.
TEST ON/OFF
CONT
BRIGHT
+15V
24V
GND

B-BOARD Section

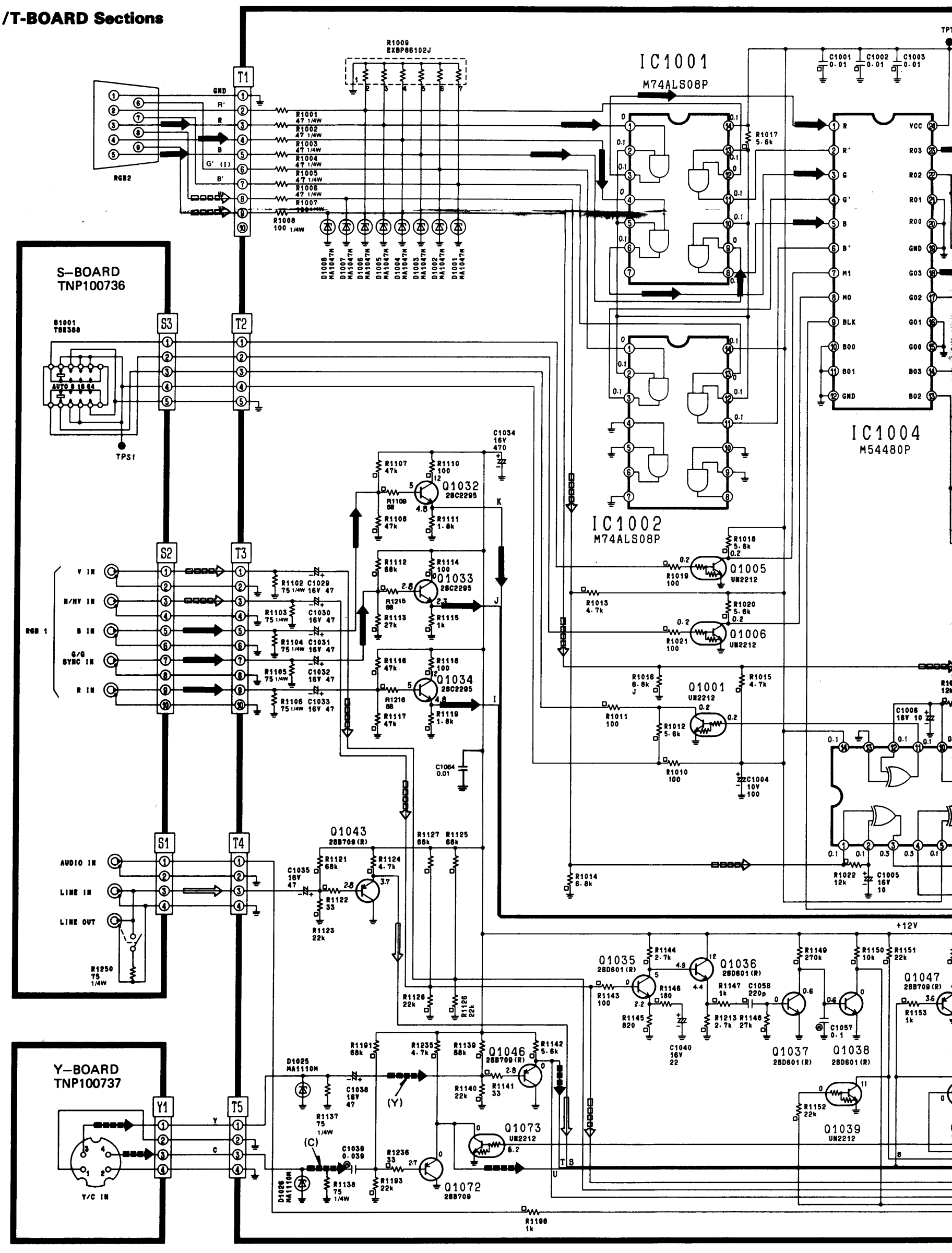


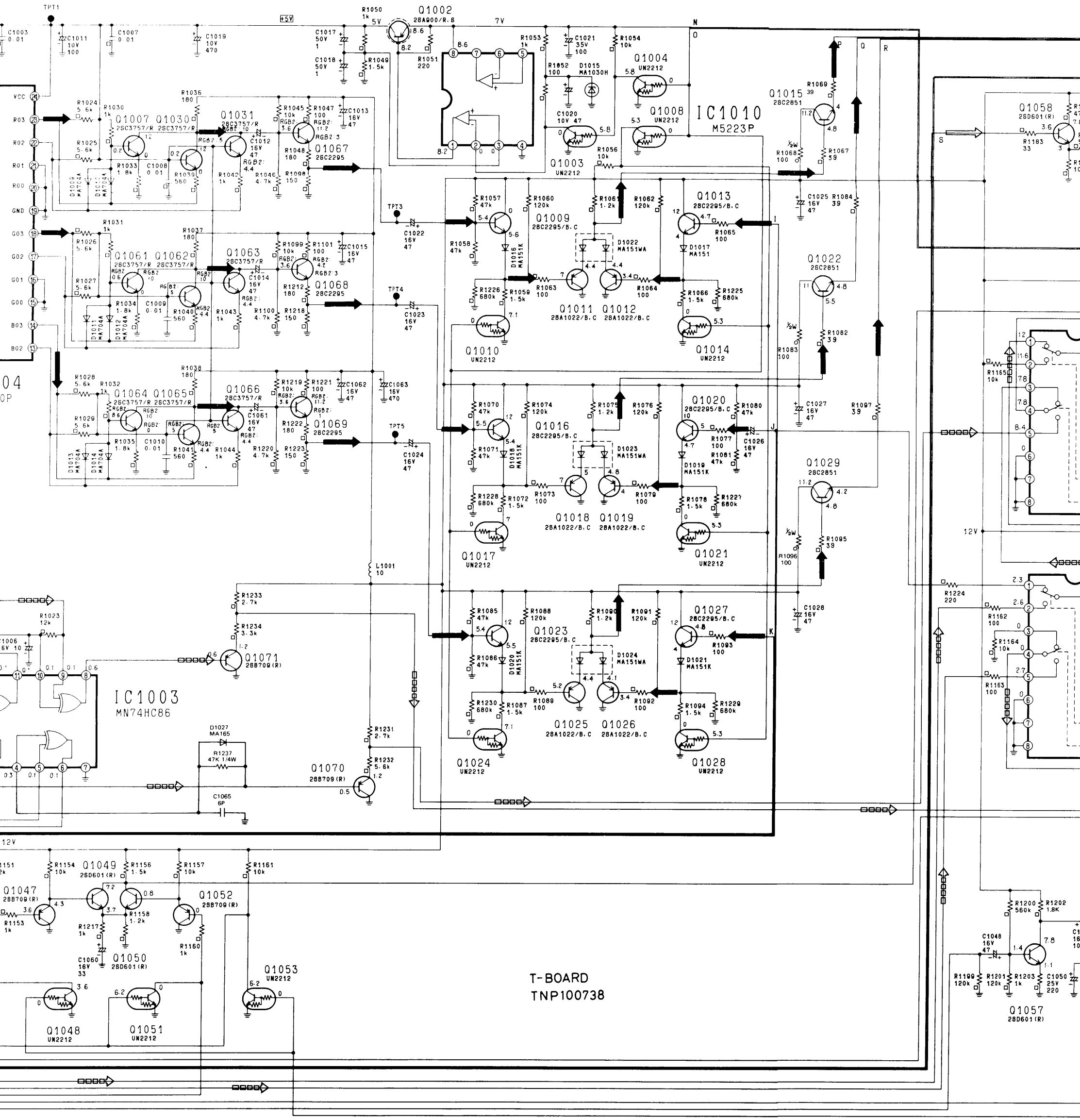

IC304
M51387P
IC503
CX7948
IC504
AN78N05
IC505
TVSTC4066BP
IC508
M51847P
IC509
M52051P
IC510
TVS4LS00
IC511
TVSS4LS03N
R-DRIVE
G-DRIVE
B-DRIVE
SERVICE SW
NORMAL
SERVICE
RGB SUB-CONT.
VIDEO SUB-BRIGHT
RGB SUB-BRIGHT
+12V
+5V
-24V
TO A24

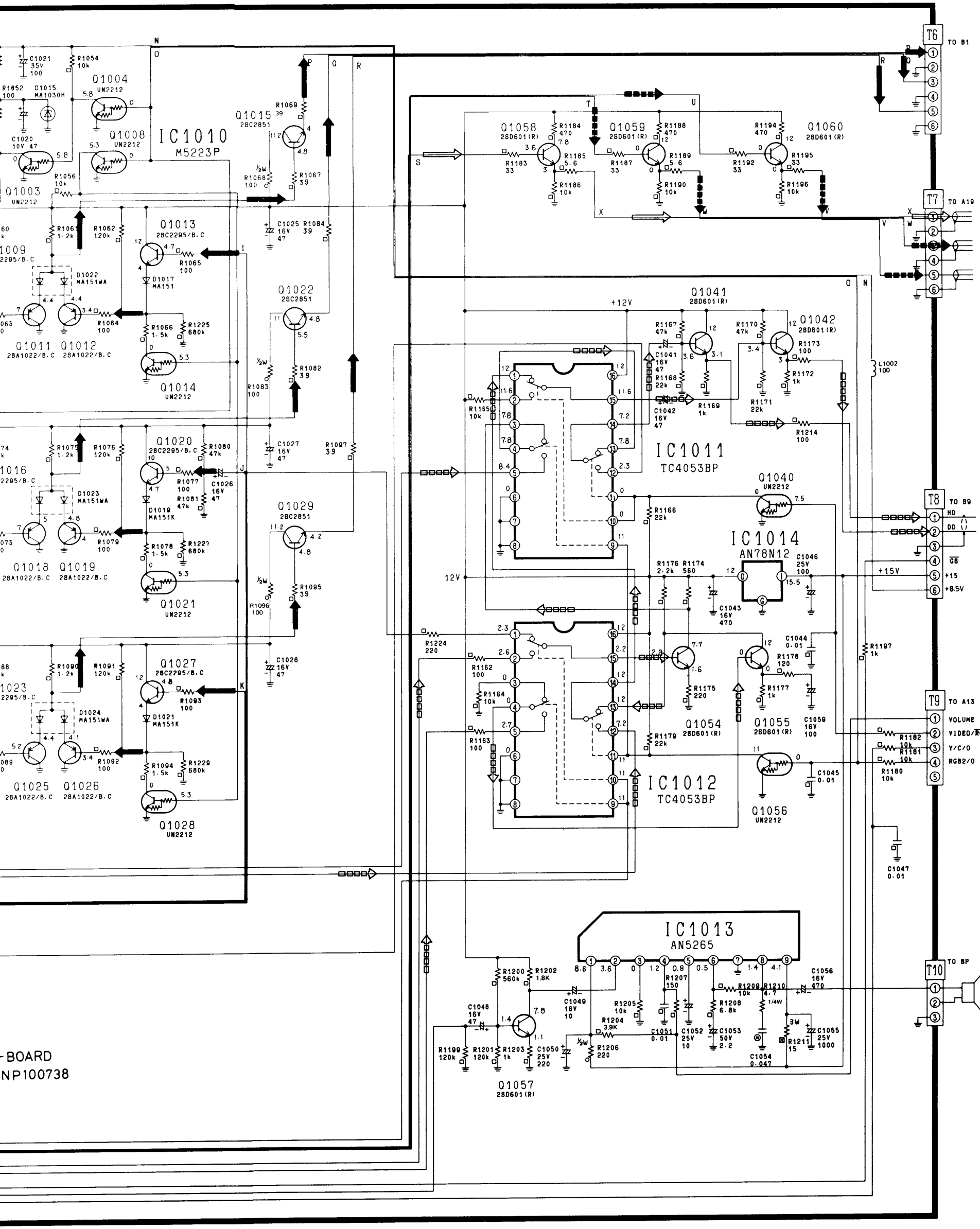
00740


IC501 AN78M24
IC502 AN78M12
IC505 TVSTC4066BP
IC506 TVSTC4528BP
IC507 BA236B
IC509 MS2051P
IC510 TVS4LS00
IC511 TVSS4LS03N
IC512 TVSTC4011BP
IC513 TVSTC4528BP
RGB V-BLK WIDTH
PAL V-BLK POSITION
NTSC V-BLK POSITION
VIDEO H-BLK POSITION
RGB H-BLK WIDTH
V.P
TO P33
TO P16
TO D10
TO T8
TO A10
TO A15
+8.5V
+30V
+15V
-15V
GND
ABL
PROTECT
H.P
VIDEO/RGB
RGB1/O
HD
VD
GS
BRIGHT
24V

Y/S/T-BOARD Sections

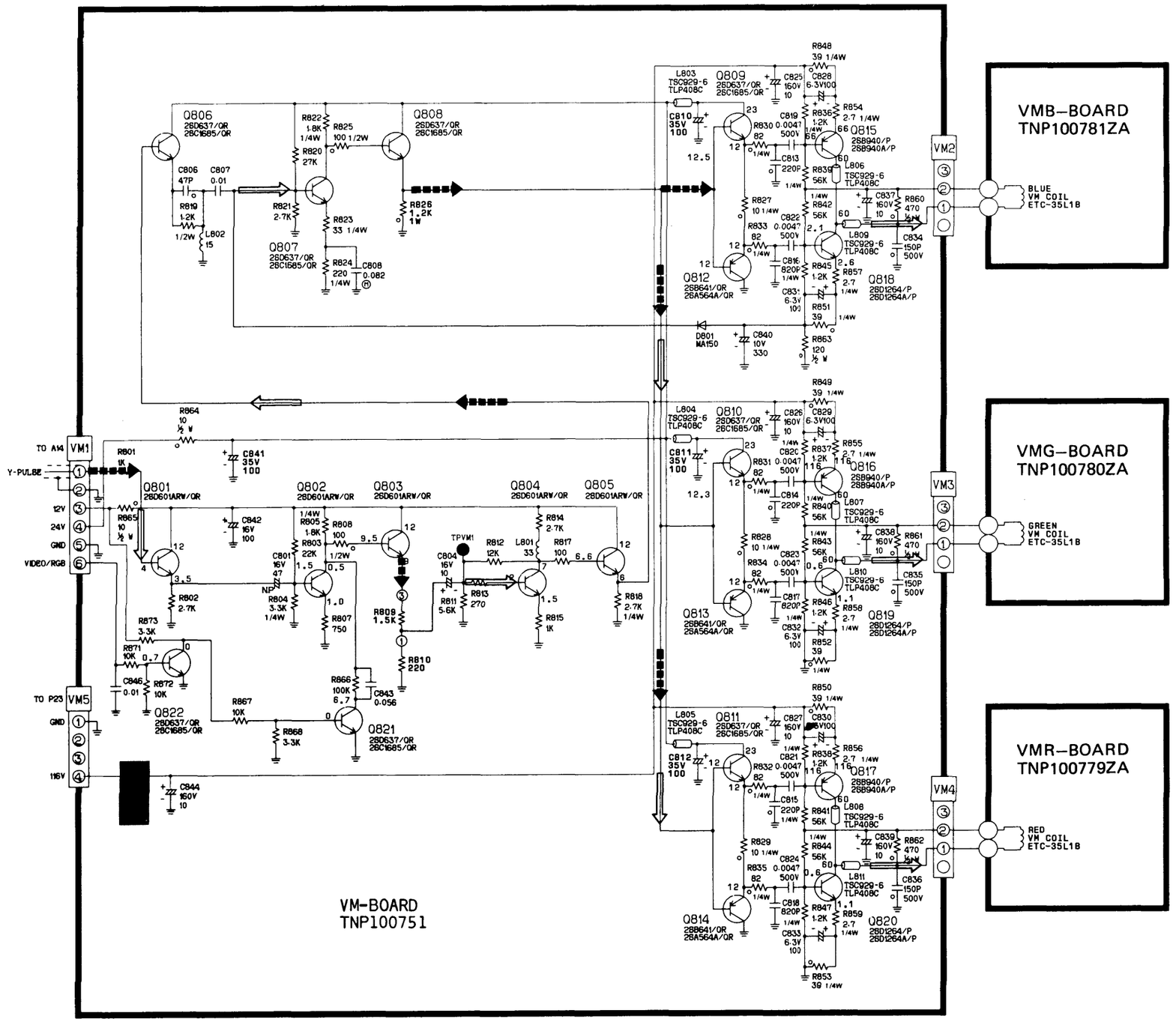


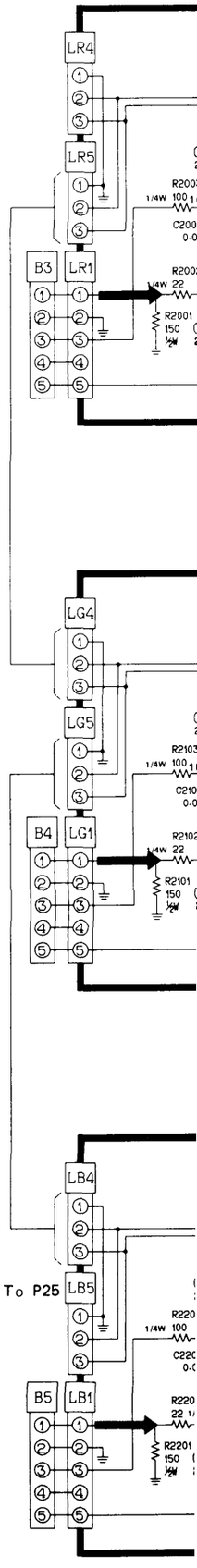

IC1010
M5223P
IC1003
MN74HC86
T-BOARD
TNP100738
Q1002
2SA900/R,S
Q1004
UN2212
Q1008
UN2212
Q1003
UN2212
Q1007 Q1030
2SC3757/R 2SC3757/R
Q1031
2SC3757/R
Q1067
2SC2295
Q1061 Q1062
2SC3757/R 2SC3757/R
Q1063
2SC3757/R
Q1068
2SC2295
Q1064 Q1065
2SC3757/R 2SC3757/R
Q1066
2SC3757/R
Q1069
2SC2295
Q1009
2SC2295/B,C
Q1011 Q1012
2SA1022/B,C 2SA1022/B,C
Q1010
UN2212
Q1013
2SC2295/B,C
Q1014
UN2212
Q1016
2SC2295/B,C
Q1018 Q1019
2SA1022/B,C 2SA1022/B,C
Q1017
UN2212
Q1020
2SC2295/B,C
Q1021
UN2212
Q1023
2SC2295/B,C
Q1025 Q1026
2SA1022/B,C 2SA1022/B,C
Q1024
UN2212
Q1027
2SC2295/B,C
Q1028
UN2212
Q1015
2SC2851
Q1022
2SC2851
Q1029
2SC2851
Q1058
2SD601(R)
Q1057
2SD601(R)
Q1071
2SB709(R)
Q1070
2SB709(R)
Q1047
2SB709(R)
Q1052
2SB709(R)
Q1049
2SD601(R)
Q1050
2SD601(R)
Q1048
UN2212
Q1051
UN2212
Q1053
UN2212
D1022 MA151WA
D1023 MA151WA
D1024 MA151WA
D1016 MA151K
D1018 MA151K
D1020 MA151K
D1017 MA151
D1019 MA151K
D1021 MA151K
D1027 MA165
D1009 MA704A
D1010 MA704A
D1011 MA704A
D1012 MA704A
D1013 MA704A
D1014 MA704A
+5V
12V
TPT1
TPT3
TPT4
TPT5
L1001 10
C1065 6P



-BOARD
NP100738

C4/VM/VMR/VMG/VMB/K/LR/LG/LB-BOARD Sections

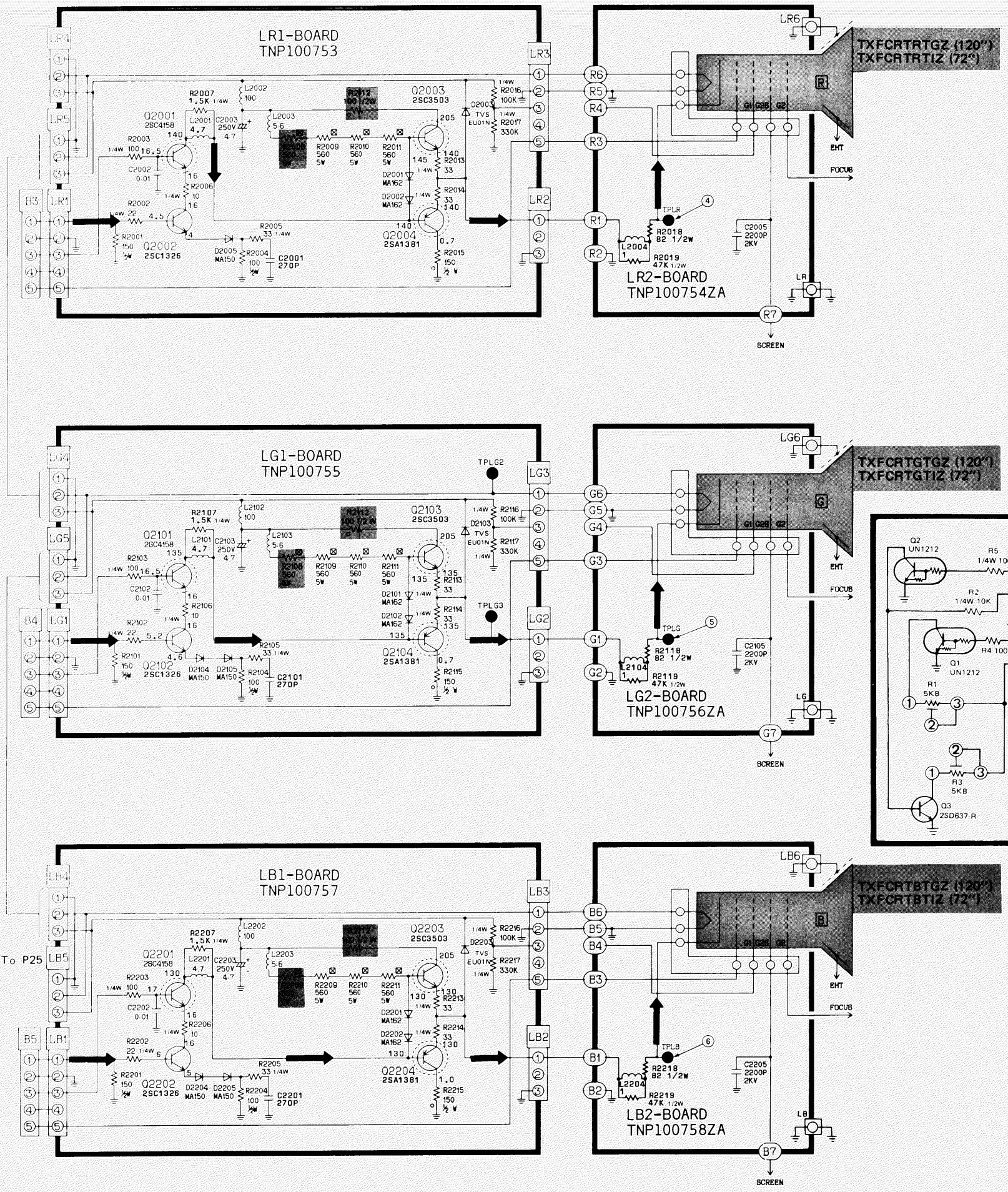


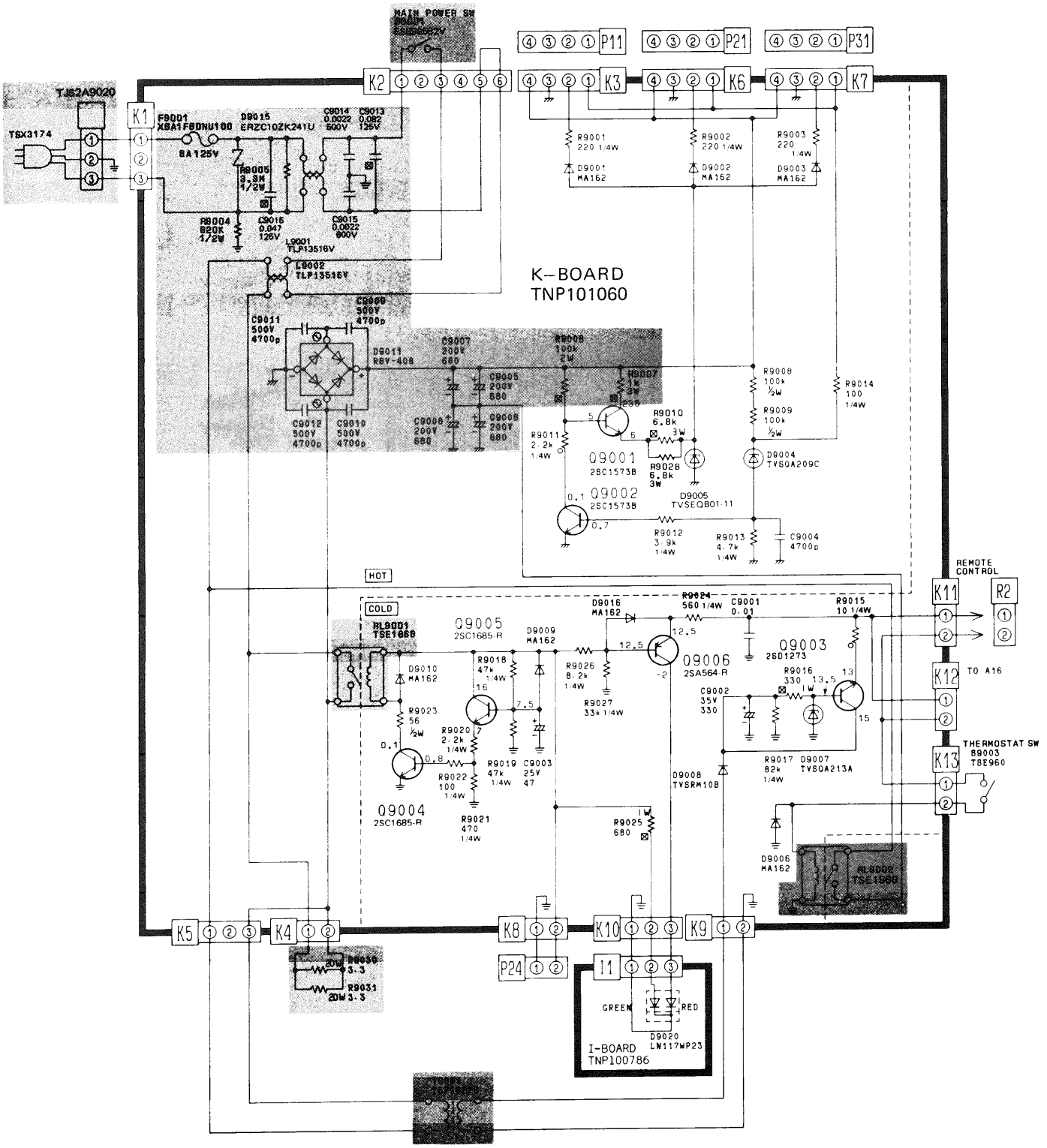


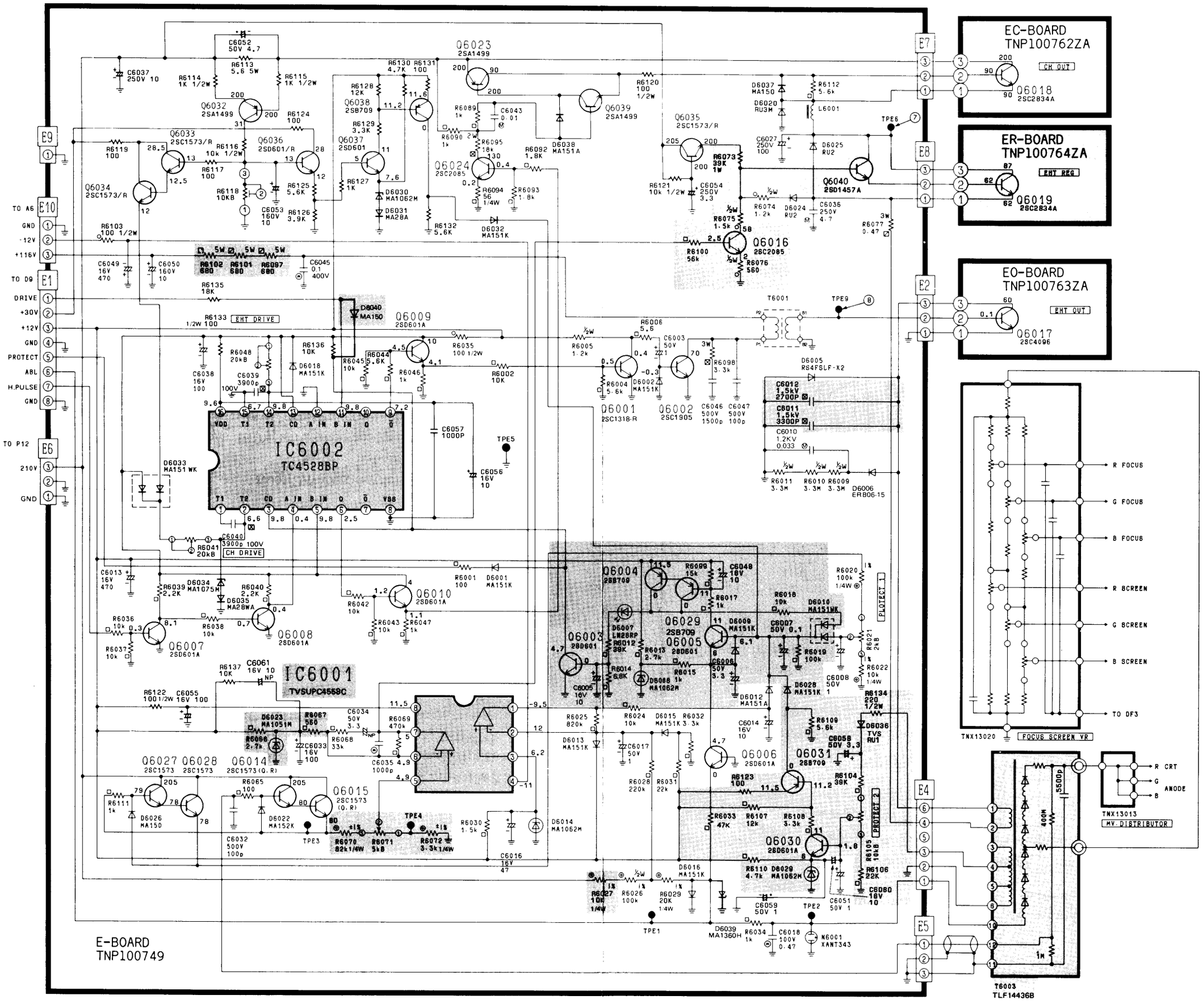
ARD
81ZA

ARD
80ZA

ARD
79ZA




K-BOARD
TNP101060
I-BOARD
TNP100786
HOT
COLD
REMOTE CONTROL
TO A16
THERMOSTAT SW
89003
TSE960
TJS2A9020
TSX3174
F9001
XBA1F8DNU100
8A 125V
D9015
ERZC10ZK241U
C9014
0.0022
500V
C9013
0.082
125V
R9005
3.3M
1/2W
R9004
820K
1/2W
C9016
0.047
125V
C9015
0.0022
600V
L9001
TLP13516V
L9002
TLP13516V
C9009
300V
4700p
C9011
300V
4700p
D9011
RBV-408
C9007
200V
680
R9006
100k
2W
C9005
200V
680
C9012
300V
4700p
C9010
300V
4700p
C9008
200V
680
C9006
200V
680
R9001
220 1/4W
R9002
220 1/4W
R9003
220
1/4W
D9001
MA162
D9002
MA162
D9003
MA162
R9008
100k
1/2W
R9009
100k
1/2W
R9014
100
1/4W
R9010
6.8k
3W
R9011
2.2k
1/4W
R9028
6.8k
3W
09001
2SC1573B
09002
2SC1573B
D9004
TVSOA209C
D9005
TVSEQB01-11
R9012
3.9k
1/4W
R9013
4.7k
1/4W
C9004
4700p
RL9001
TSE1868
09005
2SC1685-R
D9009
MA162
D9016
MA162
R9024
560 1/4W
C9001
0.01
R9015
10 1/4W
09006
2SA564-R
09003
2SD1273
R9018
47k
1/4W
R9026
8.2k
1/4W
R9027
33k 1/4W
R9016
330
1W
C9002
35V
330
D9010
MA162
R9023
56
1/2W
R9020
2.2k
1/4W
R9019
47k
1/4W
C9003
25V
47
R9022
100
1/4W
09004
2SC1685-R
R9021
470
1/4W
R9025
680
D9008
TVSRM10B
R9017
82k
1/4W
D9007
TVSOA213A
D9006
MA162
RL9002
TSE1966
R9030
3.3
2W
R9031
3.3
2W
GREEN
RED
D9020
LN117WP23
K1
K2
K3
K4
K5
K6
K7
K8
K9
K10
K11
K12
K13
P11
P21
P31
P24
I1
R2


E-BOARD
TNP100749
EC-BOARD
TNP100762ZA
CH OUT
Q6018
2SC2834A
ER-BOARD
TNP100764ZA
EHT REG
Q6019
2SC2834A
EO-BOARD
TNP100763ZA
EHT OUT
Q6017
2SC4096
IC6002
TC4528BP
IC6001
TVSUPC4558C
Q6023
2SA1499
Q6032
2SA1499
Q6039
2SA1499
Q6033
2SC1573/R
Q6036
2SD601/R
Q6034
2SC1573/R
Q6037
2SD601
Q6038
2SB709
Q6024
2SC2085
Q6035
2SC1573/R
Q6040
2SD1457A
Q6016
2SC2085
Q6009
2SD601A
Q6001
2SC1318-R
Q6002
2SC1905
Q6004
2SB709
Q6029
2SB709
Q6005
2SD601
Q6003
2SD601
Q6010
2SD601A
Q6008
2SD601A
Q6007
2SD601A
Q6027
2SC1573
Q6028
2SC1573
Q6014
2SC1573(Q.R)
Q6015
2SC1573
(Q.R)
Q6006
2SD601A
Q6031
2SB709
Q6030
2SD601A
TO A6
TO D9
TO P12
DRIVE
+30V
+12V
GND
PROTECT
ABL
H.PULSE
210V
-12V
+116V
CH DRIVE
EHT DRIVE
PROTECT 1
PROTECT 2
R FOCUS
G FOCUS
B FOCUS
R SCREEN
G SCREEN
B SCREEN
TO DF3
FOCUS SCREEN VR
TNX13020
R CRT
G
B
ANODE
TNX13013
MV. DISTRIBUTOR
T6003
TLF14436B
D6005
RS4FSLF-X2
D6006
ERB06-15
D6039
MA1360H
N6001
XANT343
TPE1
TPE2
TPE3
TPE4
TPE5
TPE6
TPE8
TPE9
L6001