

SECTION 3

CIRCUIT DESCRIPTIONS

3-1. CIRCUIT OPERATION OF BA BOARD

3-1-1. Y-System

1. Trap circuit

After passing Q11, video signal enters to a trap circuit. A Trap circuit eliminates chroma component from video signal. This projector model is equipped with 3 trap circuits, and switches/enables one of them because video signals of 3 different color TV system, i.e., PAL, SECAM, NTSC3.58, and NTSC 4.43, may enter to this projector model (subcarrier frequency is same both in PAL and NTSC4.43).

[Circuit operation with PAL or NTSC3.58 system]

Video signal passes a low-pass filter FL4, an amplifier (Q30 and Q31), a clamp-circuit (Q18, Q32, D10, D11), then enters to pin ① of a comb-filter IC10. IC10 operates as a comb-filter for PAL system when pin ③④ is held High, and for NTSC3.58 system when pin ③④ is held Low, and outputs Y-signal from pin ⑬.

Y-signal thus output from the comb-filter enters to pin 17 of IC3. IC3 gives a time-delay to Y-signal, then output it from pin ⑪. The delayed Y-signal passes an amplifier (Q118, Q119, Q120) then enters to pin ① of IC6. IC6 is the switching IC for Y-signal, and selects one from NTSC3.58/PAL, SECAM/NTSC4.43/YC, and B/W.

[Circuit operation with SECAM, NTSC4.43, or Y/C]

Video signal enters to pin ② of BPF1. BPF1 is the trap for NTSC4.43, and BPF2 is the trap for SECAM. Control to traps is done through pins ④ and ⑤ of BPF1, and traps are enabled with High state of corresponding pins.

In SECAM operation, both pins ④ and ⑤ of BPF1 are put to High to eliminate chroma components around 4.43MHz and around 4.25MHz, and Y-signal is output from pin ⑤ of BPF2.

In NTSC4.43 operation, pin ④ is put to High and pin ⑤ is put to Low to eliminate chroma components around 4.43MHz. In YC operation, both pins ④ and ⑤ are put to Low and video signal passes through traps, then is output from pin ⑤ of BPF2.

Y-signal, output from pin ⑤ of BPF2, passes a delay-line DL102 then enters to pin ③ of IC6.

[Operation with B/W signal]

B/W signal, output from Q11, passes Q52 and enters to pin ⑥ of IC6.

2. IC6 (CX-894)

This is the IC which selects one of inputs from NTSC3.58/PAL, SECAM/NTSC4.43/YC, B/W. Pin ⑧ is the signal output terminal, and pins ② and ⑥ are control terminals. Table below shows IC's operating modes and control pins' status.

operating mode	pin ②	pin ⑥
NTSC3.58/PAL	H	L
SECAM/NTSC4.43/YC	L	H
B/W	L	L

Table. 1-1.

3. IC7 (HD14053)

Y signal from pin ⑧ of IC6 enters to pin ⑫ of IC7, and Y signal in color-difference signal mode enters to pin ⑬ of IC7, respectively. Output signal switching is done using pins ⑨, ⑩ and ⑪. Input signal to pin ⑫ is output from pin ⑭ when pins ⑨, ⑩ and ⑪ are put to Low, and input signal to pin ⑬ is output from pin ⑭ when these control pins are put to High.

4. IC12 (sharpness IC)

Y signal, output from pin ⑭ of IC7, enters to pin ② of IC12, a sharpness control IC. Y-signal is given high-peaking at about 3.6MHz in VIDEO mode, and at about 6.6MHz in IDTV mode. Y-signal is output from pin ⑩ of IC12. Sharpness control terminal is pin ⑧, and the control voltage is in -2.5V to +2.5V range. Y signal, output from pin ⑩ of the IC, passes an amplifier (Q313, Q317, Q318) and enters to pin ⑦ of IC8 (CXA-1216P), a RGB matrix.

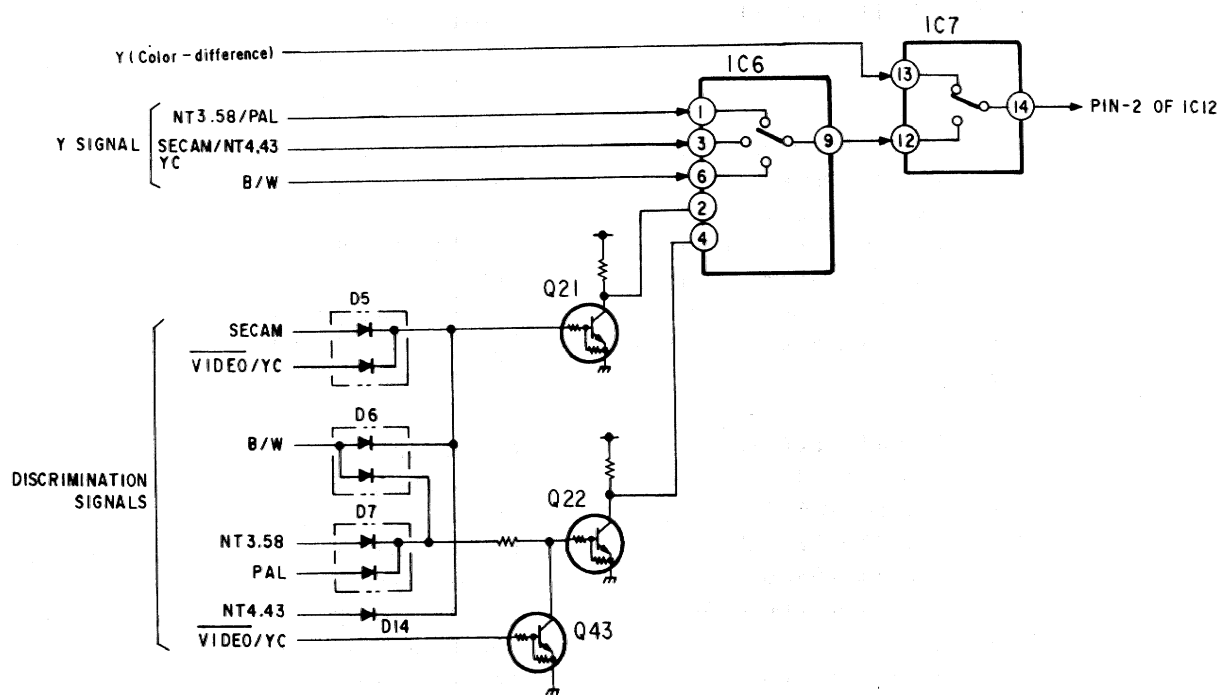


Fig. 1-1.

3-1-2. CHROMA System

Chroma signal of NTSC3.58/PAL is output from pin ⑮ of a comb-filter (IC10). Then enters to pin ⑬ of IC1. In SECAM/NTSC4.43 or YC modes of operation, chroma signal enters to pin ⑫ or pin ① of IC1, respectively. Chroma signal is output from pin ⑮ of IC1, then passes band-pass filters as shown in Fig. 1-2.

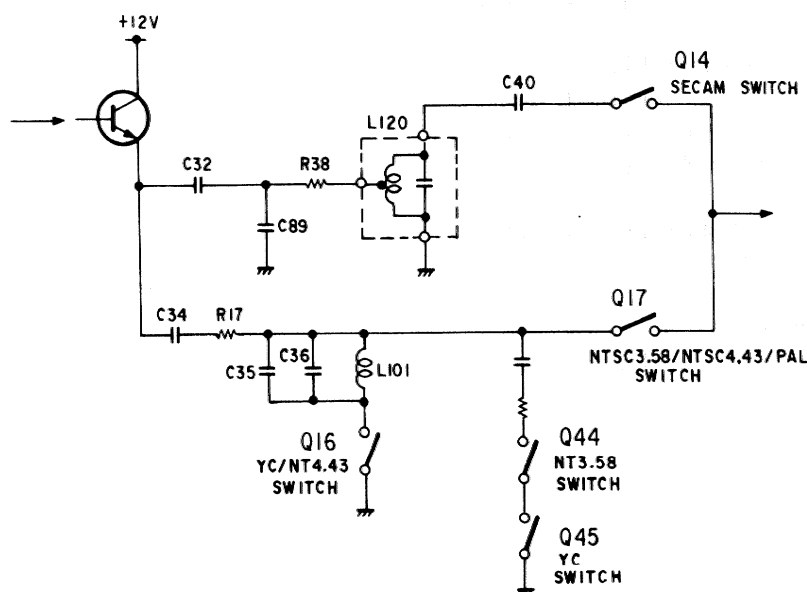


Fig. 1-2.

1. IC2 (TDA4555)

After passing corresponding BPFs, chroma signal enters to pin ⑮ of decoder IC (TDA4555). PAL or SECAM signal is output from pin ⑫, and it passes a delay-line to be delayed by 1H time, then enters to pin ⑩.

With its phase and level be adjusted by L105 and RV101, the signal is added to the signal entered from pin ⑮. The resultant signal is then decoded in the IC. R - Y signal is output from pin ①, and B - Y signal from pin ③.

ID circuit consists of following 3 circuits:

- Phase discriminator to compare the phase of burst signal of PAL/NTSC system with the phase of internal reference signal
- Frequency discriminator to provide H/2 signal in SECAM transmission an internal phase discriminator and an external phase discriminator connected to pin 22 (SECAM-ID reference circuit)
- H/2 detector circuit for PAL/SECAM system and a logic circuit for true ID

2. HUE COL CONTROL

HUE COL CONTROL voltage is in -2.5V to 2.5V range, and is converted to 2V to 7V range in an operational amplifier (IC13), then sent to IC003 (CXA1216P) as the control voltage to it. 3 potentiometers, i.e., SUB HUE (RV105, used in NTSC system), HUE ADJ (RV103), and SUB COL (RV104) are used to compensate variation in ICs and/or resistors.

3. SUB PICTURE-SUB BRIGHT

Pin ⑳ of IC8 (CXA-1216P) is PICTURE control terminal, and pin ㉑ is BRIGHT control terminal. RV102 (SUB PIC) is used to adjust PICTURE level. Output voltage from IC9's pin ① controls SUB-BRIGHT to maintain BRIGHT level constant.

3-1-3. IC15 (H8B7178B)

IC15 performs (1) SYNC separation, and (2) Sandcastle Pulse (S.C.P.) output. Y-signal, output from pin ⑭ of IC7, passes an amplifier (Q336, Q337, Q338), a clamper (D201), a limiter (D303, D304), then enters to pin ③ of IC15. IC15's pin ① outputs S.C.P., pin ⑧ outputs V. Sync, and pin ⑪ outputs H. Sync, respectively. S.C.P. enters to pin ㉔ of IC2 (TDA4555). Phase relationship between chroma signal (input to pin ⑮) and S.C.P. is as shown in Fig. 1-3.

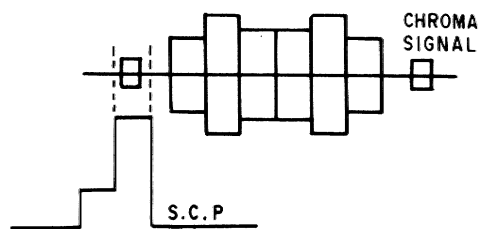


Fig. 1-3.

3-1-4. IC11 (CX-7916)

CX-7916 is an IC to discriminate 50Hz or 60Hz with H. SYNC is applied to pin ①, and V. SYNC to pin ⑤. The IC's operation is as shown in table below:

input signal	pin ②	pin ③
50Hz (PAL, SECAM)	L	H
60Hz (NTSC 3.58/4.43)	H	L

Table. 1-2.

3-1-5. B/W Discrimination

If color signal enters, one of pins ㉕ to ㉗ of IC2 is held HIGH.

This causes Q23 be turned ON, and its collector be held LOW.

Q23 does not turn ON in case of B/W signal, and its collector is held HIGH.

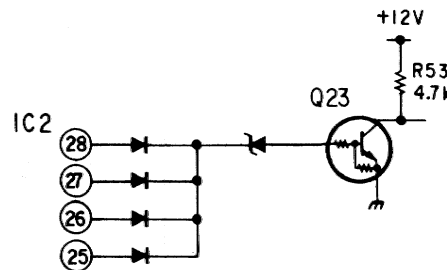


Fig. 1-4.

3-1-6. IC8 (CXA-1216P)

IC8 (CXA-1216P) is a R.G.B matrix IC. Its pin ⑦ is Y input terminal, pin ⑥ is B - Y input, pin ⑤ is R - Y input. BLK pulse enters to pin ①, and B/P. CLAMP pulse to pin ③. R, G, and B signals are output from pins ⑮, ⑰, and ⑱, respectively.

Pin ⑩ is AUTO PEDESTAL terminal, and Dynamic Pic. function is enabled when SW1 is in OPEN status.

3-1-7. IC5 (NJM2228)

IC5 generates the clock signal to be applied to pin ⑧ of comb-filter IC10.

With NTSC 3.48/PAL signal input, X101/X102 starts to oscillate. The clock signal thus generated passes Q202 and Q203, then enters to pin ① of IC5. From pin ④ of IC5, a clock signal with doubled frequency of input signal is output. It passes an amplifier (Q205, Q206, Q207), then enters to pin ⑧ of IC10.

3-1-8. IC14 (SN74LS12NS)

IC14 is a switch for IDTV discrimination. Output terminal (pin ⑫) is held HIGH during IDTV MODE or RGB MODE, and is held LOW during VIDEO MODE. This terminal controls both IC12's pin ④ (control terminal of sharpness IC) and BA-1 connector's 22a (VIDEO/IDTV).

Discrimination signals to be applied to IC14 are as shown below:

VIDEO/YC { with Composite Video input : H
with YC input: L

RGB/Video { with video input: L
with RGB input: H

Code 3 { with composite video, Y/C input: H
with color difference inputs: L

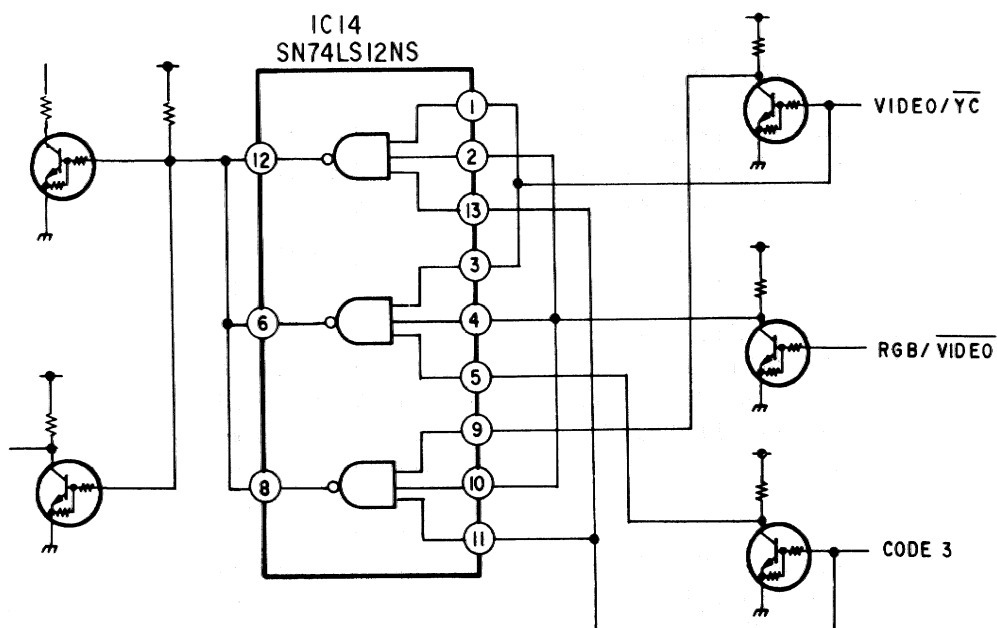


Fig. 1-5.

3-2. CIRCUIT OPERATION OF BB BOARD

3-2-1. Signal Switching Circuit

IC404, 405, 407 and the circuit around these ICs forms a signal switching circuit. It selects a video signal from (1) R.G.B. signal, (2) VIDEO signal, (3) Y/C signal, (4) color difference signal (these 4 signals enter from SLOT A, SLOT B and a switcher), and (5) VIDEO signal, (6) Y/C signal (these 2 signals enter from the panel of BB board).

1. Operation with R.G.B. Inputs (video section)

R.G.B. signals, entered to SLOT A or SLOT B, pass through BM board, then are applied to pins ⑧ of RL401, 402, 403 via pins 7a, 9a, 11a of BP-1 connector.

On the other hand, signals (entered from the switcher to BP-2 connector's pins ⑬, ⑪, ⑨ via a CCQ connector) enter to pins ⑭ of RL401, 402, 403.

Control to pin ① of each relay (RL) is done as shown in the table 2-1, and one of these two signals is output from pin ⑪. This signal is applied to transistors Q654, 710, and 757.

pin ① of RL	signal output from pin ⑪
H	pin ⑭ (CCQ)
L	pin ⑧ (SLOT A, B)

Table 2-1

Red signal passes Q651 and 653, then its pedestal level is clamped in a clamping circuit (Q650, IC410) as in case of pin ⑤ of IC410. The signal thus clamped passes a buffer (Q652), a switch (IC414) and an amplifier (IC418), then is output from pin 17b of connector BB-1.

Blue signal also passes similar circuits, and is output from pin 19b of connector BB-1.

Green signal passes "Clear Blue Circuit (see section 3-2-5)", circuits similar to Red or Blue signal, then is output from pin 18c of connector BB-1.

2. Operation with VIDEO Input (video section)

The signal, entered from VIDEO IN (panel of BB board) of the projector model, passes a resistor (R539) and a buffer (Q509), then enters to pin ⑫ of IC404.

Y-signal, entered from Y/C IN (panel of BB board), passes a buffer (Q516) then enters to pin ② of IC404. C signal passes a buffer (Q517) then enters to pin ⑤ of IC404.

Video signal, Y/C signal, and color difference signal (which enter to SLOT A and SLOT B) passes through R.G.B. signal lines via pins 7a, 9a, 11a of connector BB-1. Video signal, Y/C signal, and color difference signal (which enter to switcher) also enter to pins ⑬, ⑪ and ⑨ of connector BB-2, then enters to pins ⑭ of RL401, 402, 403. These signals are switched in accordance with the operating modes shown in the table 2-1, and is output from pin ⑪. The signals thus output pass Q506, Q507 and Q508 respectively, then enter to pins ⑬, ① and ③ of IC404.

IC404 selects its output signals from the signals described above and the signals entered from the panel of BB board. Thus, its pins ⑭, ⑮ and ④ output VIDEO, Y, C or R-Y, Y, R-Y, and these signals are sent to BA board via pins 5c, 4b, 5b of connector BB-1.

Table 2-2 shows the operating modes of IC404's control terminals:

V IN SEL (pin 23a of BB-1)	pins ⑨, ⑩, ⑪ of IC404	IC404's outputs (pins ⑭, ⑮, ④)
H	L	pins ⑫, ②, ⑤ (PJ main unit)
L	H	pins ⑬, ①, ③ (others)

Table 2-2

Signals, sent to BA board, are decoded and are applied to pins 8c, 9c, and 10c of BB-1 connector as R.G.B. signals. After that, each signal enters to pins ② of IC414, 415, 416, and passes through internal switching circuit, then is output from pins ⑪ of ICs. These signals pass circuits similar to in cases of R.G.B. input signals, then are output from pins 17b, 18c, 19b of connector BB-1.

3-2-2. SYNC Section

1. Operation with external SYNC

HD and VD, applied to SLOT A and SLOT B, enter to pins 1a and 2a of connector BB-1, then enter to pins ⑭ and ⑪ of IC405.

On the other hand, signals entered to switcher are applied to pins ⑦ and ⑥ of connector BB-2. After that, HD is terminated into a resistor (R501), and its peak is clamped to 0.7V by a diode (D501), then switched by transistors Q501, 502. Pulses with amplitude of 5Vp-p are output from collector of Q502, and enter to pin ⑬ of IC405.

VD also passes circuits similar to the ones in case of HD, and pulses output from the collector of Q504 enter to pin ⑩ of the IC. Operating mode of IC405 is controlled as shown in table 2-3, and signals are output from pins ⑫ and ⑨, then enter to pins ⑬ and ⑩ of IC407.

SLOT SEL (pin 23b of BB-1)	pin ① of IC405	outputs from IC405 (pins ⑫ and ⑨)
H	H	pins ⑬ and ⑩
L	L	pins ⑭ and ⑪

Table 2-3

In the case of VIDEO input, SYNC separation is done on BA board. HD is applied to pin 4a, and VD is applied to pin 5a of connector BB-1, then they enter to pins ⑭ and ⑪ of IC407, respectively. Operating mode of IC407 is controlled as shown in table 2-4, and signals output from pins ⑫ and ⑨ enter to 26c and 26a of connector BB-1.

pin ① of IC407	pins ⑫, ⑨, ⑦ of IC407
L	pins ⑭, ⑪, ⑤
H	pins ⑬, ⑩, ⑥

Table 2-4

2. Operation with SYNC on green

RL402 selects a signal from (1) GREEN signal entered from SLOT A and SLOT B, and (2) GREEN signal entered from switcher, as described in section 3-2-1 "Signal Switching Circuit". The signal thus selected is applied to pin ⑦ of IC401, then is output from pin ④.

The output signal passes through C762 and enter to IC417. It is output from pin ⑦ in negative polarity, and is MIXed with the pulses output from pin ⑫, then enters to pin ⑥ of IC407. Also, H SYNC enters to pin ⑤ of the IC

in Video input mode. The signal switched in accordance with modes shown in table 2-4 is output from pin ⑦, then sent to Y board via pin 25c of connector BB-1. Pin ⑨ is held to H level if input signal is 3-value SYNC.

3-2-3. AUDIO Section

A signal (R, L MIX signal), connected to switcher, enters to pins ② of IC408, 409 via pin ① of connector BB-2.

Also, R, L signals entered to SLOT A and SLOT B pass through pins 13a and 14a of connector BB-1, then MIXed by Q525, 526, 527, 532, 533, and enter to pins ⑫ of IC408, 409. Operating modes of IC408 and 409 are controlled as shown in Fig. 2-1, and they output signals from pin ⑭.

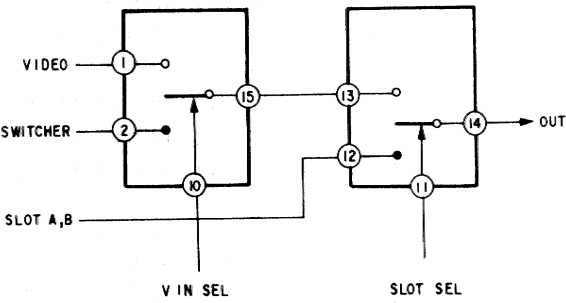


Fig. 2-1.

R, L signals thus switched enter to pins ⑥ and ④ of IC412, and are attenuated in accordance with the voltage applied to pins ② and ⑧ (VOL CONT terminals). R, L signals are output from pins ⑦ and ③, then sent to KA board via pins 3c and 3b of connector BB-1.

3-2-4. SIRCS Signal Circuit

The signal received by opto-receiver of the projector enters to pin 1c of connector BB-1, and the signal sent from the commander supplied with the main unit enters to pin 1b of connector BB-1, and the signal from the switcher enters to pin ③ of connector BB-2, respectively. The signal received by opto-receiver passes Q450, 451, a switch built in SIRCS IN terminal, then D450 and Q454, and is sent to pin 23c of connector BB-1. The signal is also sent to SIRCS OUT terminal via Q456. The signal sent from the commander supplied with the main unit enters to D450.

The signal from the switcher enters to Q453, then passes through the signal path described above.

The switch built in SIRCS IN terminal is turned OFF when a plug is inserted to SIRCS IN, and is turned ON when the plug is pulled out from SIRCS IN. Thus, wireless input of the main unit (signal from opto-receiver) is disabled when a plug is inserted, and the wired-input signal inserted to the terminal enters to D450 in return.

3-2-5. CLEAR BLUE Circuit

Red signal clamped by Q650 and IC410 appears on Q651's collector in an inverted waveform, and enters to Q652. Green signal enters to Q703 in a similar manner. Emitters of Q652 and Q703 are connected in common, and only the signal from transistor with lower base voltage (i.e., the signal with higher video level) appears on this point. The signal passes R708, 717, then enters to bases of Q704 (1/2) and Q707 (2/2). On the other hand, Blue signal appears on collector of Q751 in an inverted waveform, and enters to Q752. The signal passes R711, 714, then enters to bases of Q704 (2/2) and Q707 (1/2).

DC level of R, G signal is determined by the voltage supplied from Q753 (base voltage - V_{BE} determined by R760, 761, 762) at the time of polarity inversion, and DC level of B signal is determined by the voltage supplied from Q754.

Also, emitter of Q704 is connected to collector of Q705, and G signal's current flows in accordance with G signal applied to the base of Q705. Emitter of Q707 is connected to collector of Q709, and B signal's current flows in accordance with B signal applied to the base of Q709.

If C.B. SW (Clear Blue Switch) is turned OFF, then Q756 is turned ON. This causes the base voltage of Q704 (1/2) & Q707 (2/2) be held "Low", consequently Q704 (1/2) & Q707 (2/2) be turned OFF, and Q704 (2/2) & Q707 (1/2) be turned ON. Also, inverted waveform of G signal appears on collector of Q704 (2/2). The signal is inverted again in Q708, and enters to pin ④ of IC415.

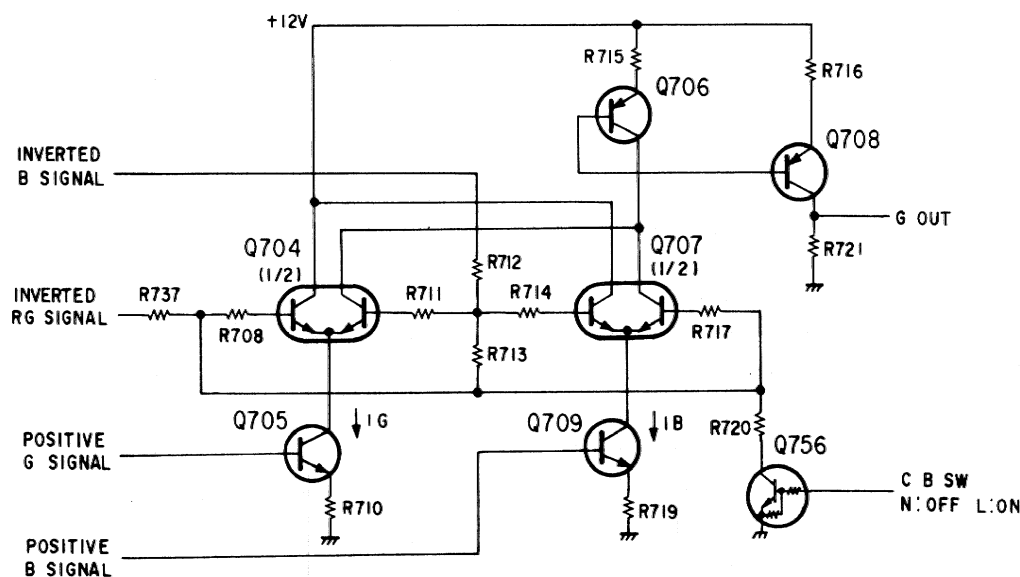


Fig. 2-2.

If C.B. SW is turned ON, the circuit compares base voltage of Q704 (1/2) & Q707 (2/2) to that of Q704 (2/2) & Q707 (1/2) to turn the transistor with higher base voltage ON. As the result, Q707 (2/2) & Q704 (1/2) are turned ON if B signal's level is higher than that of R, G signal, and MIXed signal of G and B signals enters to the base of Q708.

If B signal's level is lower than that of R, G signal, Q707 (1/2) & Q707 (2/2) are turned ON, and only G signal is applied to the base of Q708.

Thus, Clear Blue operation is to add G signal to B signal to cause Blue color be turned into Cyan color.

3-2-6. TEST SIGNAL Generator

Following test signals enter from connector BB-1 and are applied to IC413:

Test Signal	Pins of Connector BB-1	Pins of IC413
SG signal (test signals such as HATCH, DOT, etc.)	28a, 28b	12, 8
C.BRT signal (applies highlight and shade to picture in ZONE mode)	28c, 29c	7, 6
BOARDER signal (shadow portion of character signal)	29a, 29b	3, 2
PLUGE signal	27a, 27b	14, 13

Table. 2-5.

IC413 generates TEST signals based on input signals said above, and outputs them from pins ⑤ and ⑩. The test signal thus output enters to pins ⑦ and ⑧ of IC414, 415, 416, and is switched by NOR/TEST and VIDEO/RGB signals applied to pins ⑤ and ⑥ of these ICs, then is output from pin ⑪ of ICs.

Also, RGB character signals entered from pins 30A, 30B, 30C, 31C, 31A, 31B of connector BB-1 are applied to pins ⑨ and ⑩ of IC414, 415, 416, and are output after superimposed on RGB, VIDEO, and TEST signals applied to pins ②, ④, ⑦, ⑧ of ICs.

3-2-7. CODE Generator

Codes are generated by IC422, 423, 424, and transistors, diodes located around these ICs. Relationship between input and output signals is as shown in a table below:

signal applied to PJ			VIDEO	Y/C	col. dif.	col. dif. IDTV	col. dif. IDTV	RGB 2-V'	RGB 3-V'	HD 2-V'	HD 3-V'
BB IN	RGB/VIDEO	BB-1 3A BB-2 pin ⑤	L	L	M	M	M	H	H	H	H
	VIDEO/YC	BB-1 2B BB-2 pin ④	H	L	H	L	M	—	—	—	—
	HDVS SEL	BB-1 22A	H	H	H	H	H	H	H	L	L
BB OUT	VIDEO/YC	BB-1 25B	H	L	H	L	L	—	—	—	—
	RGB/VIDEO	BB-1 25A	L	L	L	L	L	H	H	H	H
	TRI/NOT	BB-1 24C	—	—	—	L	H	L	H	L	H
	CODE 3	BB-1 26B	H	H	L	L	L	H	H	L	L

*: 2V → 2-values, 3V → 3-values

—: don't care

Table. 2-6.

3-3. CIRCUIT OPERATION OF CA (RG) AND CA (B) BOARDS

Major function of these boards are video signal processing in R.G.B channel, video output, AUTO BACKGROUND circuit, single-tube ABL circuit, peak ABL circuit, Σ ABL circuit, and G1 BLANKING circuit.

3-3-1. Video Signal Processing (TY885002A)

Signal processing such as controls, cut-off switches, blanking, pedestal clamp, etc., to Background, Drive, Contrast, Brightness is done using hybrid ICs IC104, 204, and 304 (TY885002A). Fig. 1 shows the block diagram of this hybrid IC. This hybrid IC operates by entering various pulses with amplitude of 5Vp-p.

Video signal enters to pin ② with capacitor-coupling, and is clamped at its back-porch by B.P.C.P. applied to pin ⑤.

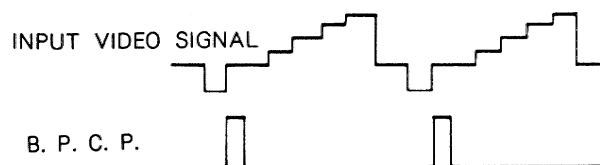


Fig. 3-2.

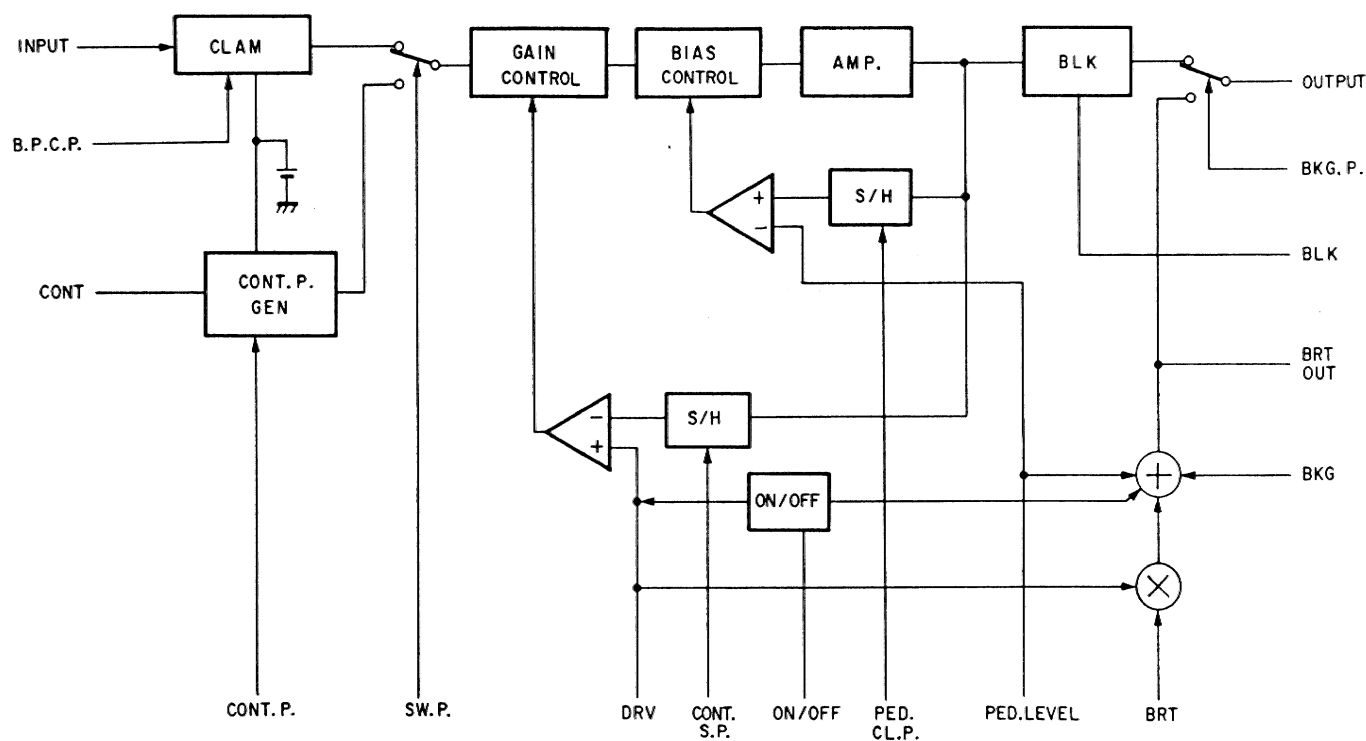


Fig. 3-1. TY885002 Block Diagram

After that, a pulse for gain control (CONTRAST pulse) is inserted to H. BLK interval of the video signal using switching pulses (SW.P.) entered to pin ⑭. Insert timing of CONTRAST pulse is determined by the pulse applied to pin ⑫, and its amplitude is controlled by DC voltage applied to pin ⑬.

After insertion of CONTRAST pulses, video signal passes a GAIN CONTROL amplifier, and is pedestal-clamped by Ped. Cl. P (pin ⑩) with the timing shown in Fig. 3-3. The IC samples and holds the amplitude of CONTRAST pulse to compare it to reference C. Based on error voltage between the two, the IC controls gain of the GAIN CONTROL amplifier. That is, a feedback is done to make the amplitude of CONTRAST PULSE be equal to the value of reference C.

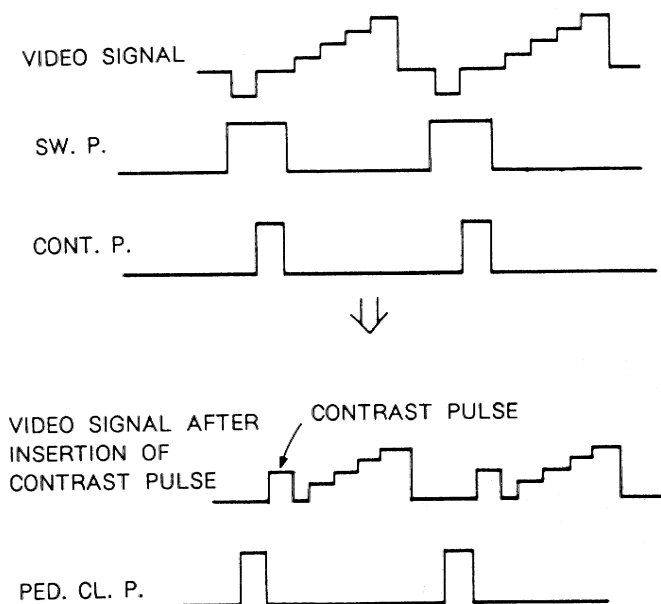


Fig. 3-3.

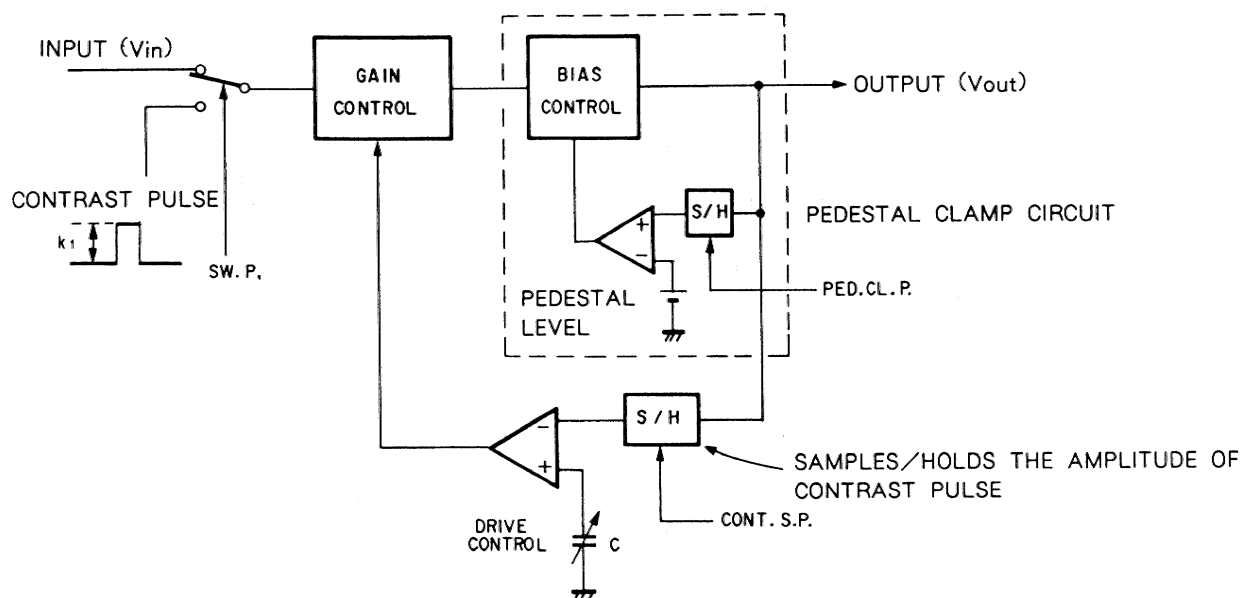


Fig. 3-4.

Contrast control is done by changing k_1 (changing DC voltage on pin ②), and Drive control is done by changing c (changing DC voltage on pin ⑨).

With this technic, control to CONTRAST and DRIVE is done using only a single gain-control amplifier.

After control to CONTRAST and DRIVE completed, blanking is done to the video signal using BLANKING PULSE applied to pin ⑤ (Fig. 3-6).

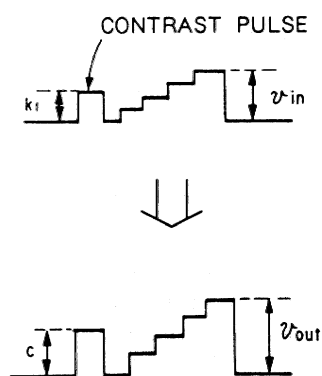


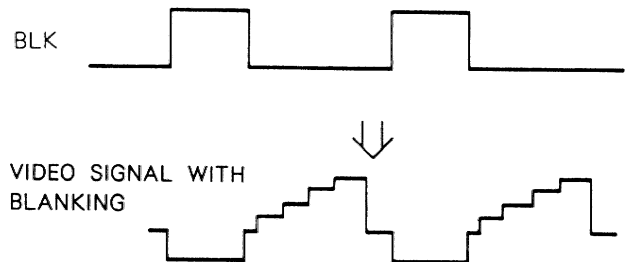
Fig. 3-5.

As shown in Fig. 3-5, gain in this stage (G_v) is calculated using following equation:

$$G_v = \frac{V_{out}}{V_{in}} = \frac{c}{k_1}$$

where: k_1 = amplitude of input CONTRAST PULSE
 c = amplitude of output CONTRAST PULSE

VIDEO SIGNAL AFTER
CONTRAST/DRIVE
CONTROL



VIDEO SIGNAL WITH
BLANKING

Fig. 3-6.

A pulse (BRT. Pulse) for brightness and background control is inserted to V. BLK interval of video signal. Timing of this pulse is determined by the pulse applied to pin ⑦, and its amplitude is controlled by current sunk into pin ⑧ (BKG terminal) and voltage applied to pin ⑩ (BRT terminal). Thus, video signal with BRT. Pulse inserted is output from pin ③. Pedestal level of the output video signal is constant, and information concerning BRIGHT and BACKGROUND is provided in the amplitude of BRT. Pulse. That is, pedestal level, hence brightness of picture, changes in accordance with the change of BRT. Pulse's amplitude by maintaining the cathode current at the time of BRT. Pulse constant (refer to 3-4. AUTO BACKGROUND circuit section).

3-3-2 γ -Correction Circuit

For correction of white balance at the intermediate level, γ -correction circuits are installed between signal-processing hybrid ICs (IC104, 304) and video output ICs (IC101, 301) on Red and Blue channels.

γ -correction circuit in Red channel has configuration shown in Fig. 3-7.

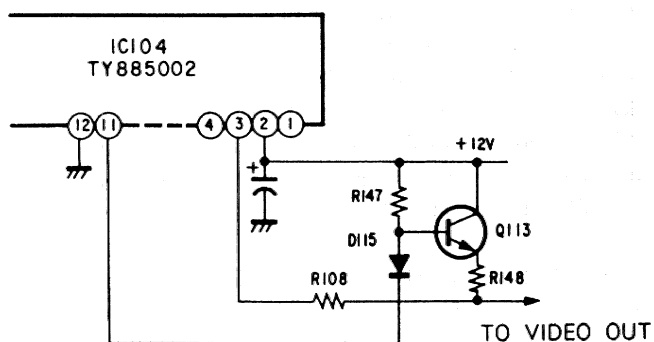


Fig. 3-7

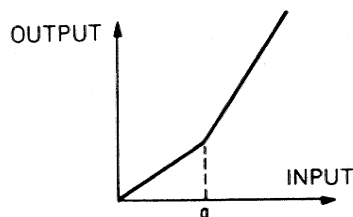


Fig. 3-8. γ -correction characteristic in Red channel

This circuit shows bending-characteristic as shown in Fig. 8.

Because the pedestal level is constant in this signal-processing circuit system, it is necessary to change the location of bending point (point-a in Fig. 3-8) of γ -characteristic in accordance with brightness level.

To achieve this, DC output voltage from pin ⑪ (BRT OUT terminal) of TY885002A is applied to the base of Q113 via D115 to change the location of bending point in accordance with brightness level because amplitude of this DC voltage is same with that of BRT. Pulse to be inserted into video signal.

In this case, the signal level at the bending point is almost same with the level of BRT. Pulse.

IC305 (TY911504) is used in γ -correction circuit for Blue channel.

This hybrid IC shows a curved, bending characteristic as shown in Fig. 3-9.

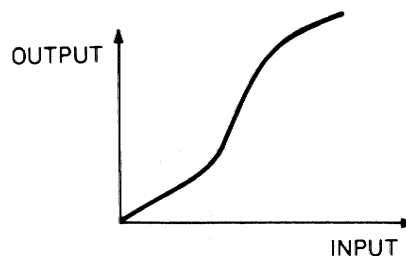


Fig. 3-9. γ -correction characteristic in Blue channel

Also it is necessary to change the location of bending point in accordance with brightness level, in this case however, it is done by connecting pin ⑪ (BRT OUT terminal) of IC304 to pin ⑦ of IC305.

Input terminal of IC305 (TY911504) is pin ⑩, and video signal (output from TY885002A) is applied to it. Also, the pedestal level (DC voltage) of the video signal is applied to pin ⑨. Video signal with γ -correction is output from pin ③ of this IC.

3-3-3. Video Out

A hybrid IC called "video pack" is used in video output circuit. Internal configuration of this IC consists of an ordinary cascode amplifier with resistive load and a complimentary buffer.

3-3-4. Auto Background Circuit

(Red channel is described here, but operation is same in Blue and Green channels)

This circuit prevents change in background (hence white balance) of picture caused by drift in Ekco of CRT, etc. This is achieved by inserting reference pulses (BRT. Pulse) to V. BLK interval of video signal to detect the cathode current at the reference pulse, then feedbacking is done to maintain the current thus detected constant. BRT pulse with 2H duration is inserted to V. BLK interval, and its timing pulse is applied to pin ⑦ of signal-processing hybrid IC (TY885002A). Detection of cathode current is done as follows: Q104 is a constant current source, and in normal state of operation, its source current flows into the base of Q105 to turn Q105 OFF. Q107 is disabled in this state, and the cathode current passes collector-emitter junction of Q105 and flows into emitter of Q103. In detecting cathode current at the timing of BRT pulse, IkDS pulse with 3H duration (which includes BRT pulse) is applied to the base of Q106 via Q112 to turn Q106 ON.

Accordingly, current from constant current source (Q104) flows into collector of Q106, and Q105 is turned OFF. This causes cathode current flow from emitter to collector of Q107. This collector current is converted into voltage by detecting it using R135. The cathode current thus converted into voltage passes a voltage follower (2/2 of IC102), and is sampled and held by Q111, R142, C119, then is applied to + input terminal of a comparator (1/2 of IC102) to compare it to a constant voltage (about 0.5V). The error voltage is applied to the base of Q101 via D112, then passes Q102, Q115, and controls G1 voltage. That is, feedbacking to control G1 voltage is performed by maintaining cathode current at the timing of BRT pulse constant (about $5\mu A$).

AUTO BACKGROUND circuit operates as described above, however, its operation may be disabled (control to Background and Brightness is disabled in this case) using AUTO ON/OFF control line. AUTO BACKGROUND circuit operates if this control line is OPEN, but connecting the control line to GND causes Q109 and Q110 to be turned ON, and output voltage from IC102 (1/2) becomes about -12V to turn D112 OFF. Also, Q108 is turned ON and R137 is connected to +12V line. A constant voltage is applied to the base of Q101, and keeps G1 voltage to a fixed level, and AUTO BACKGROUND circuit stops its operation.

3-3-5. Single-tube ABL Circuit

In normal state of operation (when IkDS pulse is LOW), cathode current of Red channel is added to the current of constant-current source (Q104), and flows from emitter to collector of Q103, then is converted into voltage using R130 and R32. The voltage is integrated by R37 and C19, then enters to the base of Q18. In same manner, cathode current of Green and Blue channels enter into bases of Q17 and Q16. Because emitters of Q16, Q17, and Q18 are connected together, voltage with the highest level out of R, G, and B passes an inverted amplifier (2/2 of IC8) via Q19, and enters to a comparator (Q15). If one of cathode current of R, G and B exceeds a level, Q15 is turned ON to decrease the voltage on CONTRAST control line, hence CONTRAST of picture.

3-3-6. Peak ABL Circuit

Cathode current detection section in this circuit is common with that of Single-tube ABL circuit above. Cathode current detected in R, G, B channels are MIXed by R34, R33, and R32. It passes an inverted amplifier (1/2 of IC8) then enters to a comparator (Q14). If the MIXed cathode current exceeds a level, Q14 is turned ON to decrease the voltage on CONTRAST control line, hence CONTRAST of picture.

3-3-7. Σ ABL Circuit

ABL voltage, detected from the secondary winding of flyback transformer, enters from pin ③ of CAB-7 and is applied to the base of Q30. The ABL voltage is compared to the base voltage of Q31. If it becomes lower than the base voltage of Q31, Q31 is turned ON to decrease the voltage on CONTRAST control line, hence CONTRAST of picture.

3-3-8 Generators of Various Pulses

Various pulses, used in processing video signals, are generated in IC4 to IC7. Fig. 3-12 shows the timing chart of these various pulses. Fig. 3-13 is the timing chart of pulses in H period. Most of signal processing pulses are generated in IC5 (MB675429: a gate array). In addition to HD and VD, a 1/2H pulse which rises at the center of HD pulse is required as input to MB675429. This 1/2H pulse is generated by a

monostable multi-vibrator IC4. For blanking pulses, transistors Q8 to Q10 prevent blanking during interval of IkDS pulse because no blanking is allowed during interval of BRT pulse for BACKGROUND control (interval of IkDS pulse includes the interval of BRT pulse). Also, a circuit (consists of C22, R42, D12, and D13) is used to perform blanking for a short time at power ON to projector. A circuit (consists of Q11, Q12, D14, D15, R48, and C26) is used to perform blanking at power OFF of the projector.

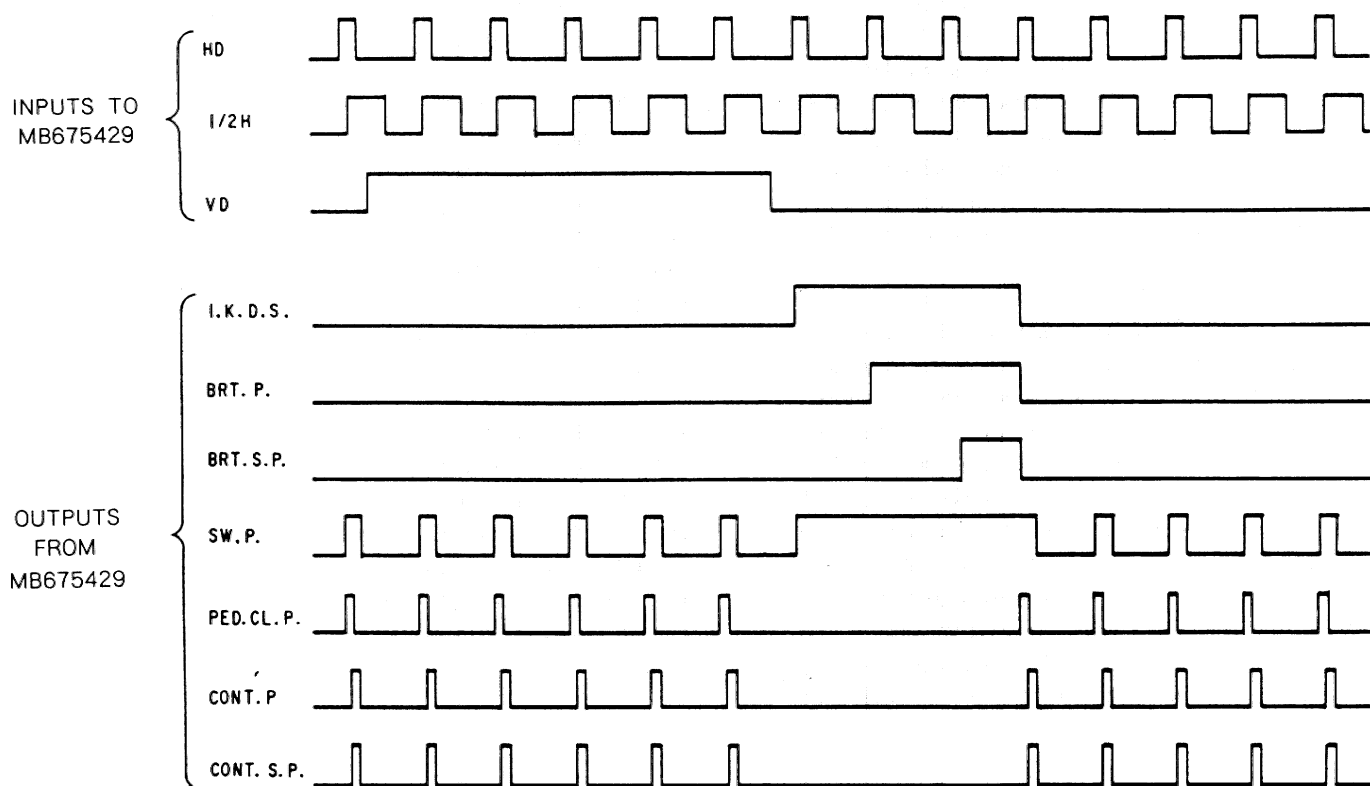


Fig. 3-12. Timing chart of various pulses

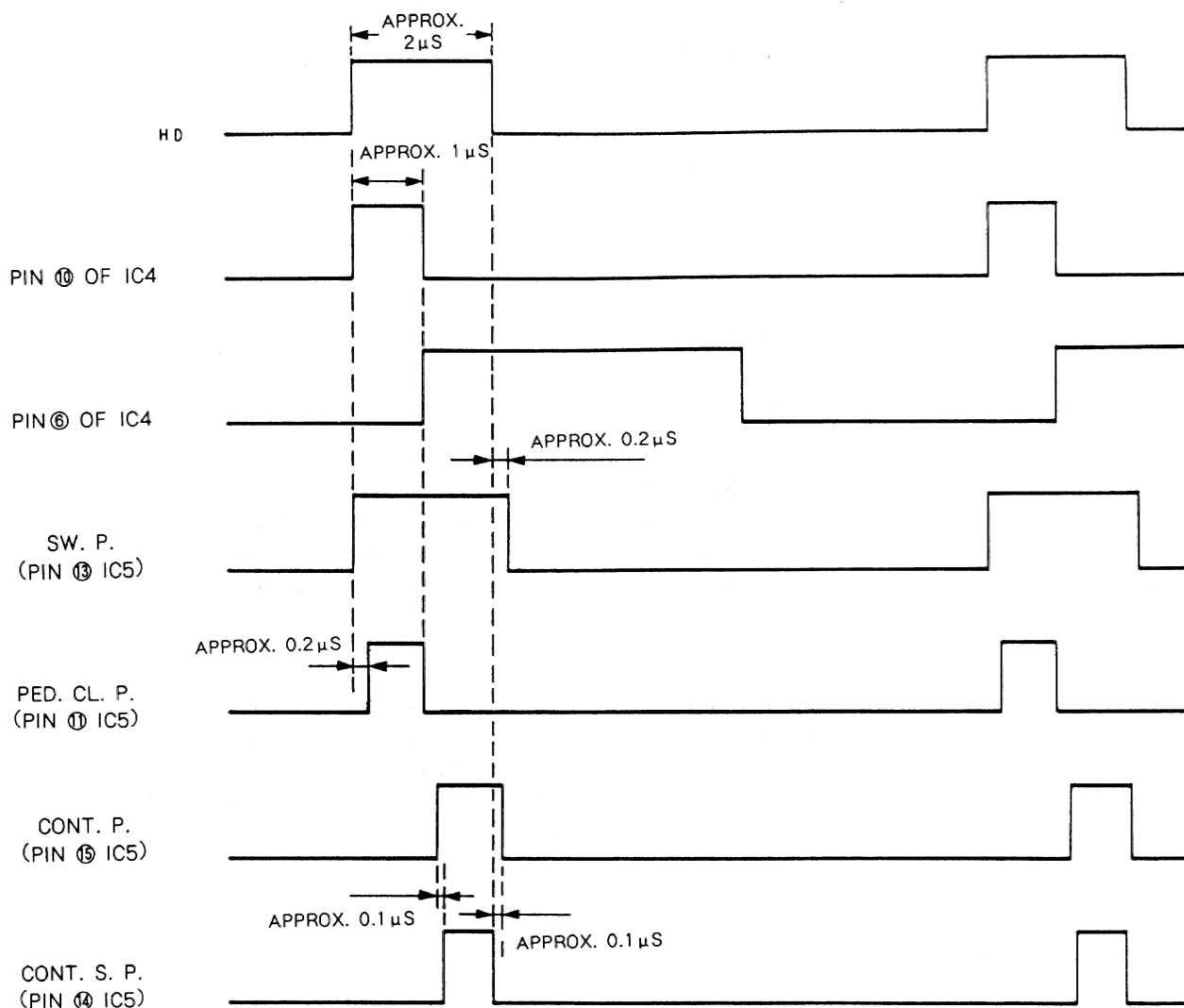


Fig. 3-13. Timing Chart of Pulses in H-period

3-3-9 $\pm 12V$ Line Protector

Power supply to this projector is cut off by connecting pin ⑩ or pin ⑫ of CAR-4 to GND. Power supply is cut-off to protect the projector when $\pm 12V$ lines on CA (RG) or CA (B) board are short-circuited or voltage on these lines decreases by some reasons. This circuit consists of Q2 to Q4 and components around them. If the voltage on +12V line decreases below zener voltage of D3, Q3 is turned OFF and Q2 is turned ON. This pulls pin ⑩ of CAR-4 down to GND. Also if voltage on -12V line increases, Q4 is turned ON. This pulls pin ⑫ of CAR-4 up to GND. Thus, protection for $\pm 12V$ line is activated.

3-3-10 G1 Blanking Circuit

Blanking pulse, output from pin ⑫ of IC6, passes through Q11 and enters to pins ⑤ (BLK terminal) of IC104, 204, and 304. Blanking pulse also enters to G1 blanking circuit. Blanking pulse from pin ② of CAB-5 and IkDS from pin ④ of CAB-5 are MIXed by transistors Q33 and Q32, then pass a buffer (Q34 and Q35) and enter to an inverting amplifier (Q36 to Q38).

First, let blanking pulse rise from Low to High. This causes Q36 and Q38 be turned ON, and Q37 be turned OFF. Voltage on Q38's collector is pulled down to about -100V. When blanking pulse falls from High to Low, Q36 and Q38 are turned OFF, and Q37 is turned ON. Voltage of Q38's collector increases by a summed voltage (24V) across zener diodes D33 and D34 up from about -100V. Thus, blanking pulse of 24Vp-p with its lower limit at about -100V is generated. The blanking pulse enters to G1 control circuits, and after level-shifted, is applied to G1 of R, G, and B channels.

3-4. CIRCUIT OPERATION OF DA BOARD

Functions on DA board may be classified as shown below:

- (1) AFC circuit
- (2) V. HOLD circuit
- (3) H.V. SHIFT circuit
- (4) BLK circuit
- (5) Registration waveform generator
- (6) Miscellaneous

This section describes the signal flow based on the block diagram of DA board shown in Fig. 4-1

H. PULSE (12Vp-p) generated in retrace time of horizontal deflection enters to 7-B from E board. The pulse is distributed to 3 circuits. One enters to AD. HD waveform generator (1) to generate pulse in timing advanced by 1 to 3 μ s than HD. This is sent to registration waveform generator as trigger pulse for horizontal registration waveforms. The 2nd one enters to H. BLK circuit (2) and is used as the trigger to H. BLK. The 3rd passes HF. HD circuit (3) and H. SHIFT circuit, then enters to circuit (6). H. SYNC for AFC enters from 8-A.

From Y board, V. SYNC enters to 9-A. It passes V. SHIFT circuit (5) and enters to V. HOLD circuit. Output from V. HOLD circuit is called as VD, and is sent to registration waveform generator (9) as the trigger to vertical registration waveforms.

External V. SIN generator (10) and H. SIN generator (11) are used because registration IC, used in the registration waveform generator, provides no SIN output.

To prevent beam concentration by too small raster size, a size ABL circuit (14) is used for protection from damage to CRT phosphor.

DA BOARD BLOCK DIAGRAM

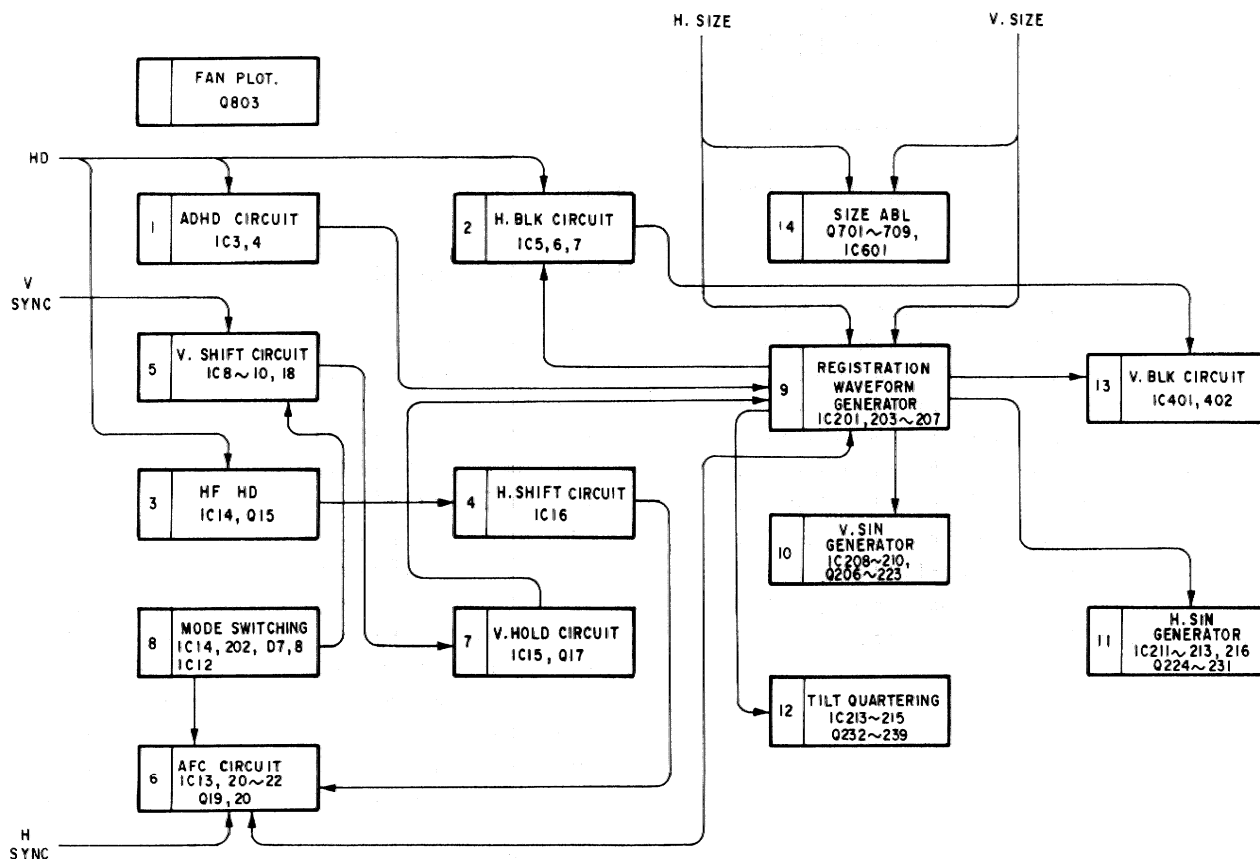


Fig. 4-1.

Basic Circuit on DA board (I)

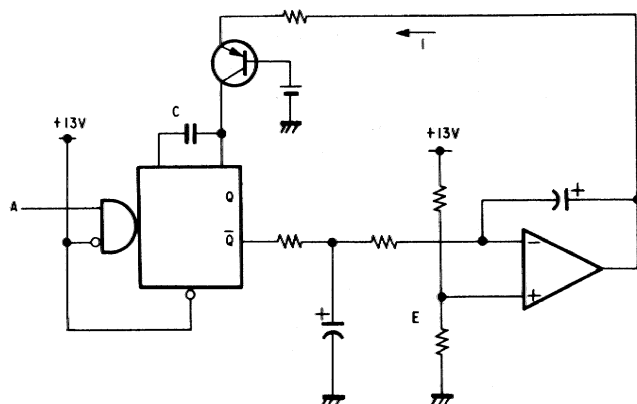


Fig. 4-2.

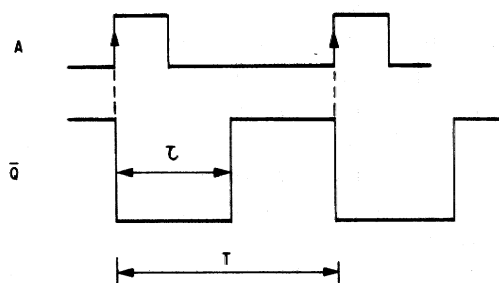


Fig. 4-3.

Using positive-going edge of square waveform of A input as the trigger, the basic circuit generates pulse with duty of τ/t at \bar{Q} output. Circuit shown above is a monostable multivibrator of feedback type, and feedback is done to make the integrated voltage of \bar{Q} output be equal to the reference voltage E of operational amplifier. Because $+B = 12V$, \bar{Q} output is the pulse with amplitude of 12V. Integrated voltage (E') of \bar{Q} output is calculated using following equation:

$$E' = (T - \tau) \times 12/T = E$$

where : T is the time of 1H or 1V

For example, when generating a pulse with duty of 50%, $\tau/T = 0.5$. You can calculate E by following equation :

$$E = (T - \tau) \times 12/T = (1 - \tau/T) \times 12 = 6 (V).$$

Basic Circuit on DA board (II)

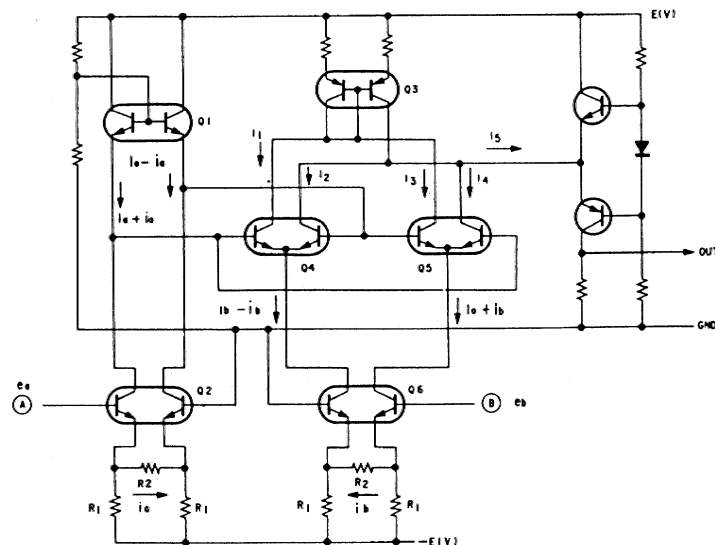


Fig. 4-4.

The circuit above is a multiplier with ea to Q2 and eb to Q6 as their inputs (ea and eb > 0).

I_0 (idling current at ea, eb = 0) is calculated using following equation :

$$I_0 = (E - V_{BE}) / R_1, i_a = e_a / R_2, i_b = e_b / R_2$$

where : i_a and i_b are increase in current caused by increase in input voltage

Following relationship exists between voltage and current in semiconductor:

$$i_0 = I_0 \left(e^{\frac{qV}{kT}} - 1 \right) \approx I_0 e^{\frac{qV}{kT}}$$

Taking logarithm of equation above, following equation is obtained:

$$\ln(i_0) = \ln(I_0) + \frac{qV}{kT}$$

Applying equation above to Q1 and Q2, then:

$$V = \frac{kT}{q} (\ln(i_b) - \ln(I_b))$$

$$V_s = E1 - \frac{kT}{q} (\ln(I_o + i_s) - \ln(I_b)) \dots\dots\dots(1)$$

$$V_b = E1 - \frac{kT}{q} (\ln(I_o - i_s) - \ln(I_b)) \dots\dots\dots(2)$$

$$V_s - V_b = \frac{kT}{q} (\ln \frac{(I_o + i_s)}{(I_o - i_s)}) \dots\dots\dots(3)$$

Applying the equation to Q4, Q5 and Q6 in similar way:

$$V_s - V_b = \frac{kT}{q} (\ln \frac{I_2}{I_1}) = \frac{kT}{q} (\ln \frac{I_3}{I_4}) \dots\dots\dots(4)$$

From equations (3) and (4),

$$\frac{I_2}{I_1} = \frac{I_o - i_s}{I_o + i_s} \dots\dots\dots(5)$$

$$\frac{I_3}{I_4} = \frac{I_o - i_s}{I_o + i_s} \dots\dots\dots(5)$$

From circuit diagram,

$$I_3 + I_4 = I_o + i_s \dots\dots\dots(7)$$

$$I_1 + I_2 = I_o - i_s \dots\dots\dots(8)$$

From equations (5), (6), (7) and (8),

$$I_1 = (I_o - i_s) (I_o - i_s) / 2i_o \dots\dots\dots(9)$$

$$I_2 = (I_o + i_s) (I_o - i_s) / 2i_o \dots\dots\dots(10)$$

$$I_3 = (I_o - i_s) (I_o + i_s) / 2i_o \dots\dots\dots(11)$$

$$I_4 = (I_o + i_s) (I_o + i_s) / 2i_o \dots\dots\dots(12)$$

Because $I_1 + I_3 = I_2 + I_4 + I_s$, by substitution of equations (9), (10), (11) and (12),

$$I_s = -2 i_s \cdot i_o / I_o$$

3-4-1. AD•HD Circuit

In correction of registration using SUB-DY, some delay occurs between correction waveform and picture movement on CRT screen because of various conditions such as eddy current, etc. To make the picture movement on CRT screen ideal, it is necessary to advance the timing of correction waveform by 0.5 to 1 μ S than that of HD pulse for horizontal deflection. Based on results of various experiments, the absolute value of this timing is nearly constant regardless of f_H .

Using positive-going edge of HD pulse as the trigger, this circuit generates a pulse with width of τ (pin ⑥ of IC3). The pulse width(τ) is wider by 0.5 to 1 μ S than that of HD pulse ($t = 0.5$ to 1 μ S). This pulse is integrated, and the result of integration is used as the reference.

Other monostable multivibrator generates a pulse using negative-going edge of HD pulse as its trigger. A feedback system is used to compare this pulse with the result of integration of \bar{Q} output (pin ⑨ of IC3).

The feedback system operates to make width of pulse on pin ⑥ of IC3 be equal to that on pin ⑨ of IC3. Because width of HD pulse is about 2 μ S, selecting component values to achieve pulse width τ be 2.5 to 3 μ S makes t be 0.5 to 1 μ S. Consequently, positive-going edge of waveform on pin ⑨ of IC3 virtually advances by 0.5 to 1 μ S than HD pulse. This is called as AD. HD, and is applied to the registration IC to be used as trigger for registration waveforms (refer to basic circuit on DA board (I)).

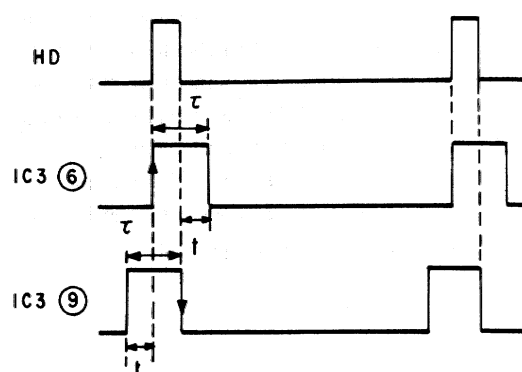


Fig. 4-5.

3-4-2. V. BLK Circuit

V. registration waveforms are generated using VD (V drive pulse after V. HOLD) as trigger. V. SAW is selected from waveforms above, and applied to IC401. In IC401, V. SAW is compared to DC voltage called BLK (T), (B), then is added to VD to generate V. BLK signal. DC voltage of BLK (T), (B) determines the timing when V. BLK be applied, and changing BLK (T), (B) causes pulse width on pin ⑦ of IC401 be changed, hence the position of V. BLK.

Changing V size also changes amplitude of V. SAW waveform, hence the pulse width of V. BLK. In this case, however, DC voltage called BLK (T), (B) does not change. So, BLK position on projector screen does not move.

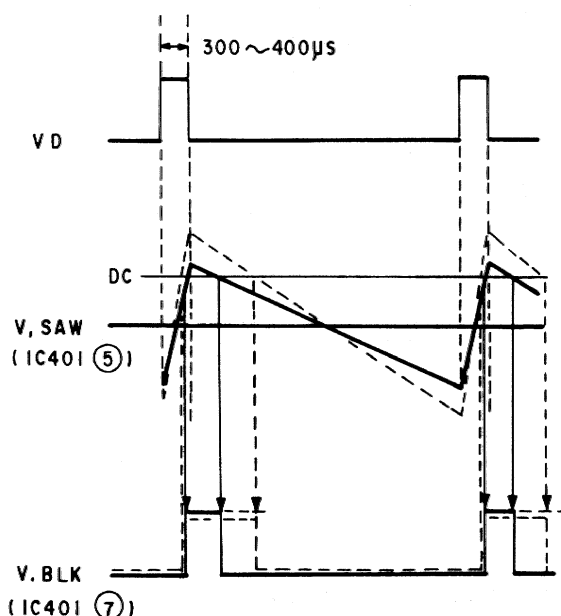


Fig. 4-6.

3-4-3. H. BLK Circuit

Generation of H. BLK is done based on a concept similar to the case of V. BLK. If constructed a circuit of system same with that of V. BLK, however, two BLK pulses are generated as shown in timing chart (right) because AD. HD is used as the trigger to generate registration correction waveforms. The reason is, H. SAW is generated in advanced timing using AD. HD.

To avoid this problem to occur, H. BLK pulse is generated using the negative-going edge of HD pulse as the trigger. Pulse width is determined in a same manner as in case of

V. BLK, that is, H. SAW registration correction waveform is compared to DC voltage called BLK (L), (R), and its integrated voltage is used as the reference.

H. SAW is applied to IC7, and is compared to DC voltage called BLK (L), (R).

Voltage obtained by integration of pulses output from pin ⑦ and pin ① of IC7 is the reference voltage of H. BLK (L), (R) respectively.

HD is applied to pin ④ of IC5 to generate a pulse with width of w . Generation of this pulse is done as follows: Reference voltage generated by IC7 enters to IC6. IC5 and IC6 forms a feedback loop to generate a pulse (H.BLK (L)) having same width with the pulse generated by comparison in IC7, at the timing of positive-going edge of HD.

In same manner, HD is applied to pin ⑫ of IC5 to generate a pulse with width of w' . This is H. BLK (R). H. BLK (L) and H. BLK (R) are generated separately, and are added together in IC402. (see timing chart to the right). (refer to basic circuit on DA board).

Decoder IC (IC402) adds together H. BLK and V. BLK said above to generate composite BLK signal.

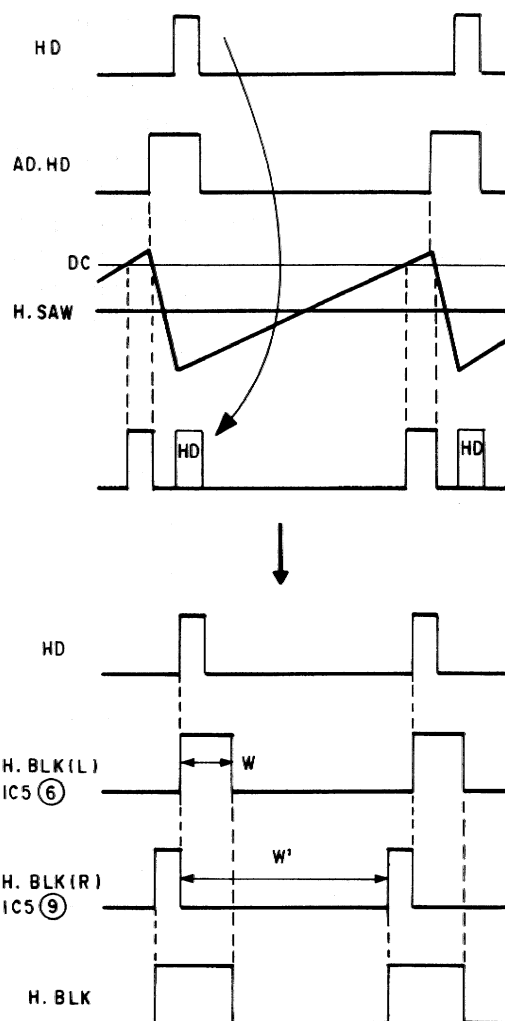


Fig. 4-7.

3-4-4. HF. HD Circuit

Result of integration of HD pulse is compared to $V_{cc}/2$ to generate a pulse being triggered at the center of HD pulse. This pulse is used in Y board to indicate center position of built-in signals.

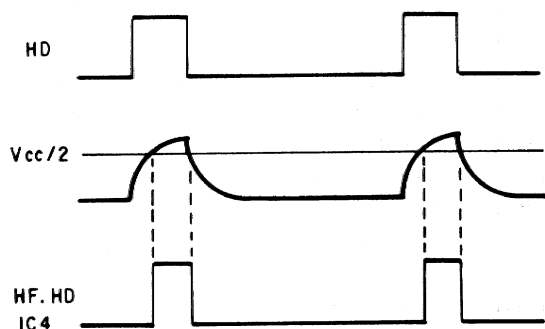


Fig. 4-8.

3-4-5. H. SHIFT Circuit

IC6 is H. SHIFT IC. This IC contains 3 set of "basic circuit (I) on DA board" connected in series.

HF. HD pulse is applied to pin ③, and is used as trigger to generate a square wave with duty of 50% in the 1st stage, and a square wave with variable duty of $50\% \pm 10\%$ in the 2nd stage. Based on result of the 2nd stage, the 3rd stage generates a square wave with duty of 50% to be used as return of H. Pulse for AFC. $\pm 10\%$ variable duty cycle in the 2nd stage causes output's duty cycle of the 3rd stage also change by $\pm 10\%$ if compared to the input pulse. AFC synchronization is done based on SYNC and H. Pulse. Shift of video is done by changing the phase of a signal which substitutes for H. Pulse. Pin ② is SHIFT cont. terminal, and pin ⑧ is out terminal.

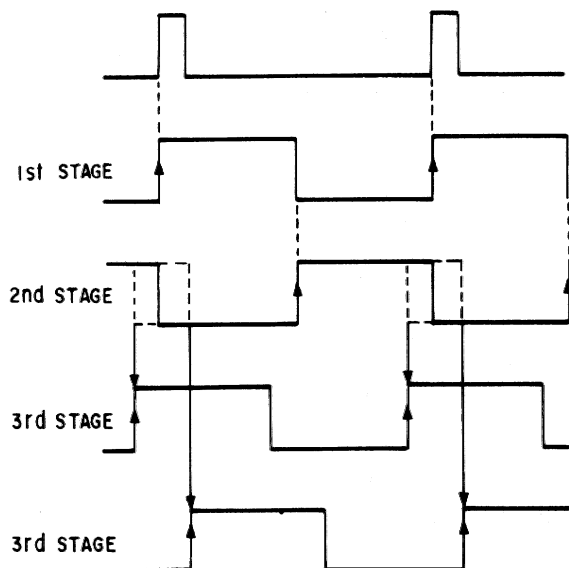


Fig. 4-9.

3-4-6. V. SHIFT Circuit

V. SHIFT circuit contains two circuits, i.e., NARROW V. SHIFT and WIDE V. SHIFT.

NARROW V. SHIFT circuit consists of IC10 and IC18, and WIDE V. SHIFT circuit consists of IC8 and IC9. IC10 is VIDEO V. SHIFT circuit, and IC12 selects one of these 3 signals in accordance with the type of input signal.

These circuits generate dummy V. SYNC signals which time-delayed to the original V. SYNC.

In WIDE V. SHIFT circuit, V. SYNC is converted to a pulse having amplitude of 12V using Q9. The signal is applied to pin ④ of IC8 to generate a pulse from Q output (pin ⑦ of IC8) with variable duty of 70% to 90%. Using this as trigger, monostable multivibrator of the next stage generates a pulse with duty of 20% (pin ⑨ of IC8). The pulse is delayed by 190% to 110% as compared to the original V. SYNC. In other words, timing of the pulse varies $\pm 10\%$ as compared to the original V. SYNC (refer to "basic circuit (I) on DA board").

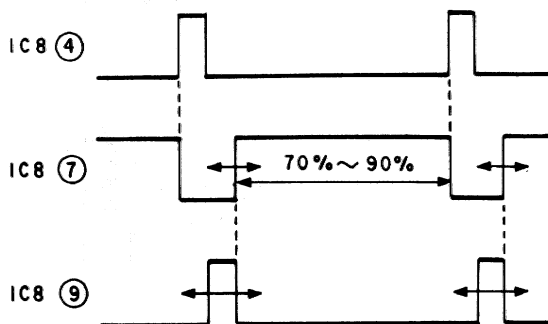


Fig. 4-10.

NOTE : In case of a special interlaced signal with different V period between adjacent fields, V jitter may occur if selected WIDE V. SHIFT circuit. Select NARROW V. SHIFT circuit described below in this case.

In NARROW V. SHIFT circuit, Q9's output is applied to pin ⑫ of IC10 to generate timing pulse delayed by 0% to 10% in ideal. Actually, minimum pulse width is limited to $200\mu\text{S}$ because of restriction by the circuit system used. But the pulse width may be varied up to 10% of 1V period.

Both WIDE V. SHIFT and NARROW V. SHIFT circuits are controlled by DC voltage called "V. SHIFT" on 27-C of connector (refer to "basic circuit (II) on DA board").

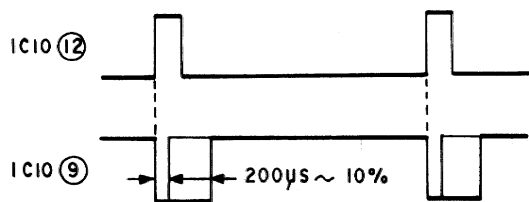


Fig. 4-11.

Because timing of front porch and back porch in video signal is different, VIDEO V. SHIFT signal is used to adjust (using RV5) picture position to come to the center of screen.

IC12 selects one of outputs from three V. SHIFT circuits, and IC13 generates dummy V. SYNC signal.

3-4-7. AFC Circuit

IC22 is jungle IC for AFC, and IC13, 20 and 21 are its peripheral circuit.

Pin ① of IC22 is SYNC IN terminal, and pin ② is SYNC SEP OUT terminal which outputs negative pulses with amplitude of 12V. It enters to pin ④ of IC13 to generate a pulse with width of w (pin ⑥ of IC13). The pulse is inverted (with its DC component be cut) in IC20 (pin ① of IC20), then after peak-hold, F-V conversion is performed. In this F-V conversion, RV2 is used to adjust for $V_{FV} = 2V$ at $f_H = 30\text{kHz}$. A current-mirror circuit (Q19, Q20) is used to convert this F-V voltage into current. Free-run frequency is determined by this current output and capacitors (C66, C67) connected to pin ⑤ of IC22. RV1 is used in fine adjustment of free-run frequency.

Pin ③ is H. Pulse's return input terminal, and actually H. SHIFT output described above is applied to pin ③. Error voltage obtained by comparison between H. Pulse's return input and H. SYNC applied to pin ① is output from pin ④, and is fed back to pin ⑤ to determine the free-run frequency.

On pin ⑤, a voltage is generated as result of charging/discharging of current to/from C66 and C67. This voltage is compared to the voltage internally determined in the IC to generate H. OSC pulse. The pulse is sent to E board, and drive pulse for H. deflection is generated in this board.

Described above is the AFC for RGB system. In the AFC for VIDEO system, however, F-V conversion technique is not used, and taking fluctuation of SYNC into consideration, f_0 current is determined by a resistive divider.

When VIDEO is selected, the output of F-V conversion is reset to zero using IC14. If F-V conversion voltage decreases under reference voltage, output of IC17 becomes OPEN. Free-run frequency is determined by F-V voltage for VIDEO, which is provided by a resistive divider R177, 178, 179, Q22, and RV3. Fine adjustment is done by RV3. Other signal routes are same with that of RGB system.

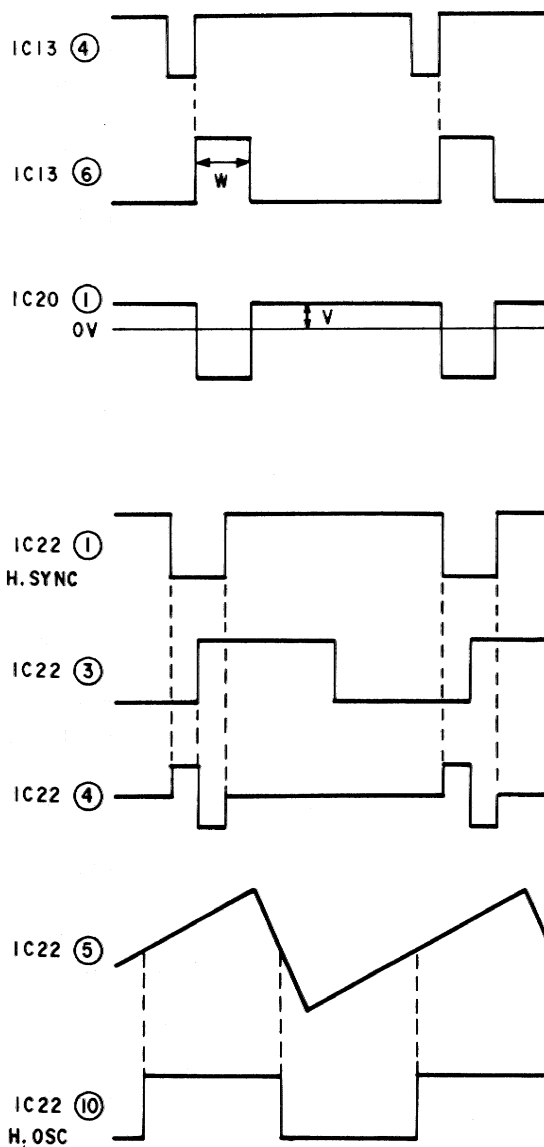


Fig. 4-12.

3-4-8. V. HOLD Circuit

IC15 is V. HOLD IC. Pin ⑥ is V. SYNC IND terminal, and actually a SYNC selected from V. SHIFT circuit's output signal is applied to it. Pin ⑦ is SYNC SEP OUT terminal, and its output re-enters to pin ④, then is applied to V. HOLD section. RV4 is used to control F-V conversion for MULTI-SCAN V. HOLD, and it adjusts fo of V. HOLD circuit.

Pin ② is V. HOLD output terminal, and V. HOLD is applied to correction waveform IC.

3-4-9. MODE Switching

This projector switches its AFC or V. SHIFT mode in accordance with VIDEO or RGB input. The switching is controlled from pin ① of IC14.

To avoid V. jitter, a V. SYNC before passing V. SHIFT circuits is selected.

If selected VIDEO and with no signal input, the system operates in RGB mode. The system operates in RGB mode when pin ① of IC14 is "H" level, and in VIDEO mode when it is "L" level.

INT/EXT	X	L	H	H
VID/TEST	L	H	H	H
NOR/TEST	X	H	L	H
pin ① of IC14	H	L	H	L

X: don't care

Table 4-1.

3-4-10. Registration Waveform Generator

IC201 is registration IC, the generator of registration waveforms.

Inputs to the IC are AD. HD described above and VD. AD. HD is applied to pin 24 as the trigger for H. correction waveform.

Triggering waveforms and corresponding output waveforms are as shown in the next page.

Pins 25 and 27 are amplitude control terminals for H and V respectively, with input level in 0.5V to 1V range.

In IC201, AGC is applied to SAW waveform generation only. Other waveforms are generated by multipliers based on SAW waveform.

For example, $H. PARA = H. SAW \times H. SAW$

$HS \times HS = H. SAW \times V. SAW$

$HP \times VS = H. SAW \times H. SAW \times V. SAW$

Accordingly, if H. SAW's amplitude decreases to 1/2, then H. PARA amplitude decreases to 1/4 and HP × VS amplitude decreases to 1/8.

IC203 to 207 are amplifiers for amplitude adjustment of waveforms.

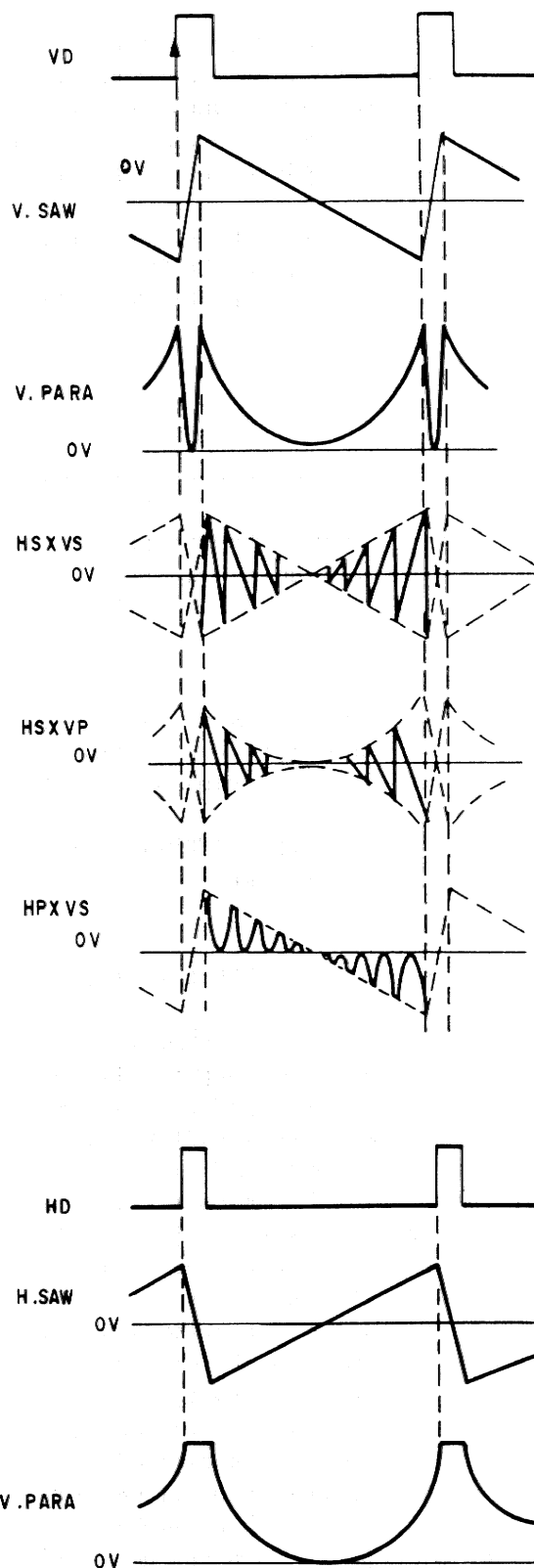


Fig. 4-13.

3-4-11. V. SIN Generator

Using a multiplier (described in "basic circuit (II) on DA board"), multiplication of V. SAW and H. SAW waveforms generated in the registration IC (IC201) is performed to generate V. SIN waveform.

Actually, IC208 and D201 is used to perform half-wave rectification on V. SAW waveform output from pin ⑦ of IC203 to obtain a waveform (D201 K in the diagram) at the cathode of D201. Also, IC209 is used to change the clamping position of V. PARA waveform at pin ① of IC204 to obtain a waveform at pin ① of IC209.

Entering waveforms of D201 K and pin ① of IC209 to "basic circuit (II) on DA board" generates a waveform of Q213 C (see diagram). This waveform is V. SIN 1.

Next, waveform at pin ⑦ of IC203 is applied to Q214 and Q215 to generate a waveform of Q215 E.

Multiplication of waveforms of Q215 E above and that of pin ① of IC209 is done to generate a waveform of Q223 C. This waveform is V. SIN 2.

Dividing V. SIN waveform by switching may cause noises at the dividing point, and results in deflection distortion called "Packman". To avoid this, V. SIN 1 and V. SIN 2 are generated separately from the beginning.

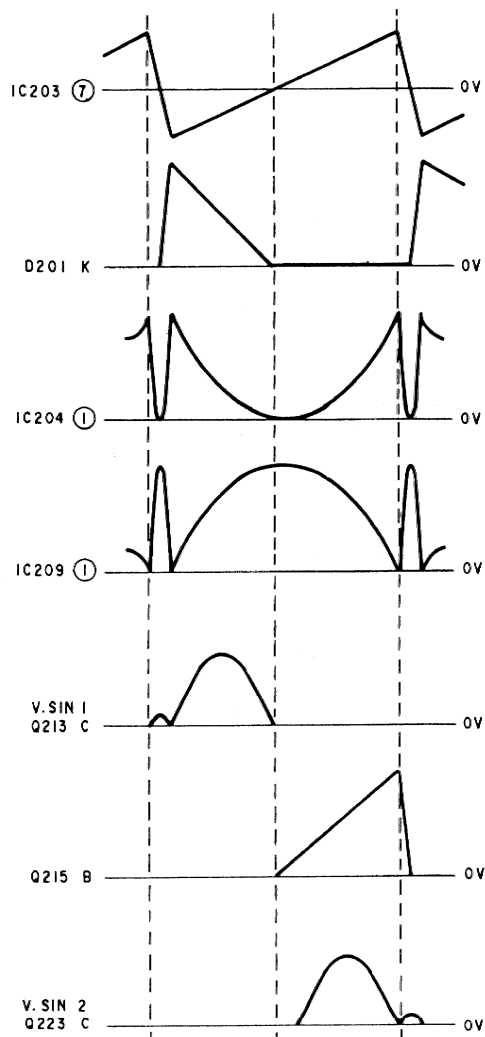


Fig. 4-14

3-4-12. H. SIN Generator

Configuration of H. SIN generator is similar to that of V. SIN generator.

Output of the registration IC (IC201) passes an amplifier (IC207) then full-wave rectification is done in IC211. Output waveform at pin ① of IC211 is as shown in the diagram.

Also, IC212 is used to change the clamping position of H. PARA waveform at pin ① of IC207 to obtain a waveform at pin ① of IC212.

Entering waveforms at pin ① of IC211 and at pin ① of IC212 to a "basic circuit (II) on DA board" generates waveform of Q231 C.

This waveform is applied to IC213, then it is divided in two using $1/2H$ waveform.

Waveform at pin ⑦ of IC216 is H. SIN 1, and at pin ① of IC216 is H. SIN 1.

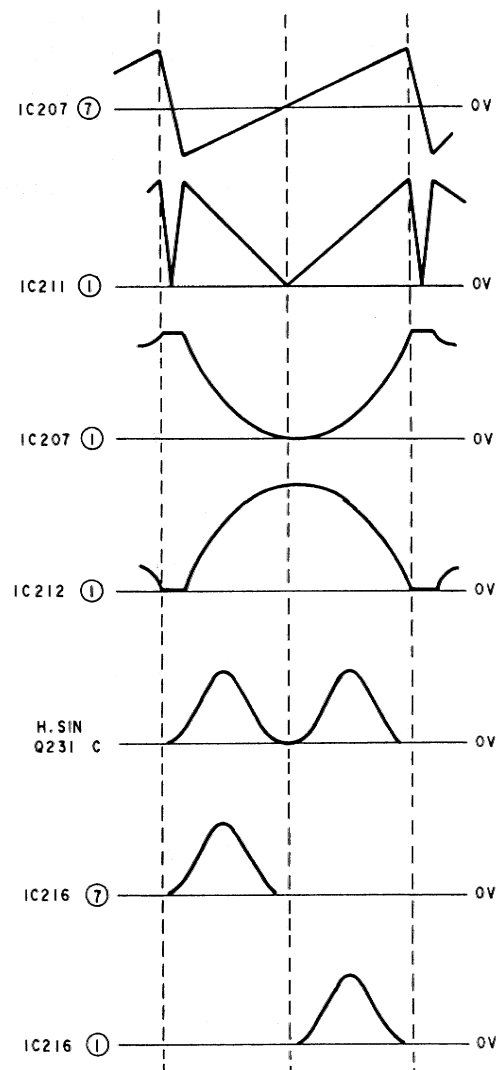


Fig. 4-15

3-4-13. TILT Quartering

TILT waveform is quartered to perform correction on areas A, B, C and D of screen (refer to illustration to the right).

Original waveform is $HS \times VS$ (output of pin ⑫ of IC201). This is divided in two (a and b) in IC213 using 1/2H square waveform output from pin ③ of IC201.

Dividing this again using 1/2V square waveform may generate waveforms A, B, C and D. But this technique causes noise with 1% to 2% of amplitude of original signal be superposed at the dividing point. This results in deflection distortion, and adverse effect called "Packman" occurs. (Noise in H direction does not affect deflection distortion.)

To avoid this, a differential emitter follower circuit is used in dividing V component instead of switching circuit. In the circuit of Q232 and Q233, for example, only positive domain of input waveform is output from emitter because one of bases is connected to GND. GND level in the original waveform, however, shifts down by $-0.7V$ (this corresponds to V_{BE}) in the resultant waveform. V_{BE} of Q233 is used for reversal compensation, and the level restores to GND potential. No switching noise is generated in this circuit, hence no deflection distortion, because it performs no switching operation. This dividing circuit consists of transistors Q232 to Q239.

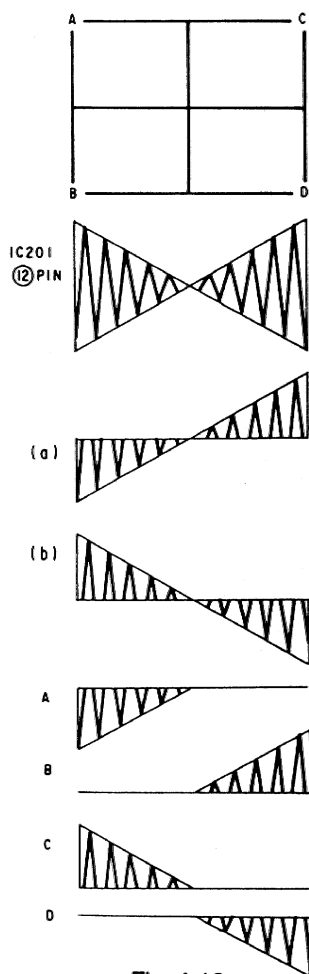


Fig. 4-16

3-4-14. SIZE ABL Circuit

Refer to "basic circuit (II) on DA board".

SIZE ABL circuit is a system shown in diagram to the right. When ABL is activated, voltage at point A is $-13.95V$ since ABL is $3.1mA$ in this projector set. Voltage at point B is $-6.975V$ when pin ① of IC15 is connected to GND.

Accordingly, ABL is activated if the voltage at point B becomes to $-6.975V$.

Changing voltage at pin ① of IC601 from GND to negative direction causes the voltage at point B decrease. So, ABL is activated before the voltage at point A reaches to $-13.95V$ (that is, before beam current reaches to $3.1mA$).

Decreasing the voltage at pin ① of IC601 in accordance with the decrease in raster size also decreases ABL point accordingly.

H. SIZE data and V. SIZE data are entered to a multiplier ("basic circuit (II) on DA board"). Its output is applied to an operational amplifier (IC601) to decrease the voltage at pin ① of IC601 in accordance with the decrease in raster size.

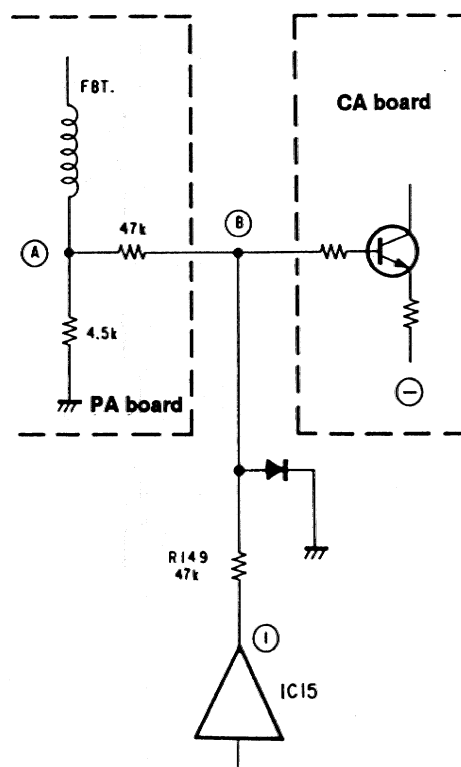


Fig. 4-17

3-5. CIRCUIT OPERATION OF DB BOARD

So far, potentiometers are used in registration controls, user controls, etc. This projector model, however, uses D/A converters in place of potentiometers to cope with remotely-controlled operation.

MB86023 is a D/A converter, and is used as an electronic attenuator with one-input/four-outputs. 36 units of MB86023 are used in this model. Each unit is equipped with 4 channels of output. This enables control to 144 outputs. Channel selection is done using addresses of 8-bit. IC505 to IC510 are address decoders. The D/A converter's resolution is 8-bit.

Description of MB86023

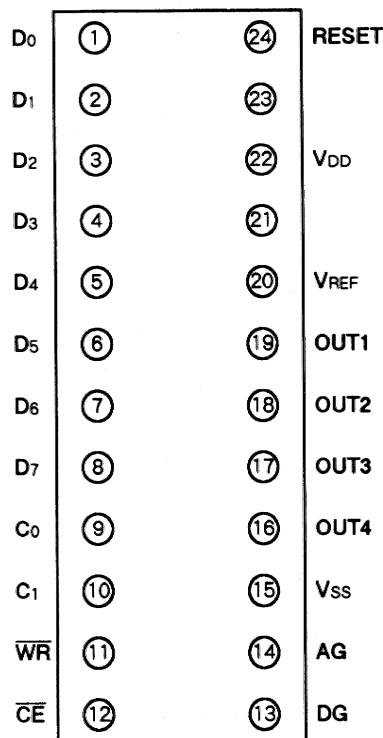


Fig. 5-1.

- ① to ⑧ DATA inputs: 8-bit parallel input
- ⑨ to ⑩ Channel Select: Selects/enables one of 4 output
- ⑪ LIGHT terminal: After reading data, CPU (Y board) sends a trigger to pull pin ⑪ momentarily down to "L" level. This latches the output.
- ⑫ CHIP ENABLE terminal: selects/enables one of 36 D/A converters. It is enabled when this terminal is "L".
- ⑬ digital GND
- ⑭ analog GND
- ⑮ - 5V input
- ⑯ to ⑰ OUTPUTs
- ⑲ Ref. voltage input
- ⑳ +5V input

Operation of MB86023

When DC voltage E (v) ($-2.5V < E < 2.5V$) is applied to pin ⑳ (V_{REF}):

For operation of this IC, its pin ⑫ (\overline{CE}) shall be "L" level. Also, the IC is equipped with 4 outputs. Output selection is done using combination of status on pin ⑨ and pin ⑩ (see the table 5-1.):

	pin ⑨	pin ⑩	pin ⑰	pin ⑯
pin ⑨	L	L	H	H
pin ⑩	L	H	L	H

Table 5-1.

If DATA is "FF", then E (V) same with V_{REF} is output from OUT terminal.

If DATA is "80", then 0 (V) is output from OUT terminal.

If DATA is "00", then $-E$ (V) is output from OUT terminal.

Almost linear change in output level by $E/128$ (v) per bit occurs with DATA of intermediate value. After reading DATA, a trigger is applied to pin ⑪ (\overline{WR}) to latch the DATA.

* When AC voltage is applied to V_{REF} terminal:

Operation of the IC is same, that is, output voltage changes in accordance with DATA as shown in Fig. 5-2.

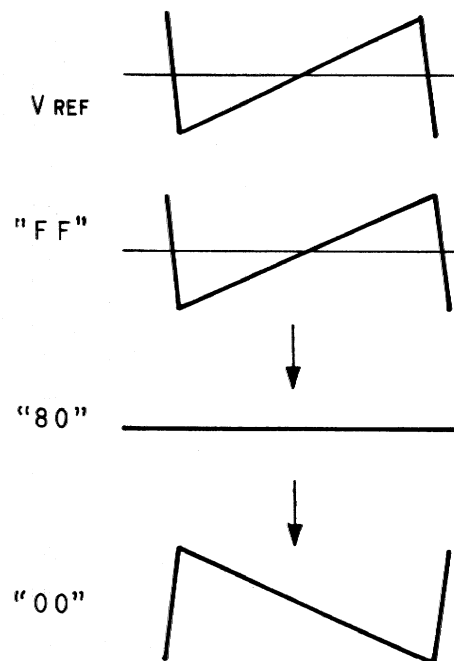


Fig. 5-2.

IC501 to IC504 are buffers, and IC505 to IC510 are address decoders. Table 5-2. shows pin numbers and corresponding output signal of ICs:

IC511	pin 19	H. SIZE	IC512	pin 19	H. SHIFT	IC513	pin 19	H. KEYS
	pin 18	H. CENT (G) 1		pin 18	H. CENT (G) 2		pin 18	H. SKEW (G)
	pin 17	H. CENT (R) 1		pin 17	H. CENT (R) 2		pin 17	H. SKEW (R)
	pin 16	H. CENT (B) 1		pin 16	H. CENT (B) 2		pin 16	H. SKEW (B)
IC514	pin 19	H. PIN	IC515	pin 19	—	IC516	pin 19	H. LIN BIAS
	pin 18	H. BOW (G)		pin 18	H. SIZE (G)		pin 18	H. LIN (G)
	pin 17	H. BOW (R)		pin 17	H. SIZE (R)		pin 17	H. LIN (R)
	pin 16	H. BOW (B)		pin 16	H. SIZE (B)		pin 16	H. LIN (B)
C517	pin 19	V. KEYS BIAS (B)	IC518	pin 19	—	IC519	pin 19	V. SIZE
	pin 18	—		pin 18	—		pin 18	V. CENT (G) 1
	pin 17	H. KEYS (R)		pin 17	H. PIN (R)		pin 17	V. CENT (R) 1
	pin 16	H. KEYS (B)		pin 16	H. PIN (B)		pin 16	V. CENT (B) 1
IC520	pin 19	V. SHIFT	IC521	pin 19	V. SIZE BIAS	IC522	pin 19	V. LIN BIAS
	pin 18	V. CENT (G) 2		pin 18	V. SIZE (G)		pin 18	V. LIN (G)
	pin 17	V. CENT (R) 2		pin 17	V. SIZE (R)		pin 17	V. LIN (R)
	pin 16	V. CENT (B) 2		pin 16	V. SIZE (B)		pin 16	V. LIN (B)
IC523	pin 19	—	IC524	pin 19	—	IC525	pin 19	V. KEYS BIAS (R)
	pin 18	V. SKEW (G)		pin 18	V. BOW (G)		pin 18	V. KEYS (G)
	pin 17	V. SKEW (R)		pin 17	V. BOW (R)		pin 17	V. KEYS (R)
	pin 16	V. SKEW (B)		pin 16	V. BOW (B)		pin 16	V. KEYS (B)
IC526	pin 19	—	IC527	pin 19	—	IC528	pin 19	—
	pin 18	V. PIN (G)		pin 18	H. ZONE 2 (G)		pin 18	H. ZONE 3 (G)
	pin 17	V. PIN (R)		pin 17	H. ZONE 2 (R)		pin 17	H. ZONE 3 (R)
	pin 16	V. PIN (B)		pin 16	H. ZONE 2 (B)		pin 16	H. ZONE 3 (B)
IC529	pin 19	H. ZONE 4 BIAS	IC530	pin 19	H. ZONE 5 BIAS	IC531	pin 19	—
	pin 18	H. ZONE 4 (G)		pin 18	H. ZONE 5 (G)		pin 18	H. ZONE 6 (G)
	pin 17	H. ZONE 4 (R)		pin 17	H. ZONE 5 (R)		pin 17	H. ZONE 6 (R)
	pin 16	H. ZONE 4 (B)		pin 16	H. ZONE 5 (B)		pin 16	H. ZONE 6 (B)
IC532	pin 18	H. ZONE 7 (G)	IC533	pin 18	H. ZONE 8 (G)	IC534	pin 18	H. ZONE 9 (G)
	pin 17	H. ZONE 7 (R)		pin 17	H. ZONE 8 (R)		pin 17	H. ZONE 9 (R)
	pin 16	H. ZONE 7 (B)		pin 16	H. ZONE 8 (B)		pin 16	H. ZONE 9 (B)
IC535	pin 18	V. ZONE 2 (G)	IC536	pin 18	V. ZONE 3 (G)	IC537	pin 18	V. ZONE 4 (G)
	pin 17	V. ZONE 2 (R)		pin 17	V. ZONE 3 (R)		pin 17	V. ZONE 4 (R)
	pin 16	V. ZONE 2 (B)		pin 16	V. ZONE 3 (B)		pin 16	V. ZONE 4 (B)
IC538	pin 18	V. ZONE 5 (G)	IC539	pin 18	V. ZONE 6 (G)	IC540	pin 18	V. ZONE 7 (G)
	pin 17	V. ZONE 5 (R)		pin 17	V. ZONE 6 (R)		pin 17	V. ZONE 7 (R)
	pin 16	V. ZONE 5 (B)		pin 16	V. ZONE 6 (B)		pin 16	V. ZONE 7 (B)
IC541	pin 19	—	IC542	pin 19	—	IC543	pin 19	SHARPNESS
	pin 18	H. ZONE 8 (G)		pin 18	H. ZONE 9 (G)		pin 18	COLOR
	pin 17	H. ZONE 8 (R)		pin 17	H. ZONE 9 (R)		pin 17	HUE
	pin 16	H. ZONE 8 (B)		pin 16	H. ZONE 9 (B)		pin 16	VOLUME
IC544	pin 19	DRIVE (G)	IC545	pin 19	BACK GROUND (G)	IC546	pin 19	BLANKING (T)
	pin 18	DRIVE (R)		pin 18	BACK GRAUND (R)		pin 18	BLANKING (B)
	pin 17	DRIVE (B)		pin 17	BACK GRAUND (B)		pin 17	BLANKING (L)
	pin 16	CONTRAST		pin 16	BRIGHT		pin 16	BLANKING (R)

Table 5-2

3-6. CIRCUIT OPERATION OF DD BOARD

3-6-1. Functions

This circuit generates ZONE correction waveforms required in ZONE adjustment in registration adjustment procedures.

3-6-2. Description of Operation

Generation of ZONE correction waveforms:

Using multipliers and switching circuits, the circuit generates 12 waveforms required exclusively in "divided-by-21" ZONE correction.

Q35 to Q37 generate pulses for 1/2V and 1/2H switching operation required in switching circuits. 1/2V pulses are applied to one of bases of a transistor pair Q37, and the reference DC voltage is applied to the other base of the pair. 1/2V pulses in mutually inverted phase are output from collectors of both transistors. In same manner, 1/2H pulses in mutually inverted phase are output from both collectors of Q36.

1/2 of IC4 performs operation of (VS1 - VS2) where VS1 and VS2 are sine waves of half cycle. Also 2/2 of IC4 performs (HS1 + HS2) operation.

Transistors Q11 to Q15, Q19 to Q23, and Q27 to Q31 form multipliers respectively. Q11 to Q15 multiply (VS1 - VS2) and H. PARA, and the result of multiplication is output from pin ① of Q13 in current form. Using a switching circuit (Q16 to Q18), this current is switched at the timing of 1/2V and 1/2H to output four correction waveforms from collectors of Q24 to Q26 in voltage form. Q19 to Q23 multiply (HS1 + HS2) and V. PARA, and the result of multiplication passes a switching circuit (Q24 to Q26), then four correction waveforms are output from collectors of transistor pairs Q25 and Q26.

Q27 to Q31 multiply (VS1 - VS2) and (HS1 + HS2), and the result of multiplication passes a switching circuit (Q32 to Q34), then four correction waveforms are output from collectors of transistor pairs Q33 and Q34.

Waveforms on DD board

1. Input waveforms

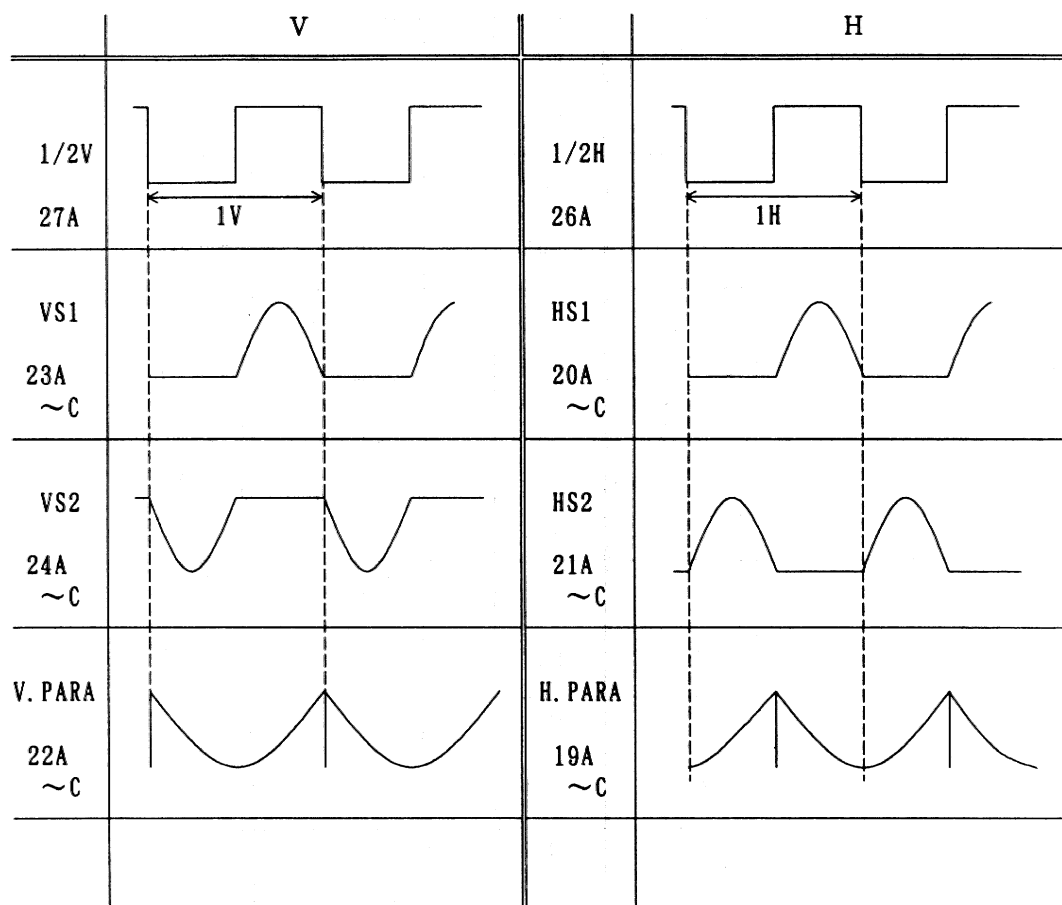


Fig.6-1.

2. Output waveforms

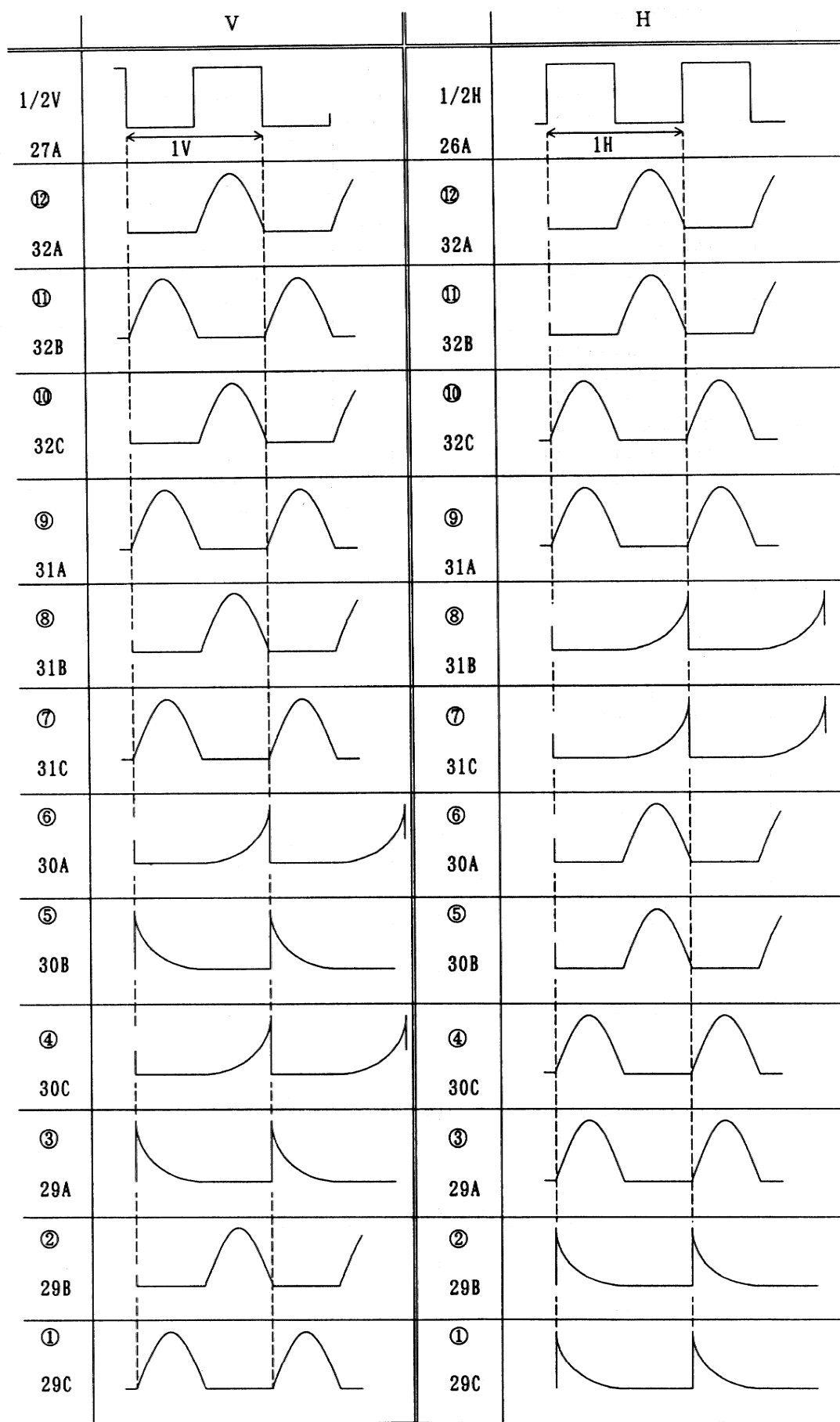


Fig.6-2.

[Block Diagram of DD board]

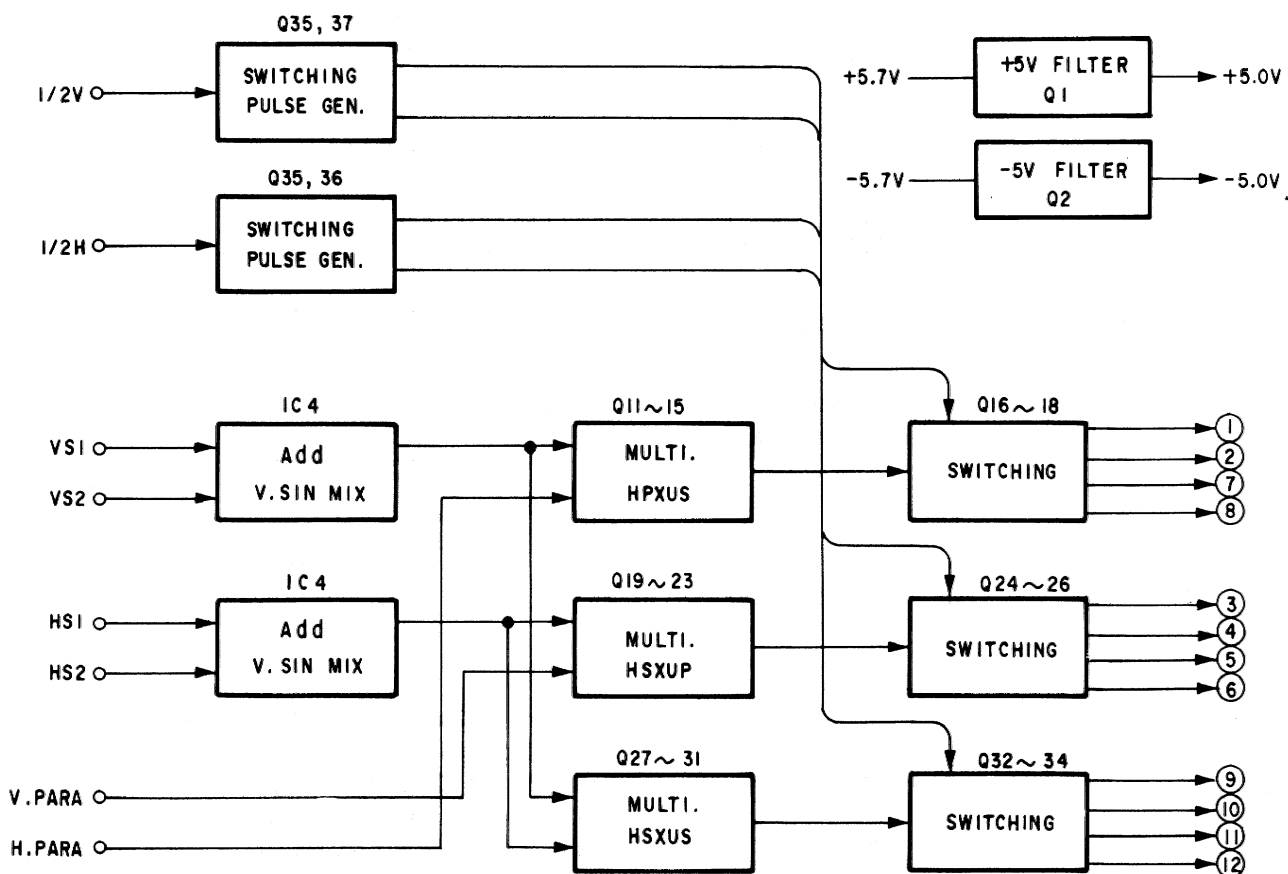


Fig.6-3.

3-7. CIRCUIT OPERATION OF DE BOARD

3-7-1. Functions

So far potentiometers were used in ZONE adjustment, however, this projector model uses D/A converters (digital attenuators) to cope with remotely-controlled ZONE adjustment. The function of this board is to synthesize attenuation waveforms for correction waveforms on ZONES ⑩ to ㉑ of divided-by-21 adjustment points.

3-7-2. Description of Operation

24 digital attenuators IC510 to IC529 and IC533 to IC536 (MB86023) are used to attenuate ZONE correction waveforms.

DATA signals D0 to D7, ADDRESS signals A0 to A7, and WRITE clock \overline{WR} enter to the board, and are distributed from buffers IC501 to IC504 (HD74HC244). Of signals from buffers, DATA signals D0 to D7, ADDRESS signals A0 and A1, and WRITE clock \overline{WR} are sent to digital attenuators IC510 to IC529, and IC533 to IC536 directly. ADDRESS signals A2 to A7 are decoded in a address decoder formed by IC505 to IC509 (HD74HC138), then sent to CE pins of digital attenuators IC510 to IC529 and IC533 to IC536 for chip selection.

Digital attenuator (MB86023, refer to Fig. 7-2) contains 4 channels of 8-bit D/A converter (voltage output). Each channel is equipped with a data latch circuit and an output buffer, and is selected by 2-bit data of A0 and A1, and operates independently.

Of these 4 channels, 3 channels are assigned to R, G and B signals respectively.

◁Setup for channel selection▷

A0	A1	ch.
L	L	0 (B)
H	L	1 (R)
L	H	2 (G)
H	H	3

Table 7-1.

Write timing of DATA:

DATA D0 to D7 are written at the positive-going edge of \overline{WR} while \overline{CE} signal is "L".

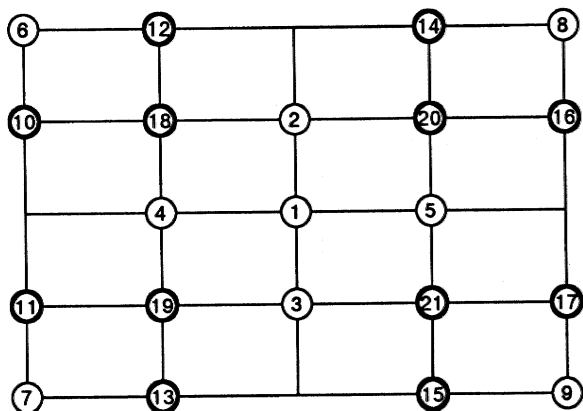


Fig. 7-1.

Adjustment points ① to ② in ZONE adjustment

* DE board performs waveform attenuation on points ⑩ to ⑪.

3-7-3. Description on MB86023

D0	①	②4	RESET
D1	②	②3	
D2	③	②2	V _{DD}
D3	④	②1	
D4	⑤	②0	V _{REF}
D5	⑥	①9	OUT1
D6	⑦	①8	OUT2
D7	⑧	①7	OUT3
A0	⑨	①6	OUT4
A1	⑩	①5	V _{SS}
WR	⑪	①4	AG
CE	⑫	⑬	DG

Fig. 7-2.

① to ⑧ DATA inputs:8-bit parallel input

⑨, ⑩ Channel Select:Selects/enables one of 4 outputs

⑪ LIGHT terminal.

After reading data, CPU (Y board) sends a trigger to pull pin ⑪ momentarily down to "L" level. This latches the output.

⑫ CHIP ENABLE terminal:selects/enables one of 24 D/A converters. It is enabled when this terminal is "L".

⑬ digital GND

⑭ analog GND

⑮ -5V input

⑯ to ⑰ OUTPUTs

⑱ Ref. voltage input

⑳ +5V input

3-7-4. Data Setup Timing

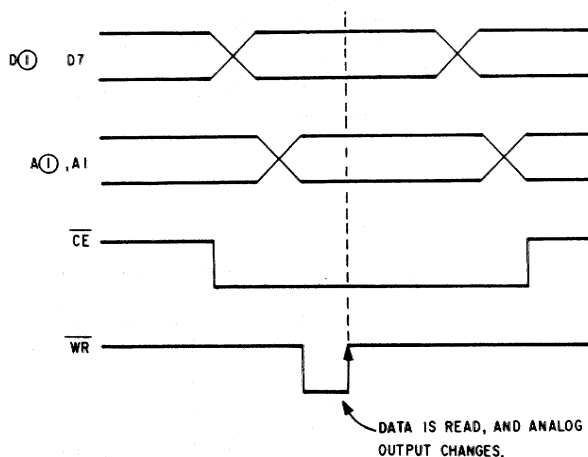


Fig. 7-3.

IC510 to IC517 and IC526 to IC529 perform attenuation of ZONE correction waveforms in H direction, and IC518 to IC526 and IC533 to IC536 perform attenuation of ZONE correction waveforms in V direction.

ZONE correction waveforms are applied to each of digital attenuators, and address signals A0 to A7 is used to select one channel of corresponding digital attenuator.

Input waveform for ZONE correction is attenuated in accordance with the values of DATA signal D0 to D7.

INPUT WAVEFORM	DATA (D0 ~ D7)	OUTPUT WAVEFORM
	00	
	80	
	FF	

Table 7-2.

Data is read, and analog output changes.

* Output changes by $E/128$ (V) at each "1-bit" change of DATA.

Inverted waveform of input is output when data is "00", and zero is output when data is "80". A waveform same with input signal is output when data is "FF".

Outputs from IC510 to IC529 and IC533 to IC536 are added in operational amplifiers IC538 to IC540, then are output as waveforms of V.SUB (R), V.SUB (G), V.SUB (B), H.SUB (R), H.SUB (G), and V.SUB (B).

3-7-5. Functions of Digital Attenuators (IC510 to IC536)

IC510	⑯ ZONE ⑩ H-B	IC518	⑯ ZONE ⑩ V-B	IC526	⑯ ZONE ⑱ H-B
	⑰ ZONE ⑩ H-R		⑰ ZONE ⑩ V-R		⑰ ZONE ⑱ H-R
	⑱ ZONE ⑩ H-G		⑱ ZONE ⑩ V-G		⑱ ZONE ⑱ H-G
	⑲ ———		⑲ ———		⑲ ———
IC511	⑯ ZONE ⑪ H-B	IC519	⑯ ZONE ⑪ V-B	IC527	⑯ ZONE ⑲ H-B
	⑰ ZONE ⑪ H-R		⑰ ZONE ⑪ V-R		⑰ ZONE ⑲ H-R
	⑱ ZONE ⑪ H-G		⑱ ZONE ⑪ V-G		⑱ ZONE ⑲ H-G
	⑲ ———		⑲ ———		⑲ ———
IC512	⑯ ZONE ⑫ H-B	IC520	⑯ ZONE ⑫ V-B	IC528	⑯ ZONE ⑳ H-B
	⑰ ZONE ⑫ H-R		⑰ ZONE ⑫ V-R		⑰ ZONE ⑳ H-R
	⑱ ZONE ⑫ H-G		⑱ ZONE ⑫ V-G		⑱ ZONE ⑳ H-G
	⑲ ———		⑲ ———		⑲ ———
IC513	⑯ ZONE ⑬ H-B	IC521	⑯ ZONE ⑬ V-B	IC529	⑯ ZONE ㉑ H-B
	⑰ ZONE ⑬ H-R		⑰ ZONE ⑬ V-R		⑰ ZONE ㉑ H-R
	⑱ ZONE ⑬ H-G		⑱ ZONE ⑬ V-G		⑱ ZONE ㉑ H-G
	⑲ ———		⑲ ———		⑲ ———
IC514	⑯ ZONE ⑭ H-B	IC522	⑯ ZONE ⑭ V-B	IC533	⑯ ZONE ⑱ V-B
	⑰ ZONE ⑭ H-R		⑰ ZONE ⑭ V-R		⑰ ZONE ⑱ V-R
	⑱ ZONE ⑭ H-G		⑱ ZONE ⑭ V-G		⑱ ZONE ⑱ V-G
	⑲ ———		⑲ ———		⑲ ———
IC515	⑯ ZONE ⑮ H-B	IC523	⑯ ZONE ⑮ V-B	IC534	⑯ ZONE ⑲ V-B
	⑰ ZONE ⑮ H-R		⑰ ZONE ⑮ V-R		⑰ ZONE ⑲ V-R
	⑱ ZONE ⑮ H-G		⑱ ZONE ⑮ V-G		⑱ ZONE ⑲ V-G
	⑲ ———		⑲ ———		⑲ ———
IC516	⑯ ZONE ⑯ H-B	IC524	⑯ ZONE ⑯ V-B	IC535	⑯ ZONE ㉒ V-B
	⑰ ZONE ⑯ H-R		⑰ ZONE ⑯ V-R		⑰ ZONE ㉒ V-R
	⑱ ZONE ⑯ H-G		⑱ ZONE ⑯ V-G		⑱ ZONE ㉒ V-G
	⑲ ———		⑲ ———		⑲ ———
IC517	⑯ ZONE ⑰ H-B	IC525	⑯ ZONE ⑰ V-B	IC536	⑯ ZONE ㉓ V-B
	⑰ ZONE ⑰ H-R		⑰ ZONE ⑰ V-R		⑰ ZONE ㉓ V-R
	⑱ ZONE ⑰ H-G		⑱ ZONE ⑰ V-G		⑱ ZONE ㉓ V-G
	⑲ ———		⑲ ———		⑲ ———

Table 7-2.

Block Diagram

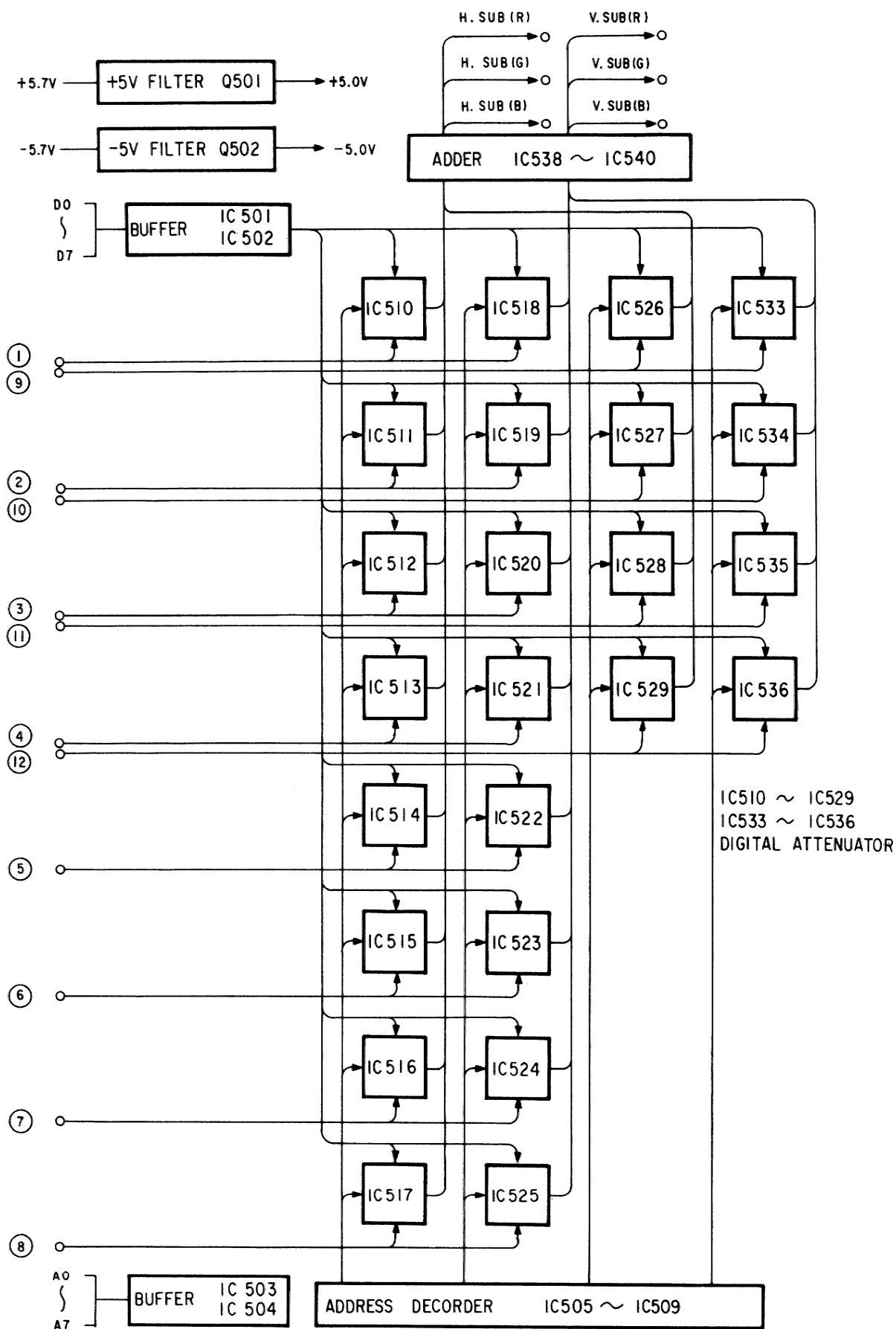


Fig. 7-4.

3-8. CIRCUIT OPERATION OF DC BOARD

DC board includes two circuit systems:

- (1) V. OUT circuit system
- (2) H (V) SUB OUT circuit system

These systems include same circuits for R, G, and B channels. Signals generated on DB board enter to DC board. Asynchronous beat noises may occur if impedance mismatching exists on signal lines connecting between DB and DC boards. Study on input/output impedance of these circuit boards was performed to cancel the impedance mismatching, and to decrease the level of asynchronous noises.

3-8-1. V. OUT Circuit System (vertical deflection output)

Vertical deflection output circuit consists of an operational amplifier (μ PC4558) and a vertical deflection output IC (μ PC1498), and has same circuit configuration in R, G, and B channels. So, circuit of G channel is described here. From DB board, V. OUT waveform (Fig. 8-1-A) enters to pin ③ of connector DC (on DC board). It enters to pin ③ of IC5. Because pin ② of IC-5 is in GND level, a waveform (Fig. 8-1-B) is feedback causing pin ③ of IC5 be kept in GND level. Based on error voltage between pins ② and ③, a waveform (Fig. 8-1-C) is output from pin ① of IC5. This enters to pin ④ of IC6, and current (Fig. 8-1-B) output from pin ② generates a voltage waveform of Fig. 8-1-D. μ PC1498 detects error portion in the input waveform (Fig. 8-1-C), and D5 and C10 superpose pulse E to waveform D to generate pulsed power supply.

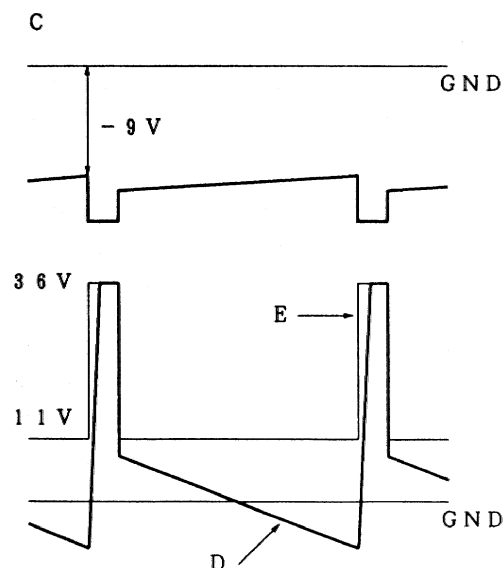
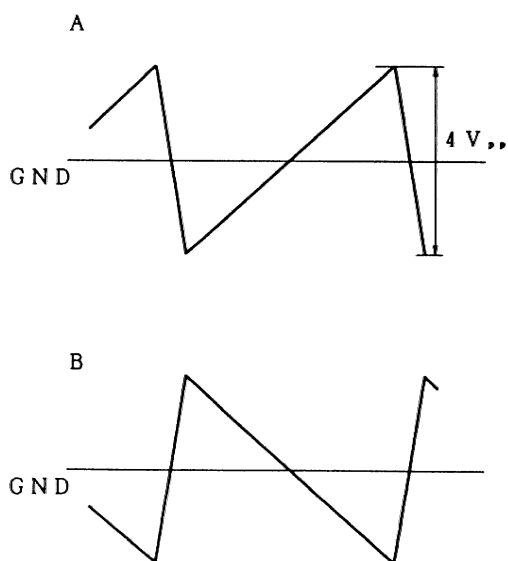


Fig. 8-1.

Q2 performs waveform shaping on deflection output pulse from pin ② of IC6 to monitor deflection output. Without C14, waveform on collector of Q2 will be a pulsed waveform as depicted in Fig. 8-2-A. Actually, integration by C14 is done to generate a sawtooth waveform as shown in Fig. 8-2-B. If something wrong occurred in vertical deflection output, pulses of Fig. 8-1-D do not appear and collector of Q2 is held to +B. This charges the capacitor as shown in Fig. 8-2-B (dotted line), and when the voltage across the capacitor exceeds the reference voltage on pin ⑥ of IC5, then pin ⑦ of IC5 goes up to "H". This turns Q4 ON and turns Q5 OFF. Pin ⑤ of connector DC-3 monitors the stop of vertical deflection. Also, IC9 performs waveform-shaping to deflection output pulse from pin ② of IC6 to output V. PULSE for vertical blanking via D10 and Q6. D9 adds vertical STOP signal to V. PULSE to perform blanking even when vertical deflection stops.

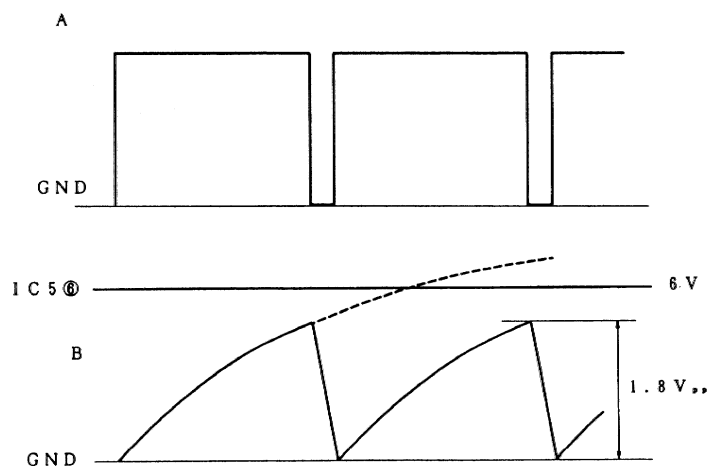


Fig. 8-2

3-8-2. H (V) SUB OUT Circuit System

Both H and V SUB OUT circuits have same configuration in R,G and B channels (6 channels in total). Description on H. SUB OUT (R) is given here.

SUB OUT circuit consists of a pre-amplifier IC302, a drive circuit (Q303 and Q306), and a buffer (Q307 and Q308). IC302 is an operational amplifier. Its pin ② is input terminal for correction waveform, and pin ③ is input terminal for current waveform feedback from SUB. DY. Current in SUB. DY is converted into voltage using resistors for current detection (R331 to R336), then enters to pin ③. Let the input voltage to pin ② be v (V). Then, the SUB.

DY current i is calculated as:

$$i = v / 0.78 \text{ (A)}$$

If current amplitude of correction waveform H. SAW is 3 Ap-p, voltage across DY shall be as shown by following equation because retrace time is $2 \mu\text{S}$ and inductance of DY is $20 \mu\text{H}$:

$$V = \frac{di}{dt} = -20 (\mu\text{H}) \frac{3(\text{Ap-p})}{2(\mu\text{S})} = -30\text{V}$$

An operational amplifier is used as pre-amplifier, and Q305 and Q306 are used as drive circuit. Q305 is used as an active load to improve frequency response of drive circuit.

SUB correction shall be proportional to correction waveform input to pin ① of connector DC-3. Beam movement, however, is proportional to integrated waveform because of effect from eddy current in CRT. Reversal correction to the eddy-current effect is done using a differentiating circuit (C301, C343, R301, R302), and amplitude adjustment is done in IC101.

3-8-3. Pulse Power Supply Circuit

Power supply voltage up to 30V is required during retrace time as shown in " (2) SUB OUT circuit". Such a high voltage, however, is not required during scanning time. To reduce power loss, a pulse power supply is used to supply voltage of 30V during retrace time only. This is done by switching ADHD signal from pin ① of connector DC-13 using Q105 and Q108 to generate pulses of $\pm 35\text{V}$, then the pulses are added to $\pm 15\text{V}$ using D102, D103, D105 and D106.

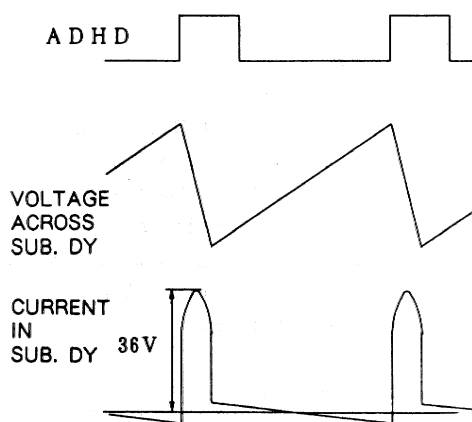


Fig. 8-3.

3-8-4. Current Limiter Circuit

CURRENT LIMITERS are used for circuit protection on DC board which are activated at 4A of load current on $\pm 15\text{V}$ lines. A current limiter on +15V line consists of Q9, R64, and R76. Current flows through a resistor connected to base and emitter, and if the voltage across this resistor exceeds V_{BE} of transistor, then Q9 is turned ON to enable V STOP PROT circuit. Limiter on -15V line consists of Q10, R65, and R75.

3-9. CIRCUIT OPERATION OF E BOARD

3-9-1. F-V Conversion

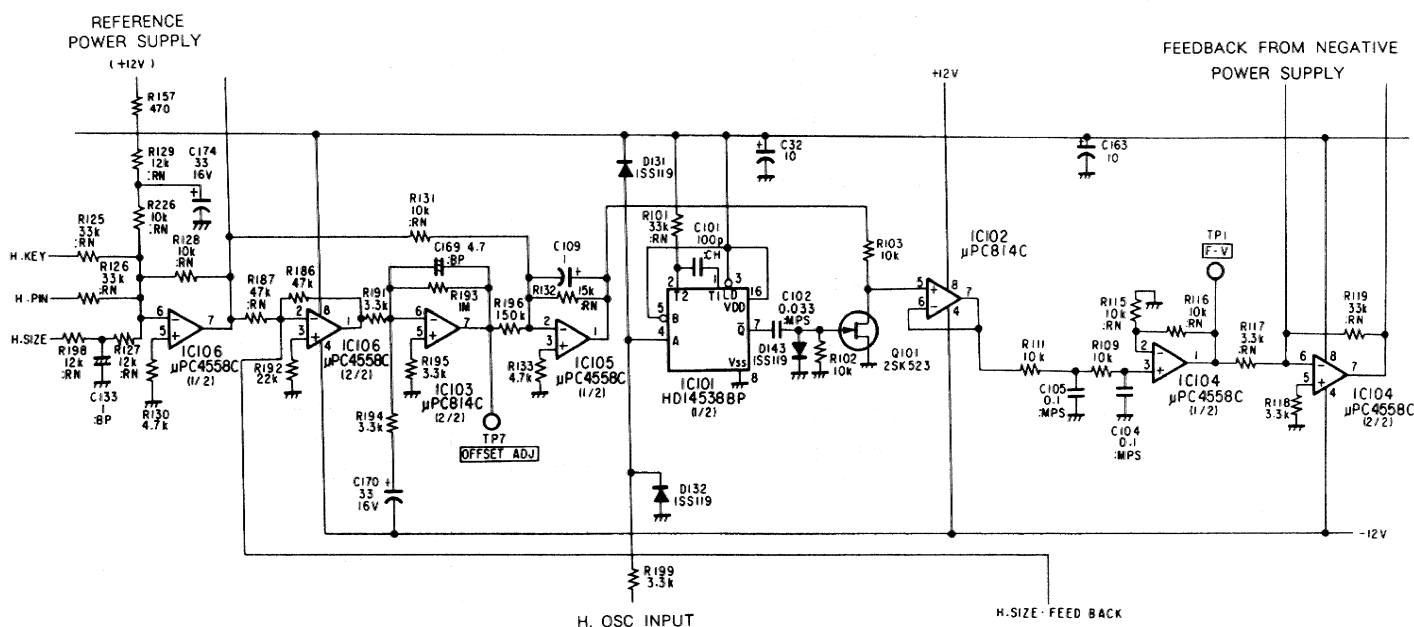


Fig. 9-1

H.KEY (V sawtooth wave, about $\pm 2.5V_{p-p}$), H. PIN (V. PARABOLA wave, about $\pm 2V_{p-p}$), and H. SIZE (DC, about $\pm 2.2V$) enter to pin ⑥ of IC106 via connector E-1, and they are added together. Also, reference voltage is connected to pin ⑥ of IC106 via R129 and R226. Output from IC106 is distributed to 3 portions of system as shown below:

- (1) To pin ② of IC105 via R131

This is the main controller to OPEN LOOP.

- (2) To pin ② of IC106 via R187

This is compared to H. SIZE feedback. Error voltage is applied to pin ⑥ of IC103, and is amplified/integrated by R191, R193, and C169, then is output to pin ② of IC105 via R196. This is the controller to error correction in CLOSED LOOP.

- (3) To pin ④ of IC107 via C110

This is used as PIN MOD. modulation waveform.

Following paragraphs describe the reason why control (1) and (2) said above are necessary.

Horizontal deflection current varies in accordance with f_H because:

- (a) Ratio of H retrace/trace time changes depending on f_H , i.e., the higher f_H , the higher PIN MOD voltage is required.
- (b) In low f_H , current dissipation increases and voltage drop across R173 and R174 increases beyond ignorable level.

Following curve is derived from (a) and (b):

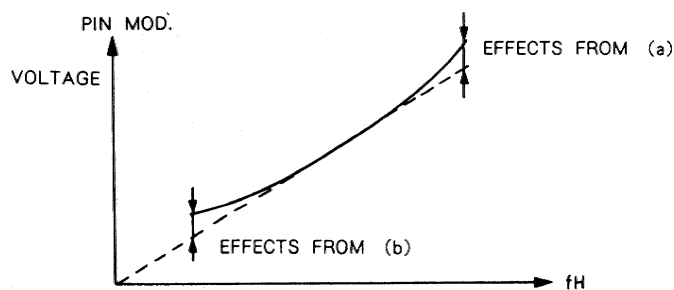


Fig. 9-2

The portion of solid-line shows the curve with constant deflection current. If formed a feedback loop based directly on the concept above to realize this, too large time constant of the feedback loop consisting of negative power supply \rightarrow PIN MOD. \rightarrow SIZE detection prevents quick response to sudden change in f_H (e.g., signal switching). In practice, feedback operation is limited to correction of errors between dotted lines and solid line in Fig. 9-2, and OPEN LOOP control to portions of dotted line is done using F-V convertor.

Now return to Fig. 9-1. Control both to (1) and (2) are applied to pin ⑤ of IC105, then integrated using R132 and C109. DC voltage obtained by integration passes R103, then is switched by Q101. Drive pulse to Q101 comes from DC board. H. OSC pulse enters to pin ④ of IC101 via R199, and after waveform-shaping, it is sent to pin ⑦ of IC101. Waveform on pin ⑦ of IC101 is as shown in Fig. 9-3.

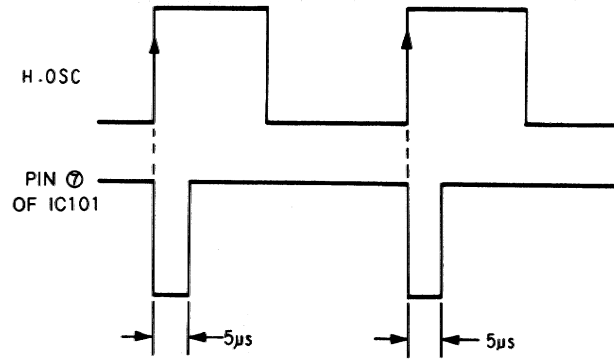


Fig. 9-3.

The pulse enters to the gate of Q101 via C102. Pulse, which is proportional to H. SIZE voltage and also to f_H , is output from drain of Q101. The pulse passes a buffer (1/2 of IC102), then is integrated by R111, C105, R109, C104, and is output to pin ⑦ of IC104 as F-V conversion voltage. Voltage at TP1 is approximately as shown below:

- at $f_H = 15 \text{ kHz}$: 0.4V to 0.8V
(with H. SIZE change from min. to max.)
- at $f_H = 34 \text{ kHz}$: 0.9V to 1.8V
(with H. SIZE change from min. to max.)
- at $f_H = 75 \text{ kHz}$: 2.3V to 4.3V
(with H. SIZE change from min. to max.)

3-9-2. Negative Voltage Supply

Fig. 9-4 shows the negative power supply.

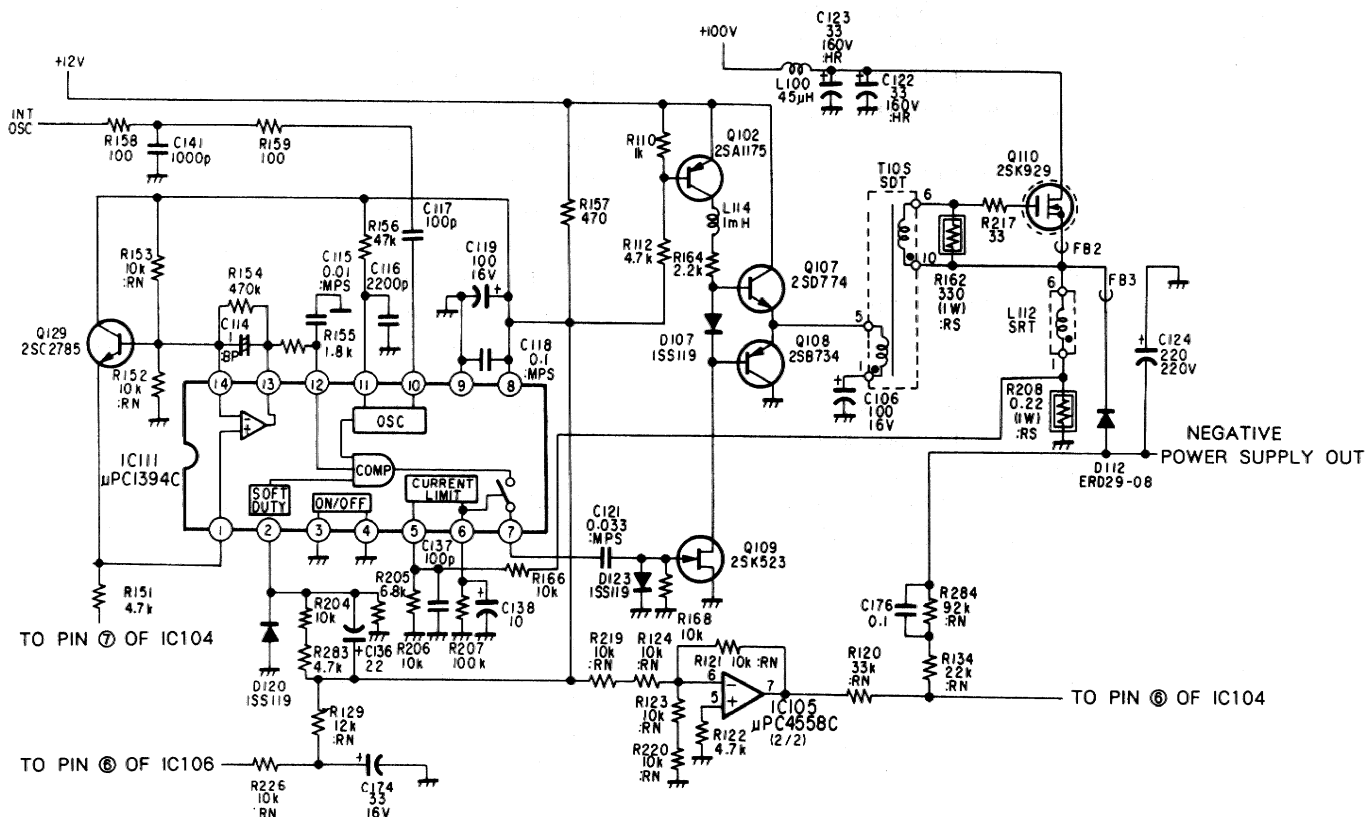


Fig. 9-4

Operation is as follows :

Output of F-V convertor enters to pin ⑥ of IC104 via R117 (see Fig. 9-1), and negative power supply is applied to pin ⑥ of IC104 through R284, C176, R134. IC104 compares these inputs, and output voltage from its pin ⑦ enters to pin ① of IC111.

Pin ① of IC111 shall be kept in positive voltage. To achieve this, bias voltage, generated by 2/2 of IC105, is applied to pin ⑥ of IC104. IC111 is a switching regulator IC. Its operation is as follows :

The IC compares voltage on pin ⑭ and on pin ① to output the error between them from pin ⑬. The output passes a filter (R155 and C115), then enters to pin ⑫. On the other hand, using INTERNAL OSC (which enters to pin ⑩) as trigger, a sawtooth waveform synchronous to INT OSC is output from pin ⑪. Result of comparison between voltage on pin ⑫ and sawtooth waveform on pin ⑪ is output from pin ⑦.

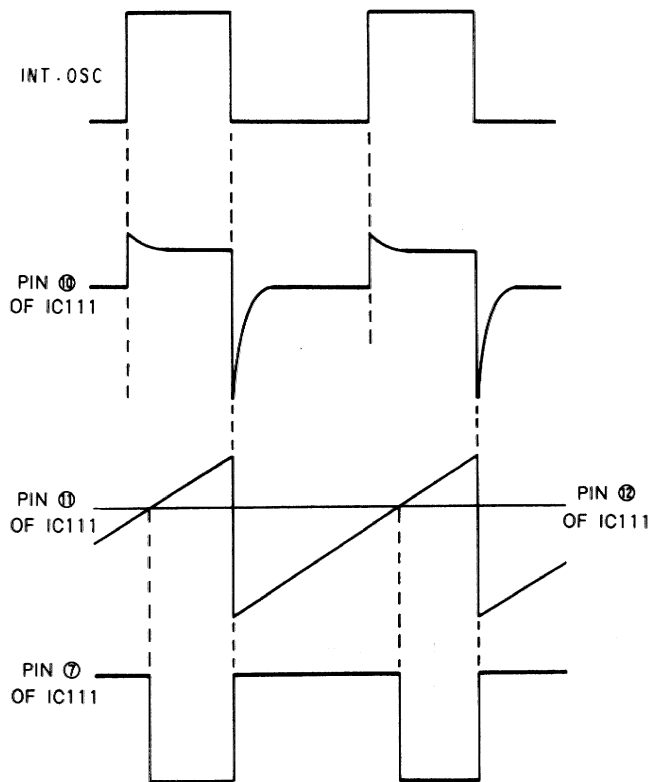


Fig. 9-5

Control to voltage of the negative power supply is done by changing duty on pin ⑦. The pulse, output from pin ⑦, is switched by Q109, passes a buffer (Q107 and Q108), then enters to pin ⑤ of T105. The pulse switches Q110 via T105. Q102 stops the switching if voltage on +12V line drops to prevent large fluctuation in output of negative power supply caused by light load at POWER OFF. Q129 prevents pin ① of IC111 from being pulled down to negative domain during POWER ON sequence. R208 is used as current detecting resistor to disable the switching of IC111 OFF at current level about 3-times larger than in normal load.

Basic operation of the inverting-polarity switching regulator is as follows:

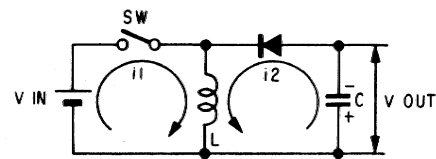


Fig. 9-6

(1) If turned SW ON for an interval (T_{ON}), current i_1 flows through L. Change in current in this case is calculated as $\frac{V_{IN} \cdot T_{ON}}{L}$

(2) If turned SW OFF for an interval (T_{OFF}), then diode turns ON and current i_2 flows through it. Energy stored in L transfers to C. Change in current in this case is calculated as $\frac{V_{OUT} \cdot T_{OFF}}{L}$

(3) In steady state of operation, changes in current of cases (1) and (2) become equal.

$$\frac{V_{IN} \cdot T_{ON}}{L} = \frac{V_{OUT} \cdot T_{OFF}}{L} \therefore V_{OUT} = \frac{T_{ON}}{T_{OFF}} \cdot V_{IN}$$

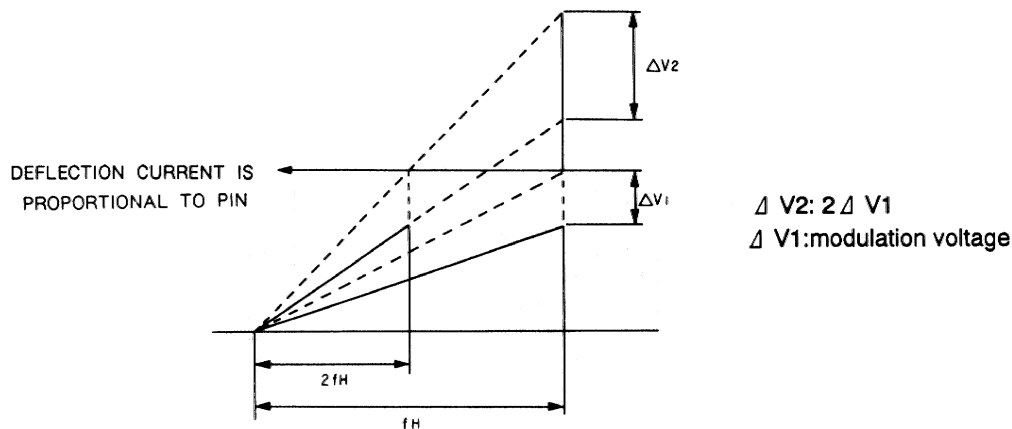


Fig. 9-9

If modulation is ΔV_1 at f_H , then PIN MOD. voltage required at $2f_H$ is ΔV_2 to maintain the modulation level same with the case of f_H (that is, ΔV_1), as depicted in the illustration above. To keep the raster size constant, modulation voltage should be changed proportional to f_H and H. SIZE.

Now return to the circuit operation. H. KEY and H. PIN modulation waveforms enter to pin ④ of IC107. Also, PIN MOD. voltage is divided by a resistive divider (R149, R150, R205), then is applied to pin ⑨. Output from pin ⑭ is proportional to PIN MOD voltage applied to pin ⑨. IC108 amplifies this voltage, and outputs it through a buffer (Q103 and Q104). C120 cuts DC component from the output, then D109 clamps the waveform to a voltage level from negative power supply. A filter (R176 and C128) is used to eliminate ripple on the negative power supply.

Q106 improves the response of circuit when f_H changes from a low frequency signal to a high frequency signal. Modulation waveform clamped to negative power supply enters to pin ③ of IC112 via R224. IC112 is a buffer. D110 and D119 perform level-shift by $2V_F$ to the clamped waveform. This is done to prevent PIN MOD waveform from being suppressed at its peak.

A $\pm 10V$ power supply from LOT, centering at PIN MOD voltage, is used as the power supply for IC112. D114 and D115 prevent IC112 from being latched up at POWER ON sequence. If input voltage exceeds the power supply voltage because of timing between input signal to IC112 and building-up of power supply voltage, latch-up of IC112 may occur.

Modulation waveform, output from pin ① of IC112, enters to gates of Q111 and Q112 via R171 and R172. Q111 and Q112 are FETs for PIN MOD OUT. D126 to D130 are used to protect Q111 and Q112. R173 and R174 are used to prevent returning of parabola voltage across S-shaping capacitor to PIN MOD section. Also, V. retrace time is determined by R173, R174 and S-shaping capacitor. So, the smaller resistance of these resistors, the better.

On the other hand, all current passing these resistors flows into C142. So, resistance of these resistors are determined by maximum ripple current of C142.

3-9-4. H. Drive Section

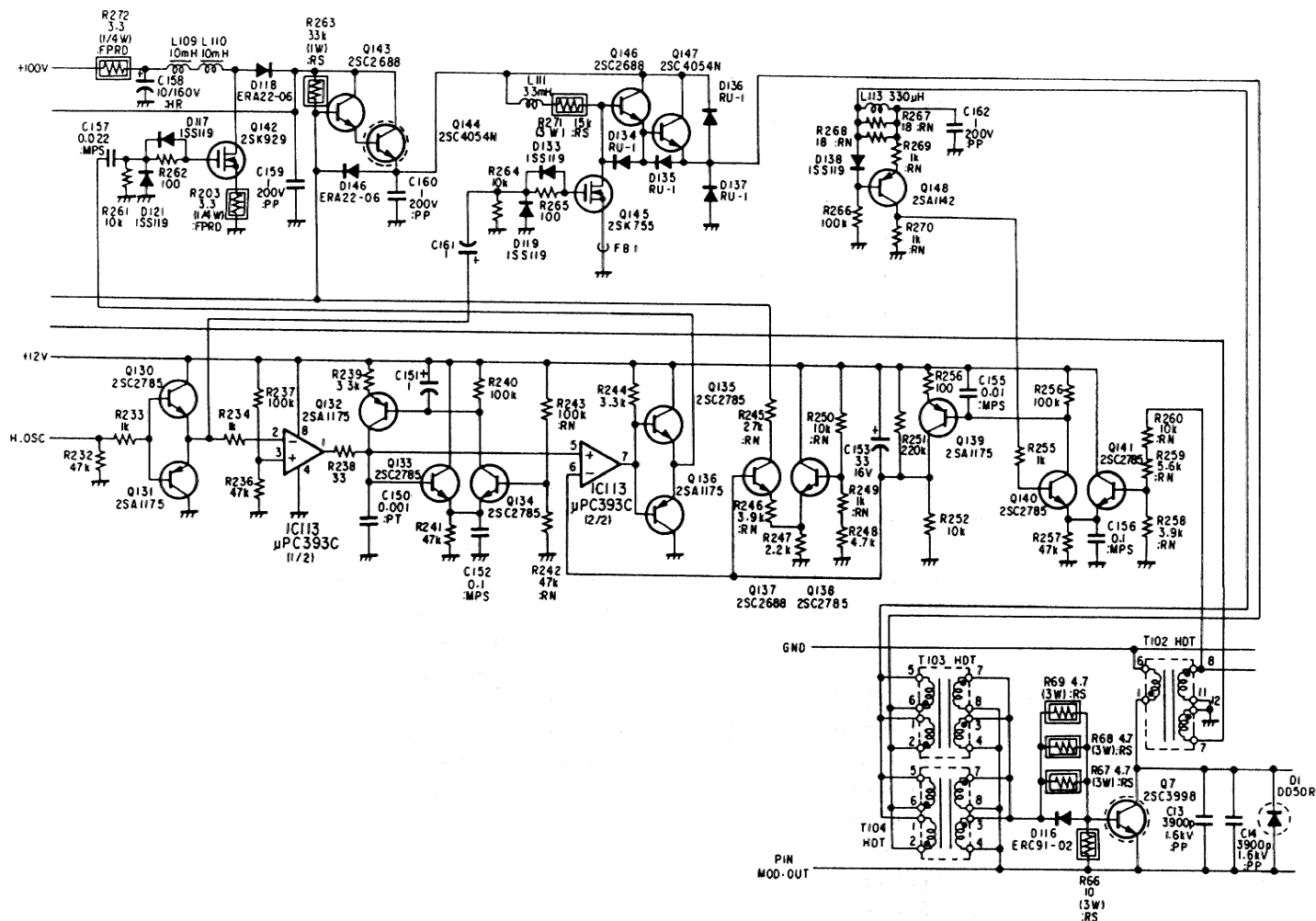


Fig. 9-10

Fig. 9-10 shows the circuit diagram of H. Drive section. Topics in this section are:

- (a) Variable power-supply for H. Drive
- (b) H. Drive circuit (ON-ON type)
- (c) Constant IB2 circuit

(a) Variable power-supply for H. drive

A power supply with variable range from 60 volts to one-hundred and several tens volts is required to keep Drive voltage in optimum level while covering change of H. SIZE control setting from minimum to maximum and fluctuation in hfe of H. OUT transistor. Voltage supplied to E board is 100V. A step-up type switching regulator is used to generate voltage higher than 100V.

If drive voltage is less than 100V, a series regulator (Q143, Q144) operates. Control to this series regulator is done by "constant IB2 circuit" to be described later. In this case, Q142 is turned OFF. If drive voltage more than 100V is required, a step-up type switching regulator starts its operation. H. OSC passes R233, then a buffer (Q130, Q131), and enters to pin ② of IC113.

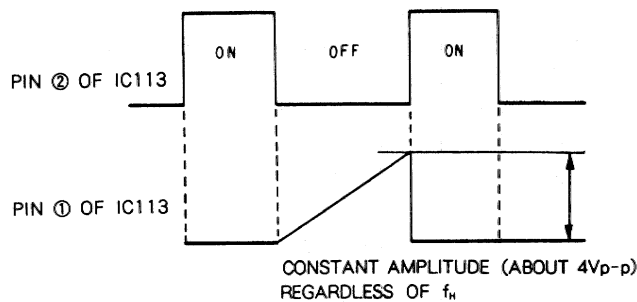


Fig. 9-11

Pin ① of IC113 is held Low, i.e. 0 volt, during ON time said above.

Pin ① of IC113 is OPEN during OFF time said above, and charging to C150 through Q132 occurs. At the next ON time, voltage across C150 quickly discharges through R238. To maintain the amplitude constant, comparison is performed by Q133 and Q134 to control a constant-current source Q132.

Q133 is an emitter-follower, and performs peak-rectification. Q133 also forms a comparator with Q134. The reason why operation of Q133 is deemed as peak-rectifier is, base-emitter junction of Q133 may be deemed as a diode if time constant of R241 and C152 is large enough against input signal.

That is, peak value of Q133's base voltage is compared to the reference voltage applied to Q134's base, and the difference between the two is feedback to Q132's base. Base voltage of Q132 may be deemed as DC because the time constant of R243 and C151 is large enough against input signal. Thus, the peak voltage of Q132's collector is maintained constant.

This output enters to pin ⑤ of IC113. On the other hand, DC voltage output from "constant IB2 circuit" to be described later enters to pin ⑥ of IC113.

Relationship between output waveform from pin ⑦ of IC113 and waveforms on pin ⑤ or pin ⑥ is as shown in Fig. 9-12.

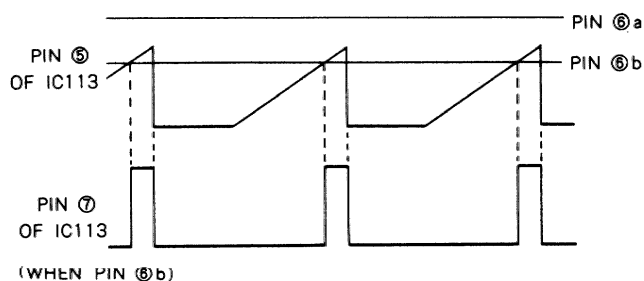


Fig. 9-12

If the voltage on pin ⑥ of IC113 is higher than that of pin ⑤, then pin ⑦ of IC113 is always held Low. When the voltage becomes lower than that of pin ⑤, then pin ⑦ is held High. This output passes a buffer (Q135 and Q136), then enters to the gate of Q142 via C157 and R262. Q142 is the switching regulator FET. At the time of Q142 to start its operation, Q143 and Q144 are fully turned ON. Basic operation of a step-up type switching regulator is as follows:

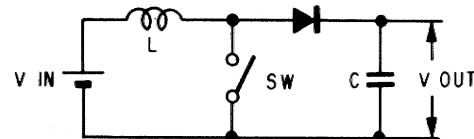


Fig. 9-13

- (1) When SW is turned OFF, then $V_{out} = V_{in}$.
- (2) If SW is turned ON, energy is stored to L for the time SW is turned ON.
- (3) When SW is turned OFF again, energy stored in L is superposed on the input voltage V_1 .

Following equation shows relationship between parameters said above.

$$V_{OUT} = \frac{T_{ON} + T_{OFF}}{T_{OFF}} V_{IN}$$

That is, voltage higher than 100V may be obtained by control to ON time of Q142. This is used as Drive voltage.

(b) ON-ON type H. drive circuit

H. Drive circuit of this projector model is the one of ON-ON type. If C162 is large enough, then IB1 is maintained constant regardless of changes in f_h . ON-ON means following operation of circuit. If current flows in the primary winding of HDT, current flows simultaneously in the secondary winding of HDT, and output transistor is turned ON.

H. OSC passes a buffer (Q130 and Q131), then enters to the gate of Q145. D119 is a clamper, and D133 speeds up the turning OFF of Q145. D134, D135, D136, and D137 are diodes for circuit protection. Timing chart of H. Drive voltage is as shown in Fig. 9-14.

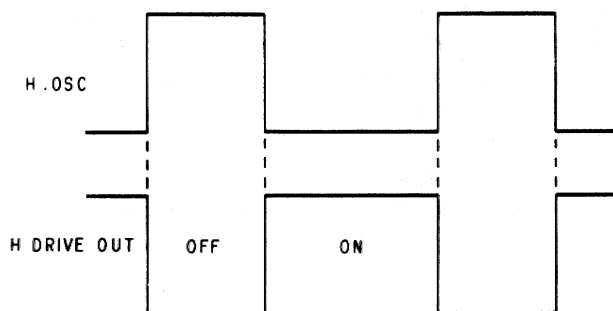


Fig. 9-14

Current flows from Q146 and Q147 during ON time, and Q145 sinks the current during OFF time.

(c) Constant IB2 circuit

Operation of IB2 detector circuit is as follows. In practice, current to be detected flows in secondary windings of T103 and T104. Current in primary windings of T103 and T104, however, is proportional to the current in secondary windings. So, the current in primary windings of T103 and T104 is detected as IB2. Detection is done by L113, R267 and R268. Let L113 be ignored to simplify the operation.

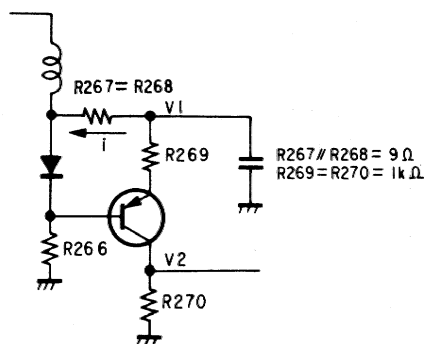


Fig. 9-15

Let voltage and current of circuit be as shown in the circuit diagram. Base voltage of Q148 is given as $(V1 - ai - 0.6)$, and emitter current of Q148 is given as $(v1 - ai)$. Thus, current in R269 is given as $\frac{9}{1000} i$, 1000 and the current flows to R270. Thus, V2 is calculated by following equation;

$$V2 = 1000 \times \frac{9}{1000} i = 9i$$

where: $R267/R268 = 9 \text{ ohms}$, $R269 = R270 = 1k \text{ ohms}$

That is, current proportional to IB2 appears on collector of Q148. D138 is used for temperature compensation to VBE of Q148. The reason why L113 is necessary is as follows. Optimum point of IB2 depends on f_H . Insertion of L113 gives the detector a sort of frequency response for correction of optimum point of IB2 depending on f_H .

This voltage enters to the base of Q140 via R255. Q140 and Q141 forms a differential amplifier. H. Pulse from the secondary winding of H.O.T is divided by a resistive divider R259, R260 and R258, then enters to the base of Q141. H. Pulse may be deemed that it contains all the fluctuation in H. SIZE and hfe. That is, maintaining IB2 constant by comparison between IB2 and H. Pulse makes the optimum Drive be possible.

For the method of comparison, base-emitter junctions of Q140 and Q141 may be deemed as forward-biased diodes if the time-constant of R257 and C156 is large enough against input signal. That is, the circuit compares the peak DC values of IB2 detect voltage and of H. Pulse. In case of H. Pulse is greater than IB2 detect voltage, circuit operation is as follows: decrease in V_{BE} of Q140 \rightarrow decrease in collector current of Q140 \rightarrow increase in base voltage of Q139 \rightarrow decrease in emitter current of Q139 \rightarrow decrease in collector voltage of Q139. The output is connected to pin ⑥ of IC113 and to the base of Q137. IC113 (2/2) is the variable power supply control IC for H. Drive. Q137 and Q138 form a differential amplifier, and its operation is as follows: decrease in base voltage of Q137 \rightarrow decrease in emitter current of Q137 \rightarrow increase in collector voltage of Q137.

Because collector of Q137 is connected to the bases of Q143 and Q144 (a series voltage regulator) via R245, output from the series voltage regulator increases for Over Drive, hence increase in IB2. In case of H. Pulse < IB2 detect voltage, operation of the circuit is reversed, and results in Under Drive, hence decrease in IB2.

3-9-5. H. SIZE Feed Back, H. SIZE MAX/MIN Protector L.O.T +B line Current Protector

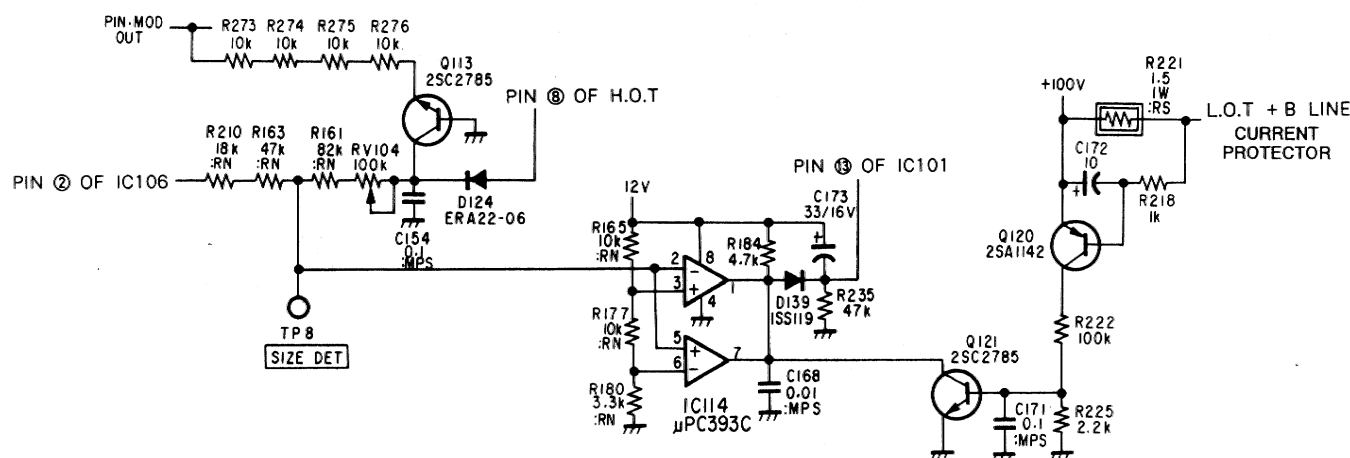


Fig. 9-16

Fig. 9-16 shows circuits of H. Size Feed Back, H. SIZE MAX/MIN Protector, and L.O.T +B line Current Protector.

In H. Size Feed Back circuit, D124 and C154 performs peak-rectification of H. Pulse from the secondary winding of H.O.T. This DC voltage is returned to pin ② of IC106 as the detection voltage. Operation of Q113 is as follows : Even if amplitude of H. Pulse is constant, mean voltage of peak-rectification differs depending upon f_H .

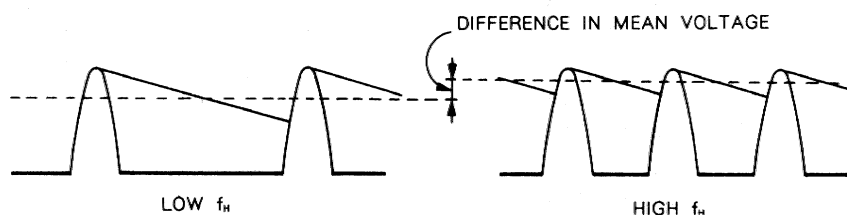


Fig. 9-17

Long time-constant eliminates difference in mean voltage, however, this deteriorates effectiveness of Feed Back loop. Therefore, control to discharge time in accordance with f_H is used to maintain the mean voltage constant.

That is, discharge time is extended when f_H is low, and is cut short when f_H is high. Emitter of Q113 is connected to PIN MOD. OUT via resistors R273 to R276. Voltage on PIN MOD. OUT is high when f_H is low, and it is low when f_H is high. That is, collector current of Q113 (= discharge current) is calculated by following equation:

$$I_c = \frac{-0.6 - (\text{PIN MOD. OUT})}{R_{237} - R_{276}}$$

NOTE: PIN MOD. OUT voltage is in negative domain.

As seen from the equation above, the collector current decreases when PIN MOD. OUT is high (smaller absolute value), and the collector current increases when PIN MOD. OUT is low (larger absolute value). Thus, if amplitude of H. Pulse is constant, the mean voltage is maintained constant regardless of fH. The detect voltage is returned to pin ② of IC106 to compare it to input signal. Error component passes IC103 (2/2) and R196, then added to the input signal using IC105 (1/2).

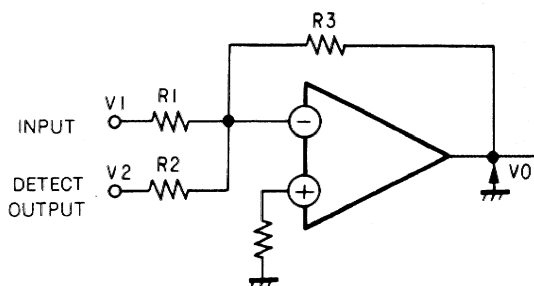


Fig. 9-18

Equation below shows the relationship between parameters in diagram:

$$I_c = -\left(\frac{R_3}{R_1} V_1 + \frac{R_3}{R_2} V_2\right)$$

To simplify the equation, $\frac{R_3}{R_1}$ and $\frac{R_3}{R_2}$ may be ignored because they are constants. When $|V_1| = |V_2|$, then output V_0 is zero with V_1 and V_2 in reversal polarity. When $|V_1| \neq |V_2|$, then voltage corresponding to $|V_1| - |V_2|$ appears on output V_0 as error voltage. If f_H is low, the error voltage corresponds to power loss in R173 and R174. If f_H is high, the error voltage corresponds to H retrace/trace time.

Operation of H. SIZE MAX/MIN Protector is as follows: IC114 is used to detect H SIZE. Voltage of 6.85V is applied to pin ③ of IC114. Also, voltage of 1.7V is applied to pin ⑥ of IC114. H. SIZE detect voltage is applied to pin ② and pin ⑤ of IC114. When the detect voltage increases over 6.85V (SIZE MAX), or decreases under 1.7V (SIZE MIN), pin ① and pin ⑦ of IC114 fall to LOW state. The output is connected to pin ⑬ of IC101 (in H. STOP circuit to be described later). When pin ① and pin ⑦ of IC101 fall to LOW state, H. STOP circuit is activated to turn the power supply OFF.

Operation of L.O.T +B line Current Protector is as follows:

R221 is the detection resistor. Operating point is set to where Q120 is turned ON, that is,
 $0.6 = 1.5 \times i \therefore i = 400 \text{ mA}$

When Q120 is turned ON, Q121 is also turned ON. Collector of Q120 is connected to the line same with that of pin ① and pin ⑦ of IC114. So, with the operation similar to that of above, the power supply is turned OFF.

3-9-6. HD OUTPUT, H. STOP Circuit

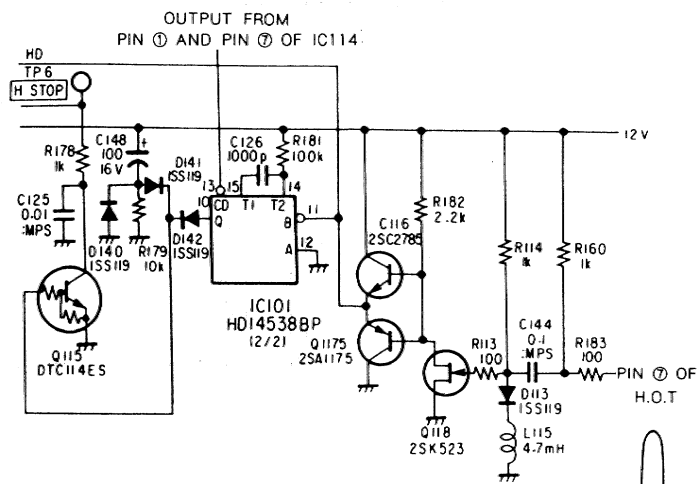


Fig. 9-19

Fig. 9-19 shows HD OUTPUT and H. STOP circuits. Generation of HD output is as follows :

C144 cuts DC component of H. Pulse in negative polarity from pin ⑦ of H.O.T. H. Pulse is biased by R114, D113, and L115. Then, the pulse switches Q118, and is output after passing a buffer (Q116 and Q117). A technique is used to expand the pulse width of HD as far as possible. Because some ringing exists in H. Pulse, spikes may appear at ringing portion if sliced H. Pulse at its base. Decreasing the slice level to eliminate adverse effects from ringing results in narrow pulse width of HD.

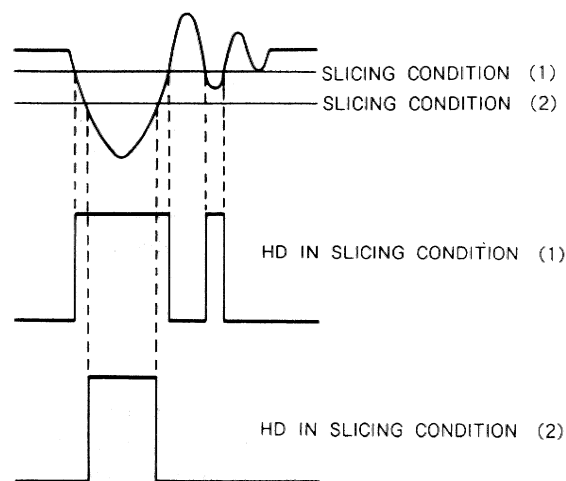


Fig. 9-20

With slicing condition ①, wide HD pulse but with spike.

With slicing condition ②, no spike but narrow HD pulse.

L115 is inserted to generate wide pulse without spike.

Without L, waveform V is clamped to voltage of VF of diode.

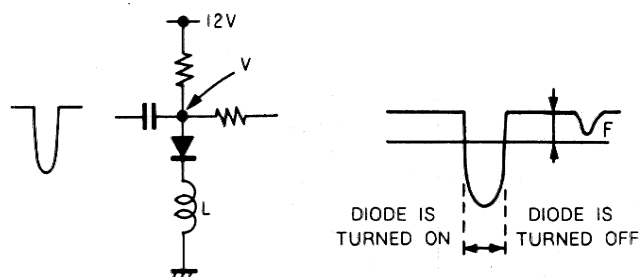


Fig. 9-21

With L inserted at the cathode of diode, the charge stored in C during OFF time of diode does not discharge quickly in ON time of diode because L impedes the quick discharge. Thus, trailing edge of V pulse is slightly lifted and results in a waveform shown in Fig. 9-22

That is, wide pulse without spike is obtained by lifting ringing portion of the waveform, and slicing H. Pulse at its base.

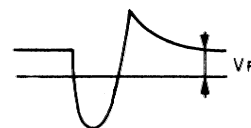


Fig. 9-22

Operation of H. STOP circuit is as follows:

IC101 is a monostable multivibrator. HD enters to B input of the IC. If the time constant of external C,R (100kohms \times 1000pF = 100 μ S, in this case) is long enough than H period, output Q is High as long as HD is applied to B input of the IC. The output enters to the base of Q115 via D142. Thus, Q115 is turned ON in normal state of operation, and H. STOP terminal is LOW. Without HD, Q output falls to LOW and Q115 is turned OFF. This causes H. STOP terminal be High state, and the power supply be turned OFF. Also, output from IC114 is connected to CLEAR terminal of the IC. If SIZE MAX/MIN, L.O.T +B line Current Protector is activated, CLEAR terminal becomes LOW. Q output also falls LOW, and the power supply is turned OFF. C148 is used to keep the base of Q115 High during POWER ON sequence.

3-9-7. L.O.T Section

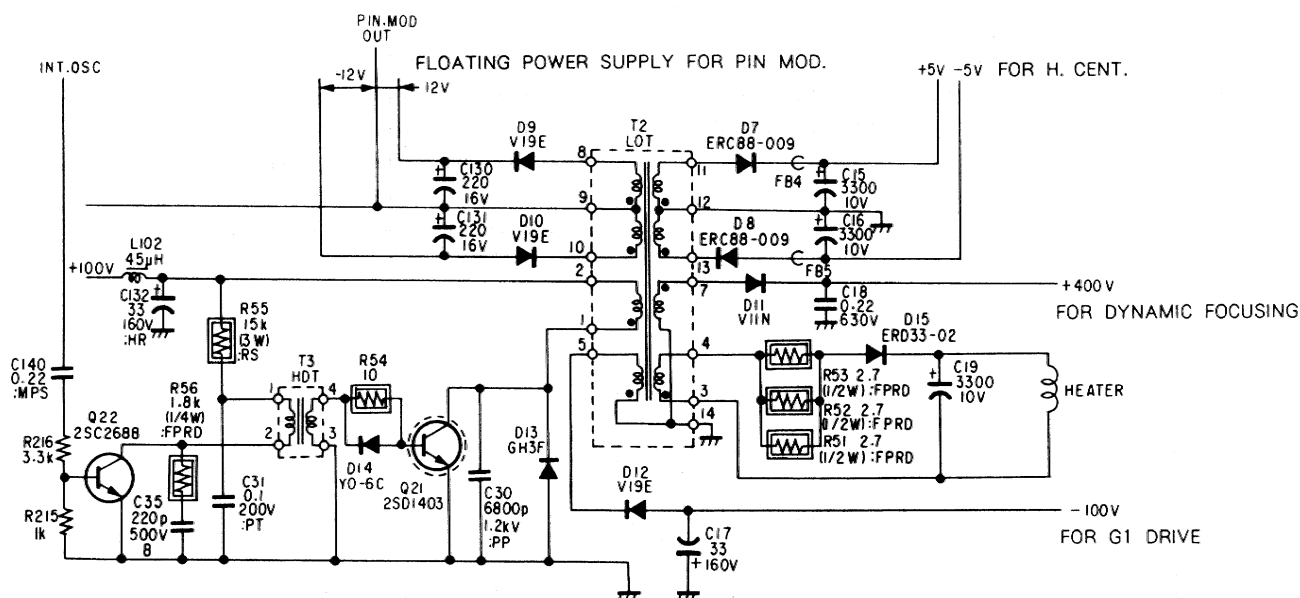


Fig. 9-23

Fig. 9-23 shows L.O.T section.

L.O.T section performs asynchronous operation, as in High Tension section. INT. OSC, generated on PA board,

is used as Drive pulse. Q22 is pre-drive transistor, and perform switching to Q21 via T3. Various voltages are provided by resonant pulse determined by inductance L of the primary winding of L.O.T and a capacitor C30.

3-9-8 H. Cent circuit

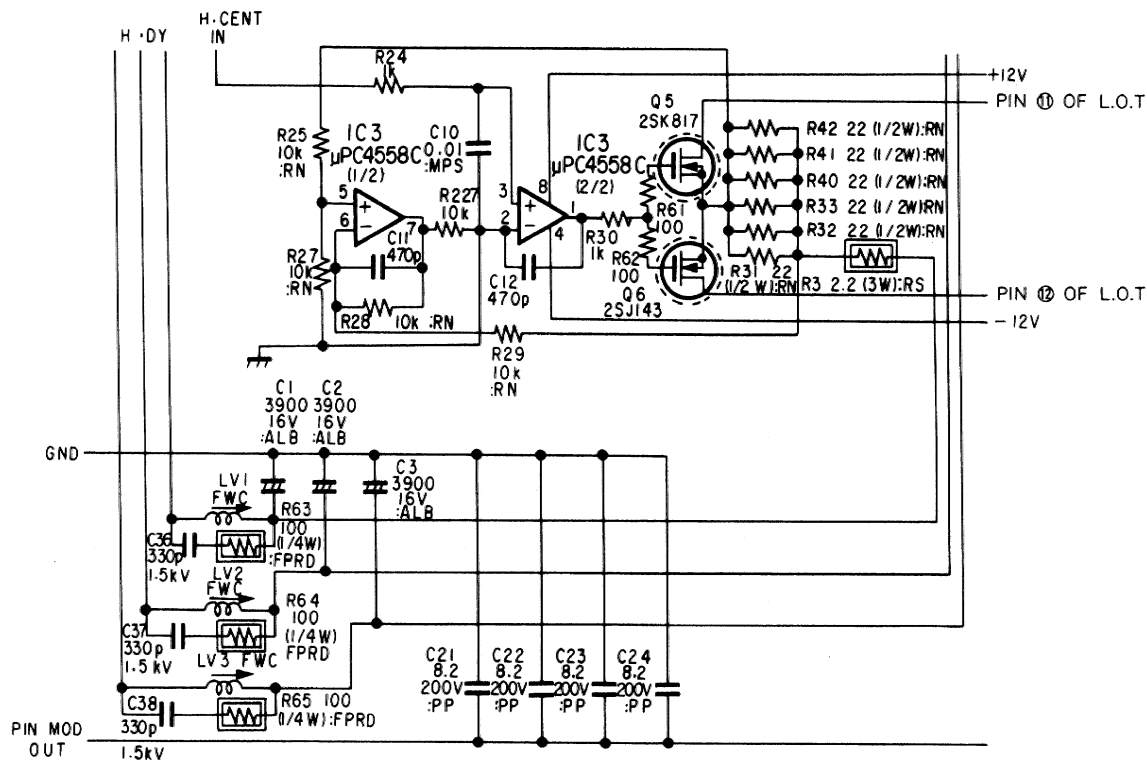


Fig. 9-24

Fig. 9-24 shows H. Cent circuit.

Configuration of H. Cent circuits is common in R, G and B channels. So, circuit operation of only one channel is given here.

R31, R32, R33, R40, R41, and R42 are used in detecting H. Cent current. Voltage across these resistors is feedback to IC3 (1/2) to convert H. Cent current into voltage. IC3 (2/2) compares the voltage to H. Cent control voltage to maintain Cent current always constant. C11 and C12 are used to prevent oscillation in the circuit. Q5 and Q6 are DRIVE FETs.

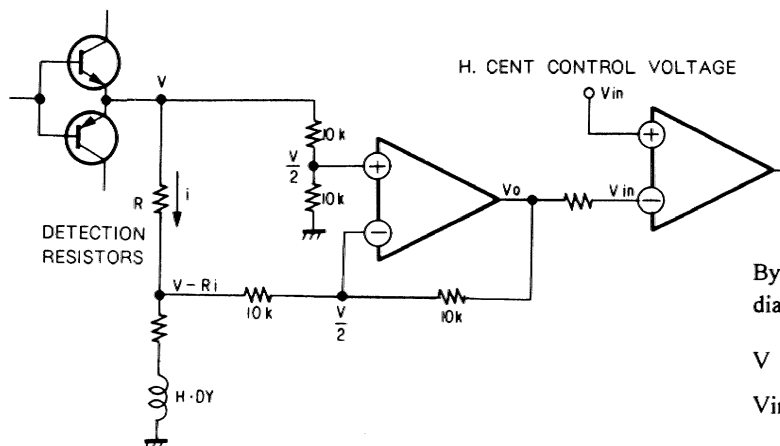


Fig. 9-25

By setting voltage and current as shown in the circuit diagram, then;

$$V - Ri = \frac{V}{2} = V_0 = V_{in}$$

$$V_{in} = Ri$$

$$\therefore i = \frac{V_{in}}{R} \dots\dots\dots \text{constant.}$$

3-9-9 H. OUT circuit

Principle of operation of H. OUT circuit is omitted because it is described in detail in various documents. In this model, Q7 is H. OUT transistor, C13 and C14 are resonant capacitors, and D1 is damper diode. The circuit features that PIN. MOD. voltage in negative domain permits H. Cent current flows into H. MAIN DY using no floating power supply. D144, C175, R287 to R290 form a pulse stopper circuit which provides protection to H. OUT transistor be damaged from jumping of collector pulse in case of discharge in high-tension circuits.

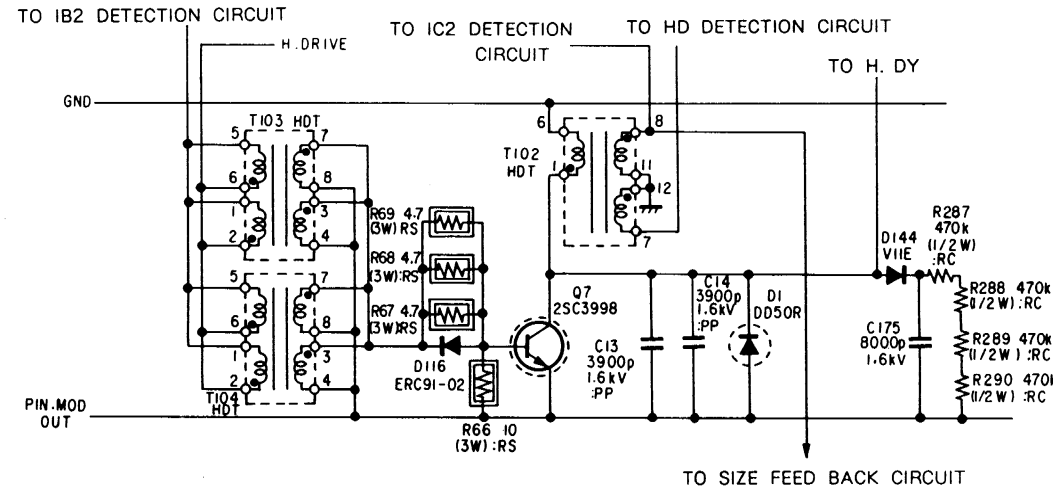


Fig. 9-26

3-9-10. Block Diagram (E Board)

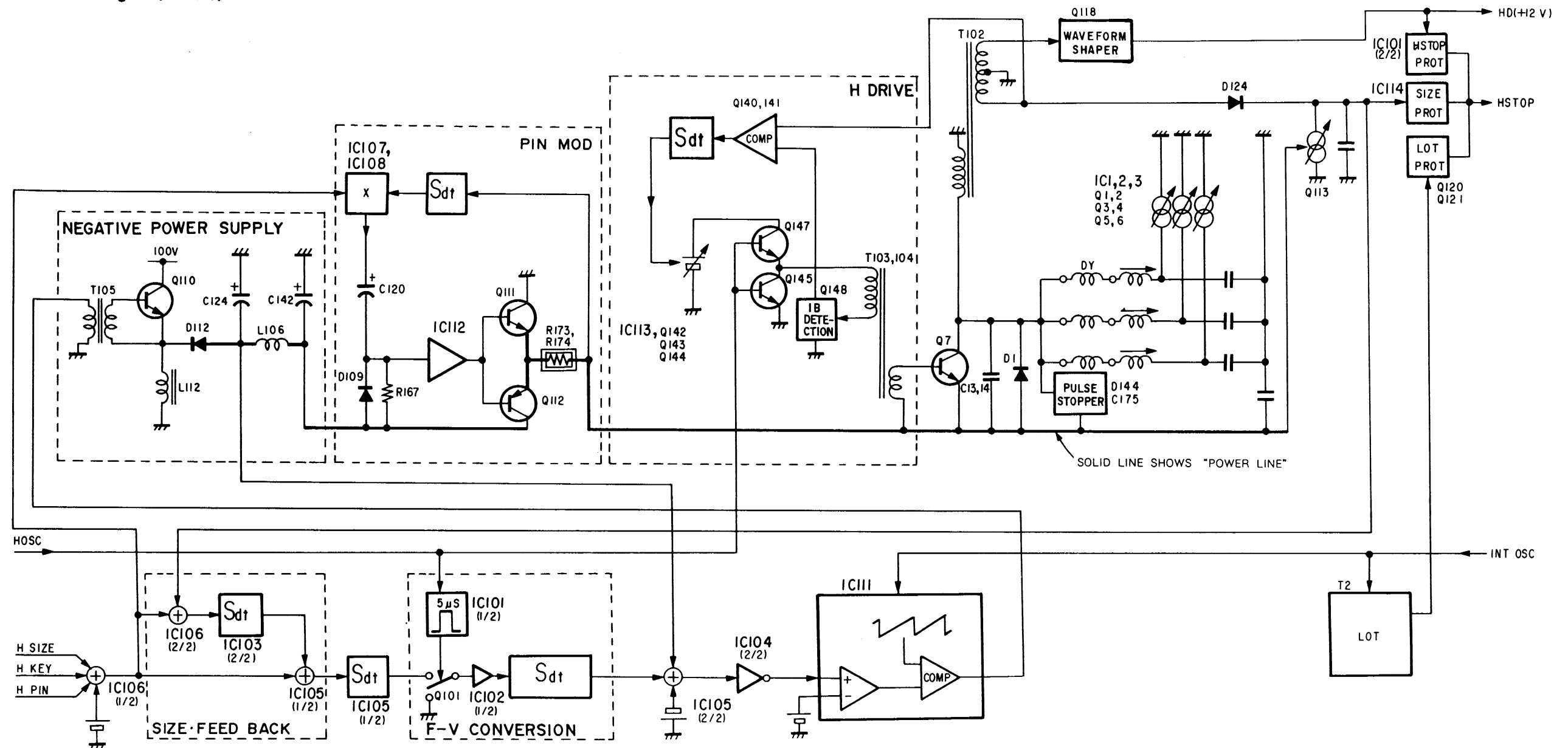


Fig. 9-27

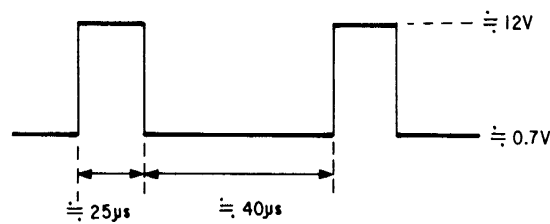
3-10. CIRCUIT OPERATION OF PA BOARD

3-10-1. Internal OSC.

This projector set is designed to operate in wide-range, multi-scanning modes. In such case, configuration of conventional high-tension circuit synchronous to fH is difficult. So, an asynchronous type high-tension circuit configuration driven by an independent oscillator is adopted.

A resonator X1 is the fundamental clock of oscillator which oscillates at 495 kHz. The clock frequency is divided by IC7 and IC8 to generate pulses about 15.47 kHz as "internal oscillator" (INT. OSC.). Pin ⑧ of IC8 is output terminal of INT. OSC. INT. OSC. is used as switching pulse in two circuits. One is sent to high-tension circuit via a buffer (Q3), and the other passes a buffer (Q4) and a connector (PA-3), then sent to E board as switching pulse for a negative power-supply.

R96, R97 and C47 connected to pin ⑪ (RESET terminal) of IC7 form a reset circuit at power-on. It differentiates voltage building-up waveform at power-on sequence so that INT. OSC. is output after complete building-up of the power supply voltage.



(EMITTER OUTPUT FROM Q4)

Fig. 10-1. INT. OSC. pulse

3-10-2. HV Generator

INT. OSC. pulse passes a buffer (Q3), pin ③ and pin ④ of connector PA-7, then drives transistor Q6 (2SC2688). Q6 drives a drive transformer T2, and output of T2 drives Q10 (2SD1887, converter transistor of FBT). Basic portion of this high-tension circuit is same with that of conventional high-tension circuits. Q10 is converter transistor; D20 and D21 are damper diodes; C51 is resonant capacitor; L3 and L4 are dummy inductors; and C54 is S-shaping capacitor.

Inductance of dummy inductors (L3 and L4) is selected about 2.1 mH, and this is roughly equal to the inductance of primary winding of FBT. In this projector set, two FBTs are connected in parallel to achieve high power output. So, the inductance as seen from collector of transistor Q10 is about 0.525 mH (four inductors of 2.1 mH are connected in parallel). A high-tension circuit utilizes LC resonance of this inductance and resonant capacitor (C51) to generate high voltage. It generates pulses (about 1kV) in the primary winding of FBT, and these pulses are stepped up by several tens times in the secondary winding of FBT. Pulse height in the primary winding V_p is determined by equivalent inductance (0.525 mH) of dummy inductors, resonant capacitor, power supply voltage connected to dummy inductors (V+B), and frequency of drive pulse (f_H):

$$V_p = \frac{V + B (1/f_H - T_w)}{2\sqrt{LC}}$$

$$\text{where: } T_w = \frac{1}{\pi\sqrt{LC}}$$

T_w : resonant pulse width

Strictly speaking, equations above is not effected in practice because of various factors. Values at cut-off of CRT's beam current are;

$$V+B \approx 110V, V_p \approx 800V, T_w \approx 12\mu S$$

Ratio of FBT's primary and secondary windings is about 40. Pulse with height about 40 times (33 kVp-p) of primary pulse is output from the secondary winding.

This is rectified by diodes built in FBT, a HVF (HV filter), and a capacitor built in HVB (HV block), and is output as DC voltage of 33kV.

Because high voltage in this projector set is generated by asynchronous circuits, picture may be adversely affected by ripple component in high voltage. To avoid this, high voltage generated in FBT passes a filter (HVF) first, then is applied to high voltage detection circuit and to a HVB for high voltage distribution to CRTs.

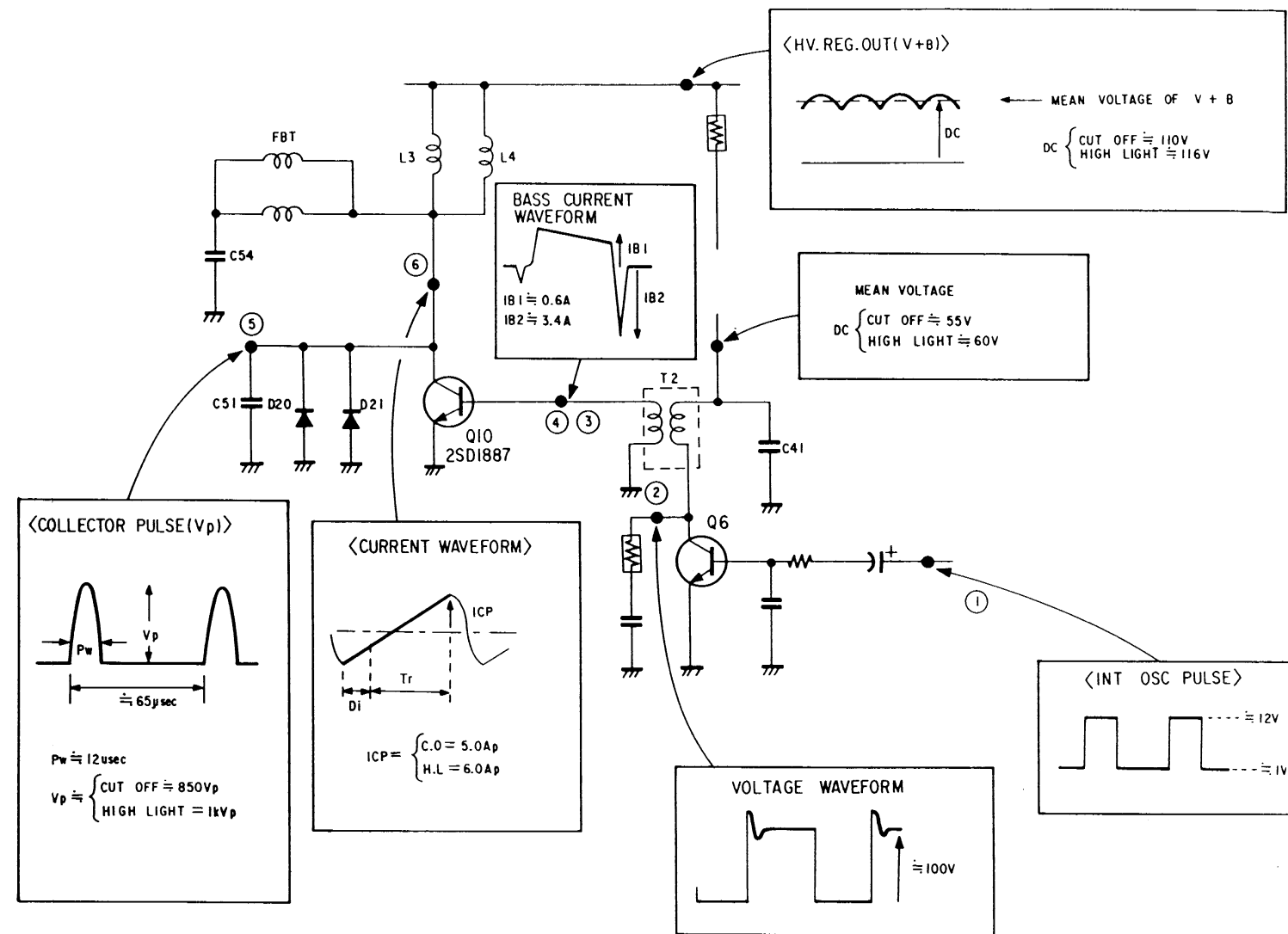


Fig. 10-2. Simplified circuit diagram (HV generator).

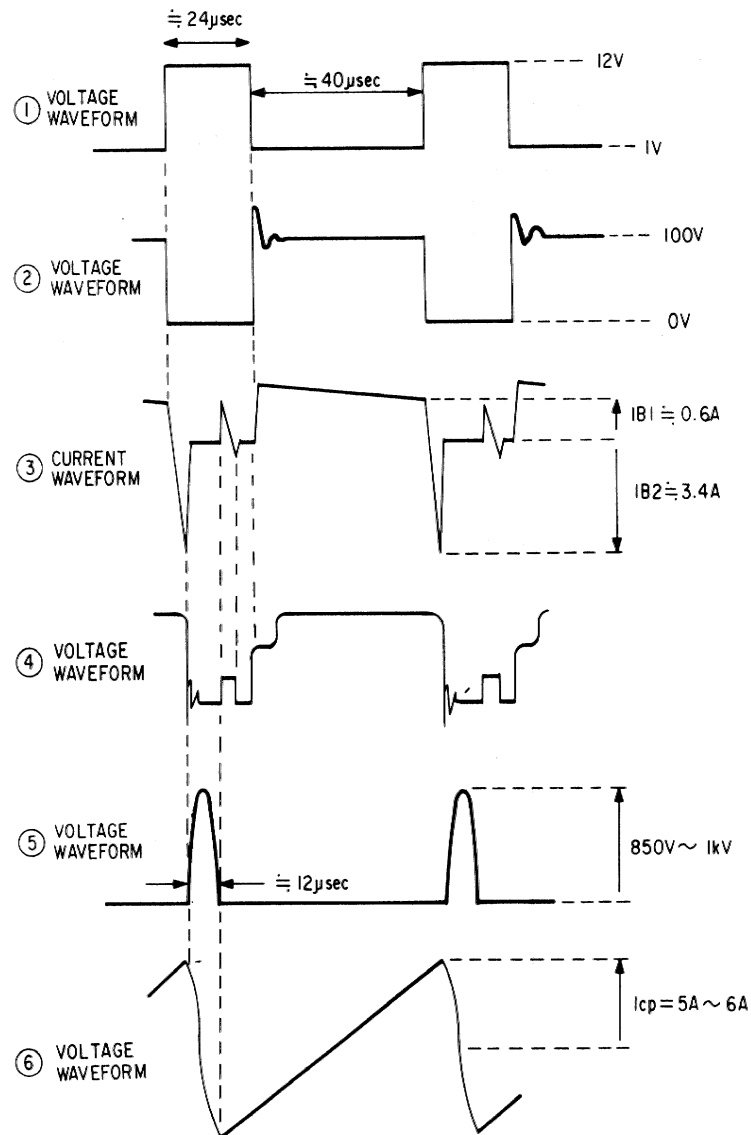


Fig. 10-3. Major waveform (HV generator).

3-10-3. HV Regulator

High voltage generation is done by rectifying pulses generated in the secondary winding of FBT using diodes and a capacitor. Regulation of this high-voltage, however, is poor because of its circuit configuration. That is, the heavier HV load (beam current increases), the less high-voltage.

Beam current increases → Ripple in HV increases →
Mean HV drops.

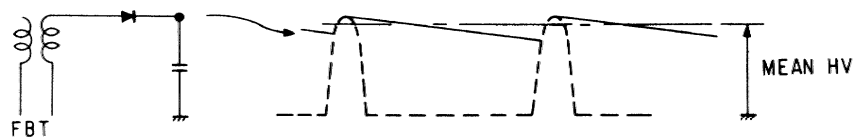


Fig. 10-4

Even with heavy load, you can achieve high mean HV by increasing pulse height in the secondary winding. FBT is a simple step-up transformer. The higher primary pulse height, the higher secondary pulse height. Configuration of HV regulator is as follows: It detects mean HV with a method available, and controls FBT's primary pulse height to maintain mean HV constant regardless of change in HV load.

Now let's consider how to control the primary pulse height. As described in preceding 3-10-2. HV Generator] section, pulse height V_p is calculated by following equation:

$$V_p = \frac{V + B(1/f_h - T_w)}{2\sqrt{LC}}$$

The equation shows that V_p also affected by power supply voltage ($V+B$). In this projector, a step-up type switching regulator is used to step-up +100V to $V+B$. Control to the pulse height V_p is done by control to $V+B$ (that is, control to portion of stepped up).

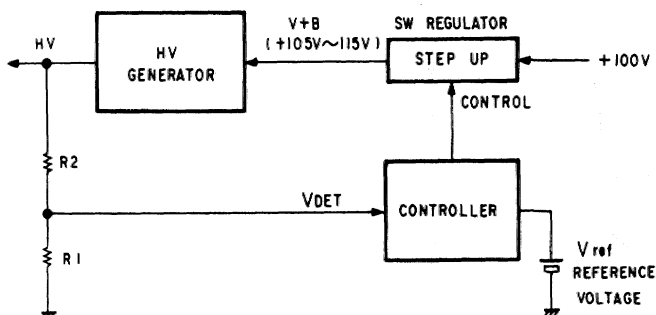


Fig. 10-5. Basic configuration of HV regulator

The system controls stepped up portion from +100V to keep V_{DET} to V_{REF} (reference voltage).

a) Switching regulator

Fig. 10-6 shows basic configuration of switching regulator.

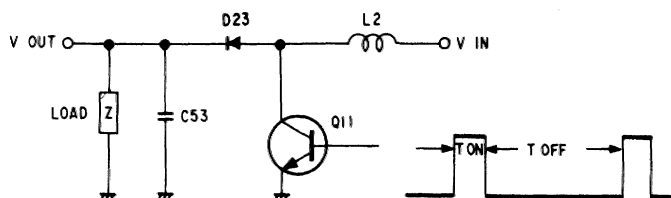


Fig. 10-6

Q11 is switching transistor. Step-up of input voltage (V_{IN}) is achieved by periodically turning Q11 ON and OFF. In this case, output voltage (V_{OUT}) is calculated by following equation:

$$V_{OUT} = \frac{T_{ON} + T_{OFF}}{T_{OFF}} V_{IN}$$

As you can see from the equation above, step-up voltage ΔV (i.e., $V_{OUT} - V_{IN}$) by the switching regulator is determined by Q11's switching duty (ratio between T_{ON} and T_{OFF}).

Operation of switching regulator is as follows:

Part numbers shown in following paragraphs correspond to the ones used in this switching regulator.

ON-OFF pulse (square wave) which determines the step-up portion (ΔV) is output from pin ⑦ of IC6 ($\mu PC1394C$) in negative polarity. The output pulse passes a buffer (Q20), then turns transistor Q5 ON and OFF. Q5 drives the primary winding of drive transformer T1, and the output pulse from T1's secondary winding turns the switching transistor Q11 ON and OFF. Polarity of pulse is inverted in T1.

b) HV detection circuit, and control circuit to switching regulator

Following sequence shows the simplified HV control derived from preceding description:

HV control ← control to FBT's secondary pulse height ← control to FBT's primary pulse height ← control to $V+B$ ← control to ΔV from switching regulator ← control to Duty of switching

That is, duty (ratio between T_{ON} and T_{OFF}) of switching pulse which controls the switching regulator determines the control to HV.

Now let's consider the outline of how to generate this switching pulse (and control to its duty). Fig. 10-6 shows its simplified circuit diagram.

First, HV is divided by high resistors to obtain a low level (about 8V) of voltage. The voltage passes a buffer and a resistive divider to obtain a final voltage level of about 3V. This is HV detect voltage. The HV detect voltage enters to non-inverting input (pin ① of IC6) of an operational amplifier. The operational amplifier forms a non-inverting amplifier, and its reference voltage V_{REF} is set to 3V. That is, HV is divided to about 3V (HV detect voltage), and the non-inverting amplifiers used to detect the error between HV detect voltage and the reference voltage ($V_{REF} = 3V$).

Amplitude of this error voltage is determined by R129 and R58 which determines DC gain of the amplifier, and appears on output terminal (pin ⑬ of IC6) of the amplifier. The error voltage enters to positive input of a comparator. On the other hand, a sawtooth waveform with some period enters to negative input of the comparator. This causes comparator's output to be square wave with constant period. The output pulse is used as the switching pulse to control the switching regulator.

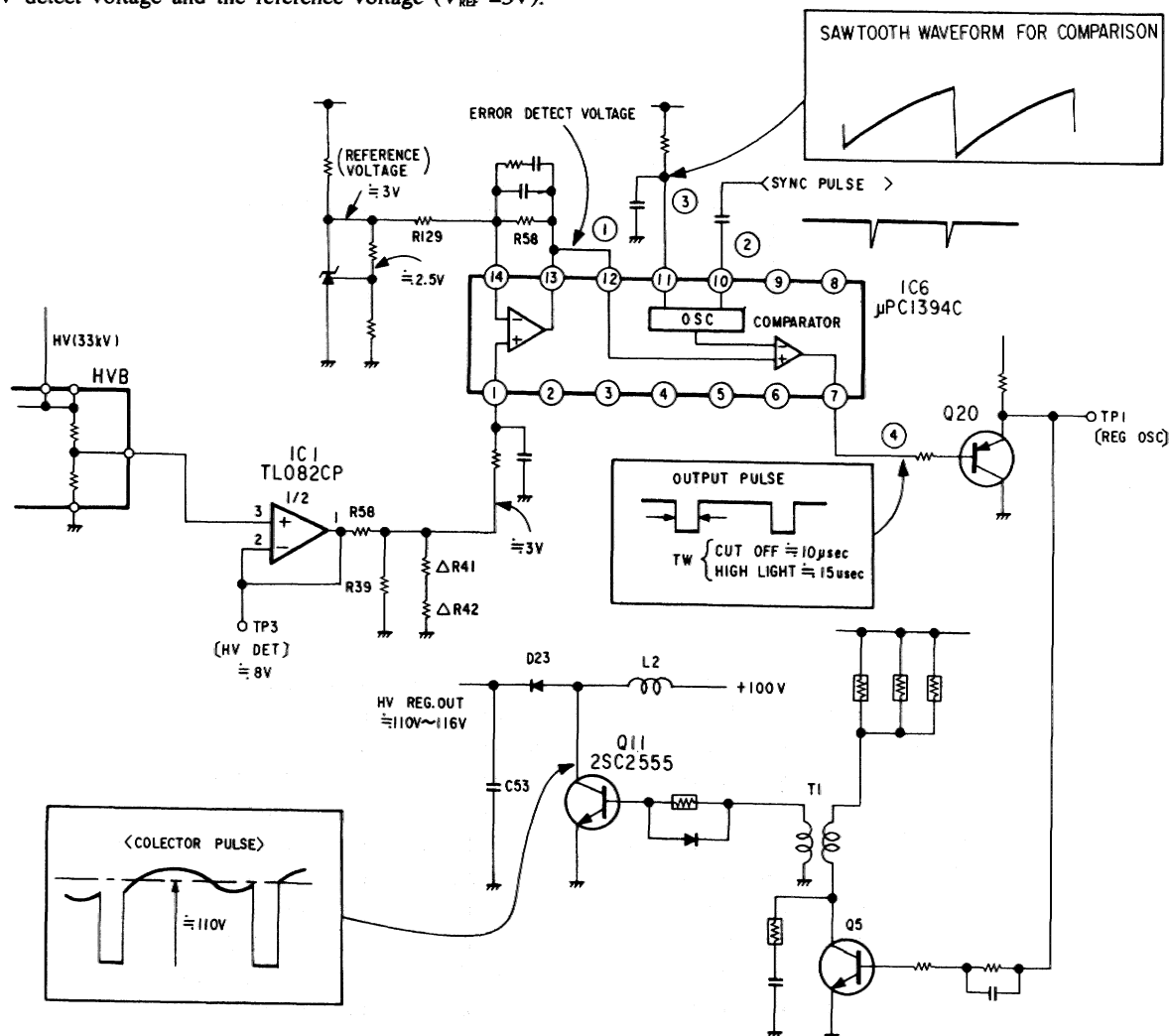


Fig. 10-7. Simplified circuit diagram (HV regulator).

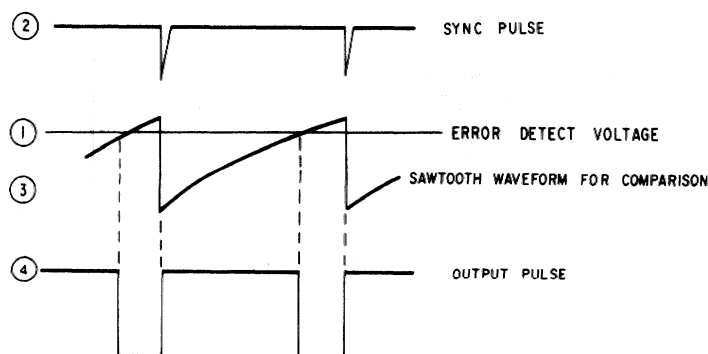
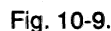


Fig. 10-8.

HV drops \rightarrow divider voltage (HV DET) drops \rightarrow output of operational amplifier drops \rightarrow T_{ON} of comparator's output increases

Now you understand that the circuit is a feedback loop in total, do you?

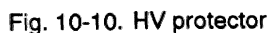
That is, the reference voltage (V_{REF}) of non-inverting amplifier is used as reference of feedback operation to make HV detect voltage (HV DET) always equal to V_{REF} (3V).



(1) HV protector

A reference voltage (about 4.8V) derived from a zener diode (RD5.1ESB2) is applied to negative input (pin ⑥) of IC2 (1/2 of LM393P). If HV increases and the voltage on positive input (pin ⑤) of the comparator exceeds the voltage on negative input (pin ⑥), the protector is activated. Sequence of operation is as follows: Output of

1/2 of IC2 (pin ⑦) becomes High (about 12V), and voltage on positive input (pin ③) of 2/2 of IC2 exceeds the voltage on negative input (pin ②) of the IC. This causes output (pin ①) of 2/2 of the IC to be High. This is applied to IC6 via D8 (1SS119) to make pin ⑤ of IC6 (μ PC1394C) to High state (about 1V), and oscillation of HV regulator stops. Then Q7 (2SC2785) is turned ON to stop oscillation of HV converter. After deactivating HV, D28, Q16 and Q15 are turned ON to turn the power supply OFF. At the ex-factory, \blacksquare R33 and \blacksquare R34 are set to activate this protector with HV at $34\text{kV} \pm 0.3\text{kV}$.

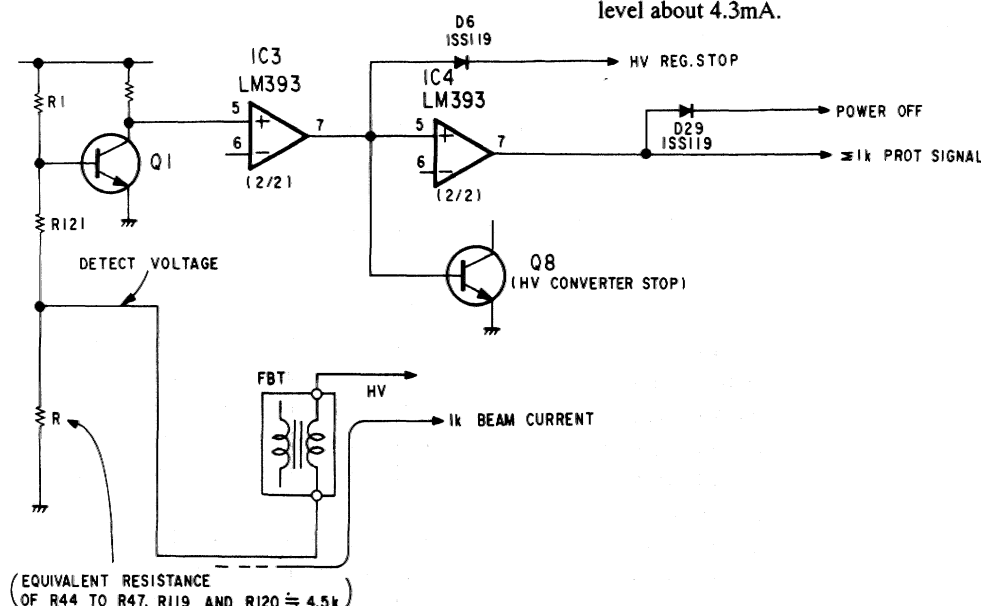


(2) ΣI_k protector ①

This is the protector to protect CRT from excessive beam current flow. R44, R45, R119, R46, R47 and R120 are used to convert FBT's secondary current into voltage. If the voltage exceeds a threshold level (about 18V), the protector is activated. Voltage detected here is divided by R121 and R1, then is applied to the base of Q1 (2SC2785). Q1 is always turned ON in normal state of operation. Increase in beam current causes the detected voltage to go down to negative direction, and Q1 is turned OFF at a threshold level to activate the protector.

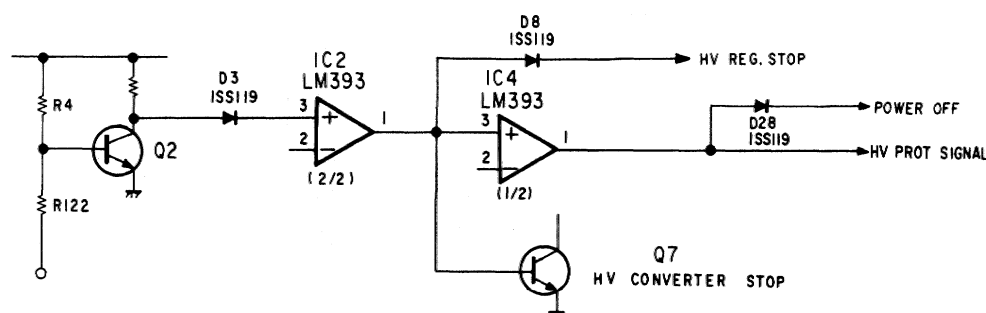
Sequence of operation is as follows:

Q1 is turned OFF \rightarrow collector of Q1 becomes High (about 12V) \rightarrow voltage on positive input (pin ⑤) of 2/2 of IC3 (LM393P) becomes higher than that on negative input (pin ⑥) \rightarrow output (pin ⑦) of the IC becomes High. After that, with a sequence similar to that in case of HV protector, D6 (1SS119) stops oscillation of HV regulator \rightarrow Q8 (2SC2785) is turned ON \rightarrow oscillation of HV converter stops \rightarrow diode/transistors operate in the order of D29, Q16 and Q15 to turn the power OFF. ΣI_k protector is designed to be activated if FBT's secondary current (= sum of beam current flow in CRT) exceeds a threshold level about 4.3mA.

Fig. 10-11. ΣI_k Protector ①(3) ΣI_k protector ②

Because of requirement from safety specifications, a spare ΣI_k protector is installed to protect CRT even if ΣI_k protector ① fails by some chance or other. Its operation is similar to that of ΣI_k protector ①, that is, the protector is activated when the detect voltage drops and Q2 is turned

OFF. Collector of Q2 is connected to positive input (pin ③) of 2/2 of IC2 (LM393P) via D3 (1SS119). This is a part of HV protector circuit, and the operation after D3 is same with that of HV protector. Current level where the protector is activated is same with that of ΣI_k protector ①.

Fig. 10-12. ΣI_k Protector ②

(4) LOW +B protector

This protector is activated if IC5 (LM7812CT) which generates Low +B (+12volts) fails, and Low +B (+12 volts) increases. Low +B (+12 volts) is divided using a resistive divider, and is applied to non-inverting input (pin ⑤) of 2/2 of IC1 (TL082CP). On the other hand, a reference voltage (about 4.8V) derived from a zener diode D10 (RD5.1ESB2) is applied to inverting input (pin ⑥) of the IC.

If Low +B increases, voltage on non-inverting input (pin ⑤) becomes higher than that on inverting input (pin ⑥). This causes the IC's output (pin ⑦) to go to High, and the protector is activated via D11 (1SS119). D11 is connected to a portion of circuit of Σ Ik Protector ①. Operation after D11 is similar to that in Σ Ik Protector ①.

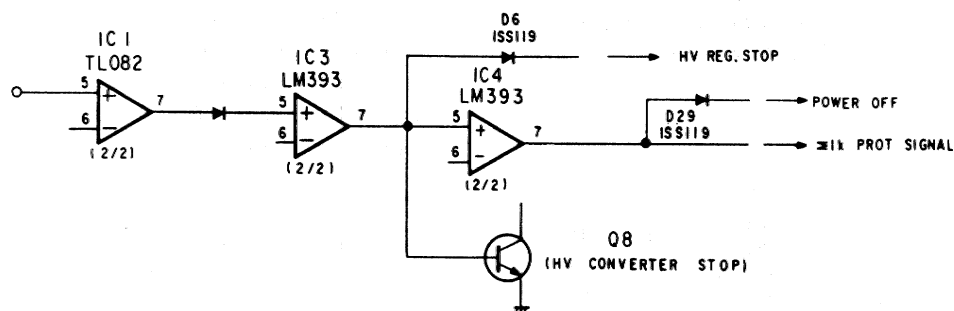


Fig. 10-13. LOW +B Protector

(5) HV regulator protector

This protector protects components, such as switching transistor, etc., from being damaged. Protection is done by stopping oscillation of HV regulator at the occurrence of abnormal high voltage in HV regulator. Output voltage from HV regulator is divided by R48, R49, R50, R14 and R15, and the resultant voltage is applied to positive input (pin ③) of 1/2 of IC3 (LM-393P). Reference voltage (about 4.8V) enters to negative input (pin ②) of the IC. If regulator's output voltage increases, voltage on positive input (pin ③) becomes higher than that on negative input (pin ②). This causes IC's output (pin ①) to be High, and pin ⑤ of IC6 (μ PC1394C) to be High (about 1V) via D7 (1SS119), and oscillation of switching regulator to stop. The protector is designed to be activated at about 140V of regulator's output voltage.

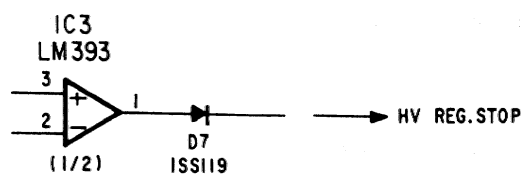


Fig. 10-14. Rebruator stop

(6) Power off circuit

To prevent secondary damage to occur in case of abnormal operating modes (e.g., deflection stop), circuit system of this projector is designed to turn immediately the power supply OFF in such cases. Of these protect signals, H. STOP (H deflection stop), V STOP (V deflection stop), FAN PROT (fan protector), HV protector, and Σ Ik protector are all concentrated to PA board to turn the power supply OFF.

H. STOP and V. STOP are OPEN collector outputs, and they are ORed by D24 and D25. In abnormal operating modes, Q16 and Q15 are turned ON to pull "POWER CONT" line down to Low state, and this causes the power supply to be turned OFF. "FAN PROT" signal is in polarity reversal to that of H. STOP or V. STOP, i.e. it is normally ON. Q17 is used to invert the polarity of FAN PROT signal, and apply it to Q15 in polarity same with that of V. STOP or H. STOP.

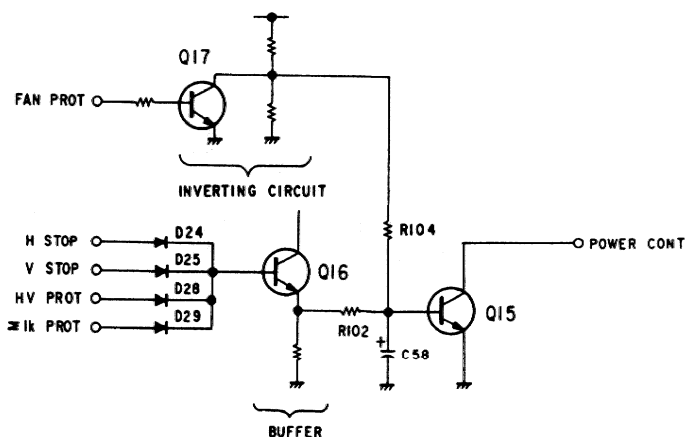


Fig. 10-15. Power off circuit

3-10-5. HV Building-up Control Circuit

In power-on sequence, this circuit prevents HV regulator from operating until +100V power supply reaches to its complete building-up, to obtain a softer HV building-up curve.

Emitter of Q12 is connected to the power supply (pin ⑧) of IC6. Voltage on this point is regulated by a shunt regulator internal to IC6, and is about 6.4V. +100V is divided by R92 and R93, and is applied to the base of Q12. If the base voltage is lower than 5.7V (that is, emitter voltage (6.4V) minus V_{BE} (0.7V)), then Q12 is turned ON. This causes voltage on pin ① of IC6 to be nearly equal to emitter voltage (6.4V) of Q12. IC6 deems this as if HV detect voltage is higher than normal state, and prevents HV regulator's switching pulse from being output.

When +100V builds up about 90V, then Q12 is turned OFF. Normal operation starts, and HV regulator starts its operation.

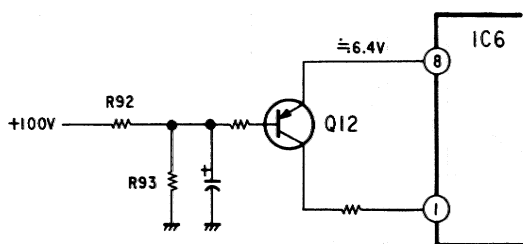


Fig. 10-16.

3-10-6. G2 Regulator

Essentially, G2 voltage (SCREEN) and G4 voltage (FOCUS) are generated by dividing medium voltage output ($MV \approx 14kV$) from FBT using resistive dividers built in FOCUS PACK.

But sometimes, leak current from G4 terminal caused by discharge in CRT, etc., may flow into FOCUS PACK. The leak current is very small (less than $50\mu A$), but this causes change in high voltage to occur because impedance of FOCUS PACK is very high. Change in G2 voltage has much effect to picture quality than in G4 voltage. In this case, pedestal level in R, G, B channels shifts to a higher level, and results in change of white balance.

G2 regulator prevents change in G2 voltage regardless G4 leak current. Regulator's configuration is as shown in Fig. 10-17. Voltage on COMMON terminal is determined by a resistor R116 and the resistance in FOCUS PACK, and does not change even if G4 leak current flows.

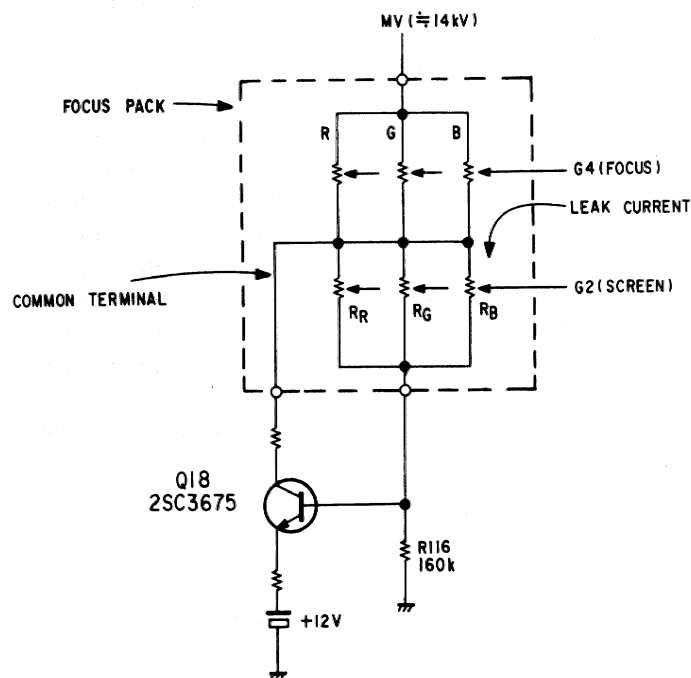


Fig. 10-17. Simplified circuit diagram of G2 regulator

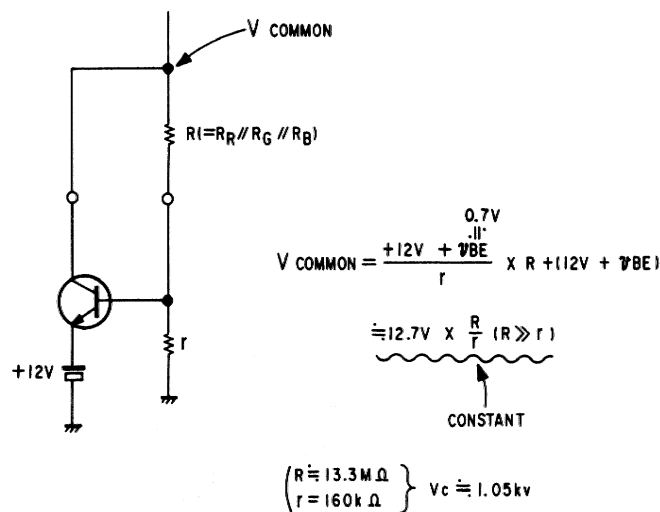


Fig. 10-8 Equivalent circuit diagram of G2 regulator

3-11. CIRCUIT OPERATION OF K BOARD

3-11-1. H Dynamic Focus

H. parabola waveform entered to pin ⑦ of connector "K-1" and H. sawtooth waveform entered to pin ⑧ of that connector are added together. After phase correction performed, the resultant waveform is inverted by 1/2 of IC201 (μ PC814). IC202 (μ PC814) and Q202 are used to amplify this inverted waveform. Output waveform passes a buffer (Q205 and Q206), then enter to dynamic focus transformer (DFT). DFT inverts the waveform, and amplitude of DFT output is 400Vp-p in case of input waveform of 30Vp-p to DFT.

Waveforms in dynamic focus circuit with no signal input are as shown below:

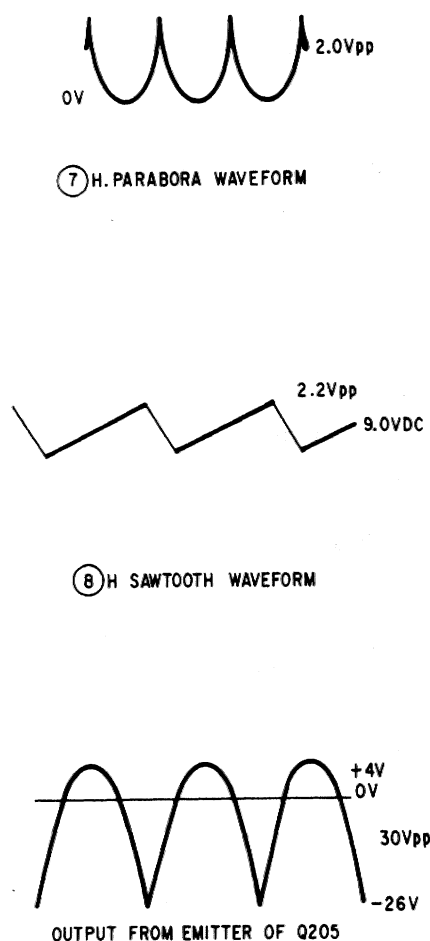


Fig. 11-1.

3-11-2. V. Dynamic Focus

Dynamic focus waveform is added to focus voltage by capacitor-coupling in FOCUS PACK. Use of a capacitor with large capacitance is impossible because of restriction from withstanding voltage and size. In practice, a capacitor with small capacitance of only 100pF is used. Frequency of V. waveform is very low compared to that of H. waveform. Decrease in amplitude or phase rotation may occur with small capacitance of coupling capacitor. Circuit configuration shown below is adopted to enable transfer of V. focus waveform. Desired waveform is obtained by placing a time constant in the negative feedback loop same with that of C, R in FOCUS PACK.

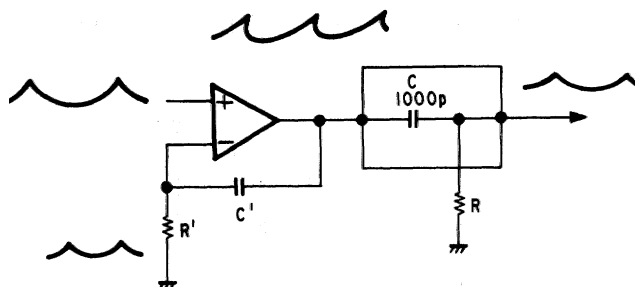


Fig. 11-2. Equivalent circuit

2/2 of IC201 (μ PC814) is an operational amplifier for negative feedback, Q203 is an inverting amplifier, and Q204 is output buffer. Time constant of C210 ($0.47\mu\text{F}$) and R212 (10kohms) matches to the time constant of circuit in FOCUS PACK. DC feedback through this CR circuit is impossible because it is a differentiating circuit. So, after integration by R214 and C209, feedback is done from R213. To obtain V component amplitude of 100Vp-p in FOCUS PACK, output amplitude of Q204 changes in 150Vp-p to 400Vp-p range in accordance with V frequency. The output is applied to DFT's secondary winding, and V component is superposed on H component. Resultant waveform is entered to FOCUS PACK.

Waveforms in V dynamic focus circuit and DF output on connector "K-2" are as shown below:



⑥ V.PARABORA WAVEFORM

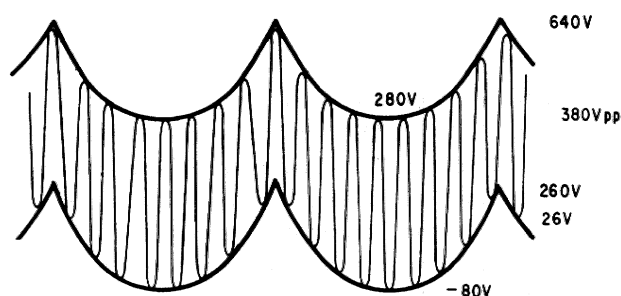
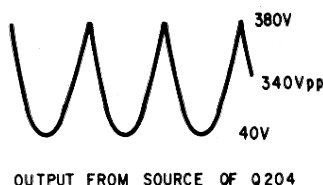


Fig. 11-3. DF output on connector K-2

3-12. CIRCUIT OPERATION OF Y BOARD

3-12-1. Power Supply Block

PS1 and PS2 are used as fuses to cut the power supply OFF at occurrence of over-current in Y board. D1 reduces input voltage +5.7V to +5.0V, and D2 reduces input voltage -5.7V to -5.0V.

Sub +5.0V is supplied at main power-on of the projector, and $\pm 5.7V$ are supplied when powered the projector ON from the commander.

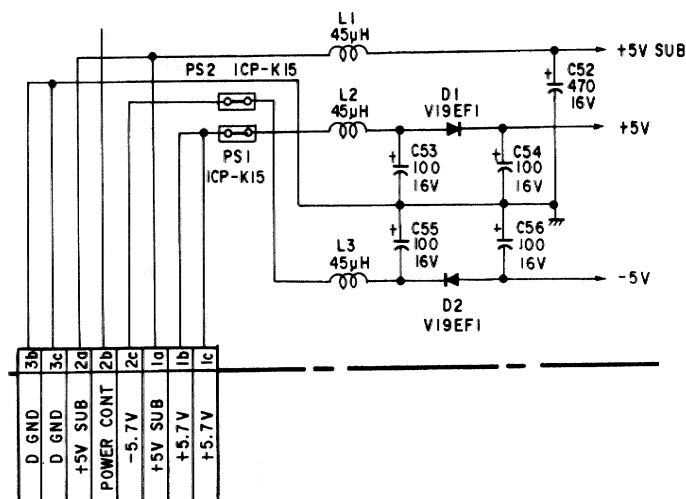


Fig. 12-1. Circuit diagram of power-supply block

3-12-2. CPU Block

1. CPU (IC1 HD64180R1P8)

HD64180R1P8 is selected as CPU (IC1). This is a CPU of Z80 type, and SIO/TIMER/DMA functions are incorporated in 1-chip. It also includes clock oscillation circuit, and in addition to NMI, it is equipped with 3 interrupt levels.

① Clock (X1)

Based upon baud rate of RS422 serial communication, clock frequency of 12.288MHz is selected. A quartz crystal (X1) is used. (Internal operating frequency is 6.144MHz.)

② Assignment of interrupt lines/ports

- * NMInot defined
- * INT0power off/power down (protector)
- * INT1SW2 (data reset)/VD (refresh)
- * INT2SIRCS receive
- * SIO ch0RS422 (internal interrupt)
- * TIMER A ..100msec timer 1 (for software timer)
- * TIMER B ..100msec timer 2 (for SIRCS continuance detection)

3-12-3. I/O Port Block

1. Parallel Interface and Interrupt control

(IC10 : MB670840PF)

IC10 is equipped with 6 sets of 8 bit parallel port shown below for detection of operating status of the set and control to various functions. A "Programable. Port" is the

port which permits IN/OUT presteting on each bit by software, and if it is preset to IN, also permits presetting connection to ports (INT0 to INT2) at the time of interruption (High active or Low active).

* IN-port 1 INPUT STATUS/SYSTEM STATUS					
pin-95 bit7 "NOINP"	no-input detect [0: no-det, 1: detect]				
pin-96 bit6 "I/V"	RGB/Video [0: RGB, 1: Video]				
pin-97 bit5 "LP"	[0: norm]				
pin-98 bit4 "3HD"	3-sync detect [0: norm, 1: detect]				
		B/W	PAL	NTSC	SECAM
pin-99 bit3 "CD2"	code 2	0	0	1	1
pin-100 bit2 "CD1"	code 1	0	1	0	1
pin-1 bit1 "V/Y"	Video/YC (S-terminal) [0: YC, 1: Video]				
pin-2 bit0 "R/V"	Input Video/RGB [0: Video, 1: RGB]				
* OUT-port 1 SYSTEM CONTROL					
pin-5 bit7 "C/B"	[don't care]				
pin-6 bit6 "R/Y"	[don't care]				
	Video	Slot-A	Slot-B	CCQ	
pin-9 bit3 "CCQ"	1	0	0	0	
pin-10 bit2 "SLOT"	1	0	0	1	
pin-11 bit1 "S2"	1	1	0	1	
pin-12 bit0 "S1"	1	0	1	1	
* OUT-port 2 SYSTEM CONTROL					
pin-86 bit7 "BOF"	Blue Beam Cut-off [0: norm, 1: cut off]				
pin-87 bit6 "GOF"	Green Beam Cut-off [0: norm, 1: cut off]				
pin-88 bit5 "ROF"	Red Beam Cut-off [0: norm, 1: cut off]				
pin-89 bit4 "SEC"	Secam on/off [0: on, 1: off]				
pin-94 bit0 "CB"	Clear Blue on/off [0: on, 1: off]				
* OUT-port 3 SYSTEM CONTROL					
pin-13 bit7 "DLY"	Clamp Pulse Delay [0: norm, 1: delay]				
pin-14 bit6 "PHS"	Clamp Pulse Trigger Source Select [0: ext-sync, 1: int-sync]				
* Programmable-port 1 DIP SW, etc.					
pin-32 bit7 IN "V-I"	Def. V-invert [0: norm, 1: inv]				
pin-33 bit6 IN "H-I"	Def. H-invert [0: norm, 1: inv]				
pin-34 bit5 OUT "LED"	LED (D4) [0: off, 1: on]				
pin-35 bit4 IN (int1) "5"	SW2 [0: on, 1: off]				
pin-36 bit3 IN "4"	SW1-4 [0: on, 1: off]				
pin-37 bit2 IN (int1) "3"	VD (for refresh) [pos-pulse]				
pin-38 bit1, 0 IN "2, 1"	SW1-2, 1 [0: on, 1: off]				
* Programmable-port 2 PROTECTOR/POWER					
pin-22 bit7 IN (int0) "+5V"	+5V power [0: power off, 1: norm]				
pin-23 bit6 IN (int0) "POW"	Power Cont. [0: on, 1: off]				
pin-24 bit5 IN (int2) "CONT"	SIRCS receive [0: active, 1: norm]				
pin-25 bit4 IN (int0) "HV"	High-Vol Protect [0: norm, 1: act]				
pin-26 bit3 IN (int0) "VP"	V-Stop Protect [0: norm, 1: act]				
pin-27 bit2 IN (int0) "IKP"	Ik-over Protect [0: norm, 1: act]				
pin-30 bit1 IN (int0) "HP"	H-Stop Protect [0: norm, 1: act]				
pin-31 bit1 IN (int0) "FP"	Fan Stop Protect [0: act, 1: norm]				

Table 12-2.

2. DIP SW (SW1, SW2)

SW1 is used to set up special operating mode required in factory adjustment. All bits (SW1-1 to -4) are set to "0" in normal operation.

Pressing SW2 causes all adjustment data to return to factory default.

3-12-4. SIRCS Decode IC Interface

1. Sircs code read process

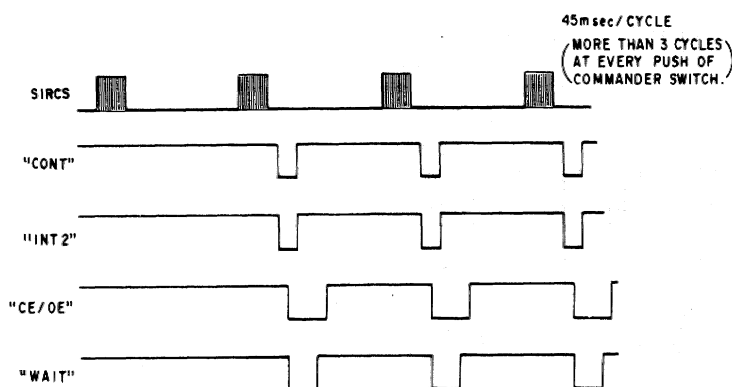


Fig. 12-3

- (1) SIRCS IC (IC9) pulls down "cont" terminal to Low state when it receives continuous 2 cycles of same SIRCS code.
- (2) The "cont" signal sends interrupt request (int2) to CPU via IC10.
- (3) After acknowledged the interrupt request, CPU reads the port of IC9, and CE/OE terminal of SIRCS IC (IC9) is pulled down to Low state.
- (4) At the same time, a monostable multivibrator (IC6) is triggered, and CPU becomes WAIT state.
- (5) With its CE/OE terminal in Low state, IC9 outputs decoded data onto data bus, and "cont" terminal returns to High state. At the same time, the interrupt request to CPU is released.
- (6) After a few milli-seconds, the monostable multivibrator is released. This releases WAIT state of CPU, and CPU acquires data.
- (7) After reading data, CPU returns CE/OE terminal to High state.

With the sequence described above, CPU acquires SIRCS CODEs.

WAIT state is required to give a time of software execution on IC9 because IC9 is an 1-chip microcomputer.

* SIRCS CODE: category code for PJ "00101010"

2. Power ON/OFF & protector operation

① Normal POWER ON/OFF (IC9, Q3)

SIRCS IC (IC9) controls normal POWER ON/OFF initiated from the commander independent from CPU. This is done to perform POWER ON/OFF regardless malfunction of CPU or software bugs.

POWER ON/(OFF) sequence is as follows:

POWER ON

- (1) At receiving POWER ON CODE, SIRCS IC pulls down "power" terminal (pin ②) to Low state.
- (2) Q3 is turned ON, and current flows via R67 and R124 to turn the power supply unit ON.

POWER OFF

- (1) At receiving POWER OFF CODE, SIRCS IC pulls up "power" terminal (pin ②) to High state.
- (2) Q3 is turned OFF, and current flow through R67 and R124 stops, and the power supply unit is turned OFF.

② PROTECTOR operation (IC9, Q4, Q5)

Forced pull-down to GND of "POWER CONT" line, which controls the power supply unit, causes automatic power shut-down to occur at activation of PROTECTOR circuit. In this case, simultaneous reset to SIRCS IC (IC9) is required to prevent oscillation of the circuit because Q3 is still ON regardless of GND level on "POWER CONT" line, and this causes the power supply unit to be turned ON again.

To prevent the oscillation to occur, reset at PROTECTOR operation is done in following sequence:

- (1) At the activation of PROTECTOR, "POWER CONT" line is externally pulled down to GND.
- (2) Collector current of Q3 increases very much, and Q4 is turned ON.
- (3) Base current of Q5 flows through a low-pass filter (R69, C14, C65), and Q5 is turned ON.
- (4) "RESET" terminal of IC9 becomes Low state. This resets IC9, and Q3 is turned OFF.

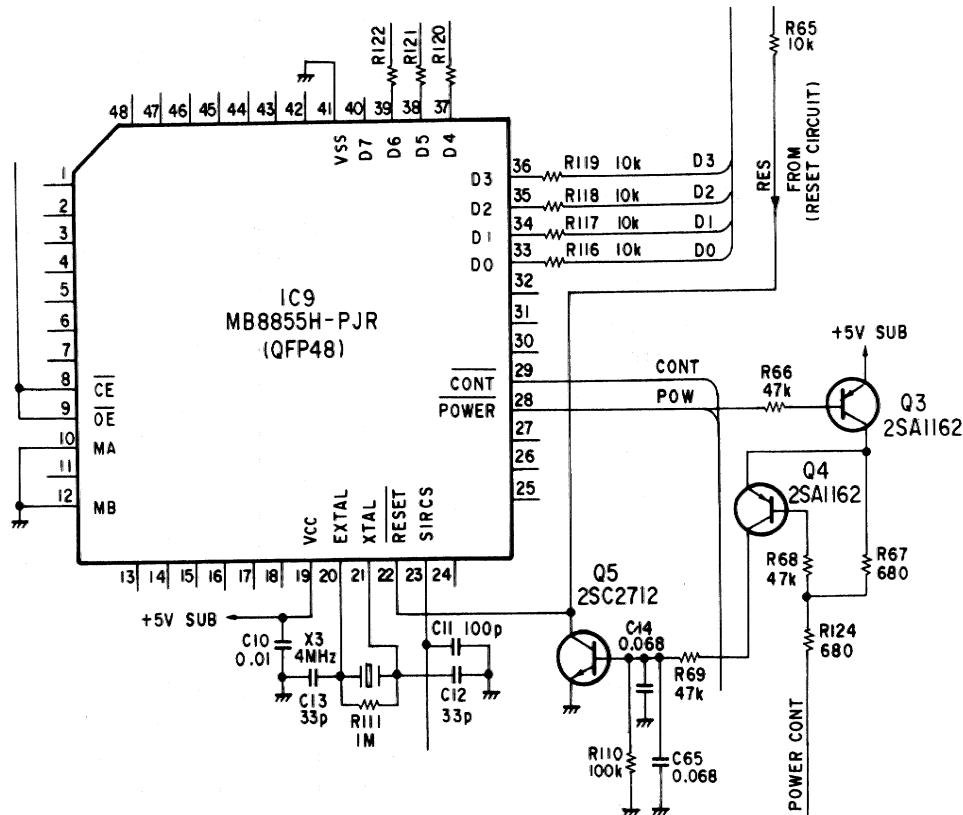


Fig. 12-4 Circuit of SIRCS decode block

3-12-5. SYNC Block

1. Input sync presence/polarity detection (IC11 MB654842UPF)

① INPUT SYNC PRESENCE DETECTION

3 types of SYNC signal enters to IC11. Detection in presence of input signal is done per following conditions:

* H/C sync (TTL level)

With Video input, composite-sync separated from input video on BB board enters to IC11. With RGB input, signal connected to H/C-sync terminal (pin ③) enters to IC11. Presence of input signal is determined simply by presence of sync pulse.

* V sync (TTL level)

With Video input, V-sync separated from input video on BB board enters to IC11. With RGB input, signal connected to V-sync terminal (pin ②) enters to IC11. Presence of input signal is determined simply by presence of sync pulse. Detection circuit operates only with presence of HD input.

* Sync on Green (TTL level)

With Video input, composite-sync separated from input video on BB board enters to IC11. With RGB input, composite-sync separated from Green signal (pin ③) on BB board enters to IC11. IC11 determines that input is present if non-changing intervals of more than $180\mu\text{S}$ appear at a period less than 30msec, and that input is not present if such interval does not appear.

NOTE:

At the 1st step, signal connected to H/C-sync input terminal is deemed as composite-sync. IC29 detects the presence of pulse on V-sync out terminal of IC11. If the pulse is present, then input signal is determined as composite-sync. If not, it is determined as H-sync. Also in SonG mode, detect condition above may not be satisfied if V-sync has no serration with H (H/2) period. In this case, final determination is done by presence of V-sync out when SonG mode is selected.

② INPUT SYNC POLARITY DETECTION

* H/C sync, V sync

Principle of polarity detection is: an UP/DOWN counter counts period of one-cycle of input sync to determine polarity of sync based on the counted value.

* Sync on Green

Negative polarity only, in this case.

2. Sync select (IC11, IC34)

① SYNC SOURCE SELECTION

Based on the presence of input, source selection of H-sync/V-sync to be sent to deflection system is done. Priority is given to external SYNC. CPU determines the state as shown in the table below, and controls IC11 via CPU bus.

sync detection			sync source selection	Clamp pulse trigger *
VD	HD/C	SonG	DATA PJ	
—	—	—	no-input	—
—	—	DET	SonG	SonG
—	HD	—	no-input	HD
—	C	—	C-sync	C-sync
—	HD	det	SonG	SonG
—	C	det	C-sync	SonG
det	—	—	no-input	—
det	—	det	SonG	SonG
det	HD	—	HD/VD	HD
det	C	—	C/VD	C-sync
det	HD	det	HD/VD	SonG
det	C	det	C/VD	SonG

* : Selection of clamp pulse in "page 3" display during Auto mode.

Table 12-3.

② SYNC OUT SELECT (IC34: MC74HC157)

Selection of H-SYNC and V-SYNC to be sent from Y board to deflection system (DA board) is done as shown below using a signal selector IC34.

* With Video input

H-SYNC/V-SYNC separated from composite video on BB board are sent to deflection system (regardless of IC11's output).

* With RGB input

H-SYNC/V-SYNC controlled in IC11 (as described in section ①) are sent to deflection system.

* Relationship between "sync source selection" in the table 12-3. and H-SYNC/V-SYNC out from IC11 is as shown Table 12-4.

sync source selection	H-SYNC out (pin 59)	V-SYNC out (pin 60)
no-input	—	—
SonG	H-SYNC separated from SonG	V-SYNC separated from SonG
C-sync	H-SYNC separated from composite SYNC	V-SYNC separated from composite SYNC
HD/VD	H-SYNC derived from HD and in negative polarity	V-SYNC derived from VD and in negative polarity
C/VD	H-SYNC separated from composite SYNC	V-SYNC derived from VD and in negative polarity

Table 12-4.

3. Unified sync polarity (IC11)

Polarity of H/C-sync or V-sync is different depending upon computer systems connected. In this projector, IC11 determines sync polarity, and sends the information to CPU. IC11 also processes sync signal to make sync polarity uniform, i.e., negative polarity.

4. H/V separator (IC11)

If the selected SYNC SOURCE is C-sync or SonG, it is necessary to separate H-sync and V-sync from it to send them to deflection system.

This is done by "Digital H/V-separator" in IC11. The separator requires no adjustment in 15 kHz to 92 kHz range. If equalizing pulses exist, they are separated and are output.

Sync outputs from IC11 are H-sync (pin 59) and V-sync (pin 60). They are signals of TTL level.

NOTE:

Weak point of "Digital H/V-separator" is unstable output for about 0.5 sec. at interrupt of input signal or at change in frequency. Without V-sync for about 0.5 sec., free-running of AFC circuit occurs. Time required to lock-up to the next sync input is about 5 seconds. To cope with this problem, the software is so designed that sync from internal SG is used until completion of signal switching.

5. Clamp pulse generation (IC11, IC30, IC31)

Generation of back-porch clamp pulse (from pin ⑤③) is done depending on types of "Clamp Pulse Trigger" described in section 5-2, and at the timing shown below:

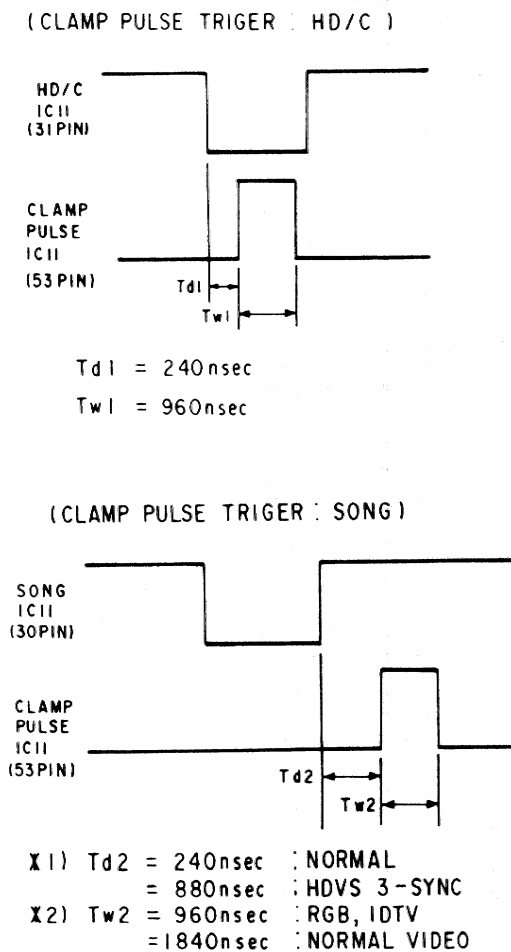


Fig. 10-5

- * 1) Control is done from pin ⑤③ of IC11.
- * 2) Control is done from pins ④①, ③⑧ and ③⑦ of IC11.

NOTE 1:

Values shown above are center of design, and in practice, they distribute in +40 nsec. to -40 nsec. range.

NOTE 2:

If V-sync has no serration, and input signal is C-sync or H/C-sync, possibility of missed clamping exists because no correct detection in presence of SonG is possible. In such a case, disconnection of external sync signal is requested. If disconnection of sync only is impossible because a D-sub pin ⑨ connector is used, a special procedure (In "Page" mode, change "clamp pulse setup" on sync signal selection as the trigger for clamp pulse generation. This will be possible on software version '012' and after.) is necessary.

< Clamp pulse Trigger: H.P = H pulse >

When an input signal causes missed clamping to occur regardless of clamp pulse selection (i.e., Auto, SonG, or H/C) in "Page 3" mode:

(ex. SonG input only, and B.P. is less than 960ns).

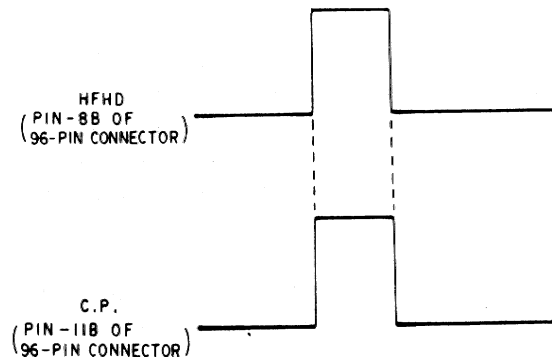


Fig. 10-6

NOTE:

Clamp pulse output from Y board differs depending upon clamp pulse selection in "Page 3" mode.

- (1) Clamp: Auto / H/C / SonG,

Output from pin ⑤③ of IC11 is selected as the output on pin 11b of 96 pin connector.

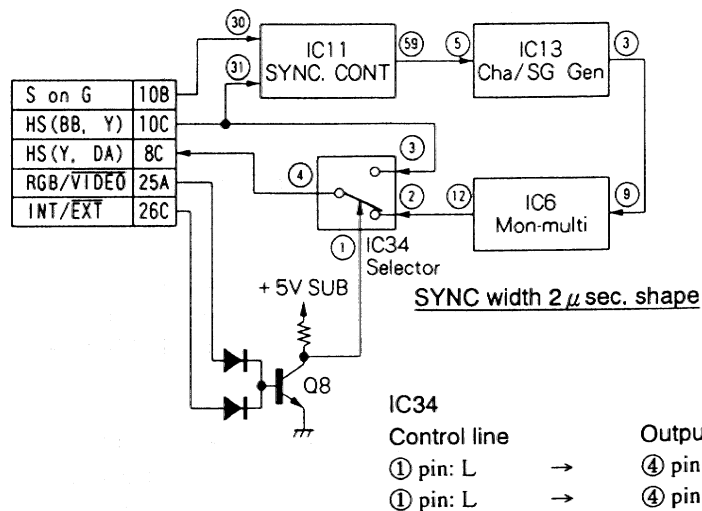
- (2) Clamp: H. P

Clamp: H.P H. pulse (HFHD: pin 8b of 96 pin connector) from deflection system is output from pin 11b of 96 pin connector.

Switching between (1) and (2) is done by control from CPU to a signal selector consisting of IC30 (74HC126) and IC31 (74HC14).

6. Sync width regulation of H-Sync out (IC6: 74HC123)

Except during video input, the width of the H-Sync output to the deflection system is fixed at approximately 2 μ sec.



< Flow of H. SYNC >

7. V-Sync detection (IC29: 74HC123)

To discriminate if the signal input to the H/C-Sync input terminal is composite or not, IC29 detects if the V-Sync out (pin 60) pulse of IC11 is present or absent, and transmits it to the CPU.

3-10-6. f_H/f_V detector block

A gate array (IC12, MB671469PF) is developed for f_H/f_V detection. IC12 consists of a f_H detector and a H-sync counter. The f_H detector performs measurement of successive 16H time interval using 16MHz clock generated by a quartz crystal. The H-sync counter counts H-sync in 2V time interval.

This circuit is so designed that it does not respond to sudden change in f_H caused by noises, etc. or to jitters less than 0.4%.

Also, HF.HD/VD returned from deflection system are applied to H-IN (pin ⑤)/V-IN (pin ⑥) of the IC to improve its accuracy of operation by counting pulses averaged by AFC.

The software is so designed that, based upon f_H data acquired from the IC, it ignores errors less than 1/256 in f_H or less than 3 scanning lines in f_V . This is quite agreeable level.

Based on values of f_H/f_V thus detected, following operation is done:

- * compensation to divergence of registration depending upon f_H .
- * compensation to color temperature depending upon f_H .
- * discrimination of input signal.
- * determination of number of scanning lines required in constructing a character.
- * determination of hatch spacing in vertical direction.

3-10-7. Character & Built-in Test Signal Generator Block

1. Character & Built-in Test Signal Generation (IC13, 14, 15, 16, 17)

① Gate array (IC13)

IC13 (MB605195PF) is a 120 pin, C-MOS gate array, and its input/output is of TTL level.

With an input, IC generates characters and built-in test signals in synchronous with frequency of the input signal using clock signal synchronous with "HF.HD" (pin ⑤: CKIN) and "VD" (pin ⑥: VDIN).

Without input signal, IC generates H-sync ($f_H = 34.3$ kHz), V-sync ($f_V = 65.0$ Hz), characters and test signals in synchronous with internal frequency generated by a ceramic resonator (X4).

		pin-number of IC13
Characters	Red	pin ④ (RCHA)
	Green	pin ④ (GCHA)
	Blue	pin ④ (BCHA)
	shadow area	pin ④ (BORDER)
Built-in Test Signals	cross hairs	pin ④ (INSG)
	hatch (5 * 5)	pin ④ (INSG)
	hatch (9 * 9)	pin ④ (INSG)
	hatch in reversal video (9 * 9)	pin ④ (INSG)
	dots	pin ④ (INSG)
	H pattern	pin ④ (INSG)
	white flat field signal	pin ④ (INSG)
	window	pin ④ (INSG)
	PLUGE (5IRE portion)	pin ④ (PH)
	PLUGE (- 5IRE portion)	pin ④ (PL)
	hatch + cursor	pin ④ (CBLT)
Miscellaneous	H-sync (IN)	pin ⑤ (HSIN)
	V-sync (IN)	pin ④ (VSIN)
	H-sync (OUT)	pin ③ (HS)
	V-sync (OUT)	pin ② (VS)
	presence of input signal detect	pin ⑥ (I/E)
	test mode detect	pin ④ (N/T)

(H: present, L: not present)
(H: normal mode, L: test mode)

Table 10-5

To suppress crosstalk between external signal and internal oscillation (X4), D5 is used to enable internal oscillation only when no input signal is present.

② RAM (IC14)

This is one of external memories, and is used as a Video RAM for characters. CPU writes ASCII code, location/color of display on this Video RAM via IC13.

Capacity is 2k bytes because 2 pages (the 1st page for ASCII codes, and the 2nd page for color data) of character configuration of 28 characters × 12 lines (effective area of screen is 28 characters × 12 lines, however, larger configuration said above is necessary because of dummy read during blanking interval, and of easy mapping) are required.

Real-time read operation in synchronous with input signal is performed. In 1H time, data bus is connected to CPU for a half of time required to display one character. Let the remaining half of time required to display a character further be divided in two, and access operation to 36 characters be required in reading ASCII codes and color data during 1H time including H blanking intervals. Then, minimum access time $T_{amin.}$ is calculated by following equation:

$$T_{amin.} = \left(\frac{1}{92} \text{ [kHz]} \right) / (36 \times 4) = 75 \text{ [nsec]}$$

In this projector, SONY's high-speed, C-MOS S-RAM (CXK5814P-45L) with access time of 45 nsec. is used.

③ Font ROMs (IC15, 16, 17)

111 characters in total are used, i.e., numbers, alphabets (upper-case and lower-case), general symbols, and symbols used in European TV receivers.

Dot configuration is 12×16 , and ROM capacity required is about 8k bytes because separate data are necessary for characters and border areas.

If a ROM of 8-bit type is used, time-division processing is necessary for 3 times because one character contains information of $(12 + 12)$ bits (for character and for border) in horizontal direction. Minimum access time $T_{amin.}$ is calculated by following equation, as in the case of section ② RAM. The value is too fast for general-purpose C-MOS ICs.

$$T_{amin.} = \left(\frac{1}{92} \text{ [kHz]} \right) / (36 \times 3) = 100 \text{ [nsec]}$$

To cope with this, 3 ROMs are used to permit simultaneous access to data of 24-bits. This results in 300 [nsec] of $T_{amin.}$, and permits use of low price C-MOS ROMs.

In practice, SONY's 64 kbit mask ROMs (FP28) are used. (IC15: CXK3864-040M, IC16: CXK3864-041M, IC17: CXK3864-042M)

3. PLL circuit (IC20, 21, 22, 23, 25, Q6, Q9)

① Basic configuration

Generation of characters and of built-in test signals is synchronized with input signal (HF.HD and VD, strictly speaking) using a PLL circuit. Output from phase comparator (IC20) passes a low-pass filter consisting of R170, R178, C85 and C86, then enters to a VCO (IC21). Output from the VCO enters to "CKIN" of IC13, then passes a 1/417 pre-scaler in IC13 before returning to the phase comparator.

With only one VCO, it is impossible to cope with the lock-in frequency range required. So, two VCOs (IC21 consists of two VCOs) are used, that is, one is used for high-band and the other for low-band. Switching between these two VCOs is done by a voltage comparator (IC22) and a flip-flop (IC23). For details, refer to section ② Lock range extender circuit..

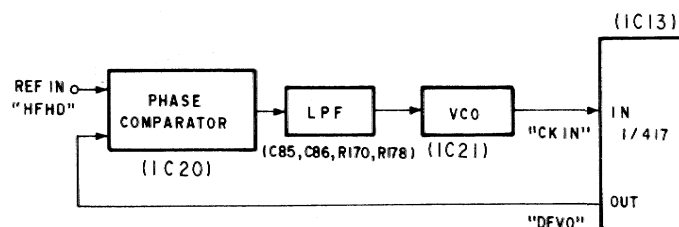


Fig.12-7 Basic block diagram of PLL circuit

(1) Phase comparator .. A high-speed digital circuit with narrow immune range is suitable.
→ IC20: CX3065A (SONY)

(2) LPF R170, C86, R178, and C85 are used.

(3) VCO One with maximum frequency more than 60MHz, and wide range of oscillating frequency is suitable → IC21: SN74S124N (TI)

② Measures against jitters/noises in SYNC

Use of HD (HF.HD) derived from deflection system in place of input SYNC gives following merits:

- * Jitters/noise components are eliminated because HD (HF.HD) derives from a section after AFC circuit. This permits easy design on time constant of low-pass filter, and contributes to extension of lock range.
- * Characters displayed do not move relative to the screen if performed RGB-SHIFT adjustment.

③ Lock range extender circuit

With only one VCO, it is impossible to cope with the lock-in frequency range required. So, two VCOs (IC21 consists of two VCOs) are used, that is, one is used for high-band and the other for low-band. Switching between these two VCOs is done by a voltage comparator (IC22) and a flip-flop (IC23).

When f_h increases starting from 15 kHz, and control voltage V_c becomes higher than about 4.5V (V_{th}), voltage comparator-1 shown in the block diagram below is enabled. A flip-flop inverts, and switching from VCO-1 to VCO-2 occurs. When f_h decreases starting from 95 kHz, and control voltage V_c becomes lower than about 2.4V (V_l), then voltage comparator-2 is enabled. Flip-flop inverts again, and switching from VCO-2 to VCO-1 occurs.

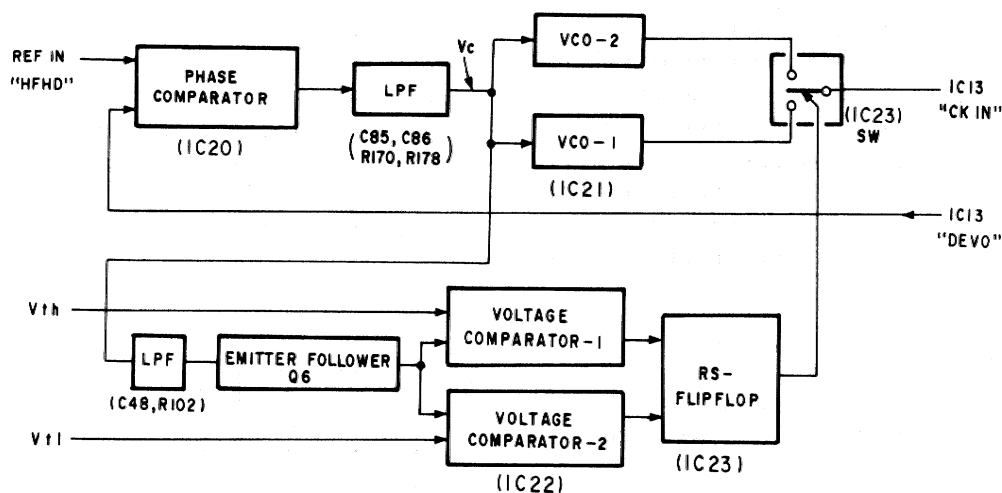


Fig 12-8. Block diagram of Automatic switching circuit of VCO

Lock-in correction waveform control described in the next section is also effective in extending lock range.

4. VD synchronizer (IC26, 27)

No restriction exists on phase relationship between HFHD and VD applied to Y board, and phase jitters by $4 \mu\text{S}$. in maximum may occur by effects from a phase-shift circuit on DA board. Consequently, a possibility exists that V-jitters of characters or built-in test signals may occur. Reason is, with phase relationship between HD and VD shown below, counting of scanning line counter (in IC13), which counts HD (this determines display position of characters or test signals such as hatch) and is cleared by VD, may fluctuate by one count.

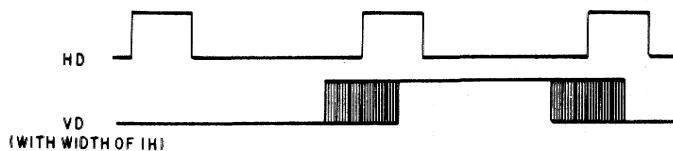


Fig 12-9.

If negative going edge of VD occurs while HD is High state, this circuit determines that HD and VD are in the timing relationship above, and delays timing of VD to be sent to IC13 by $5.4 \mu\text{S}$ than that of VD input. Also, a circuit is added which cancels delaying VD timing if the IC determines that HD and VD are still in the timing relationship said above after delay of timing has been done. Block diagram Fig 12-10. shows the circuit.

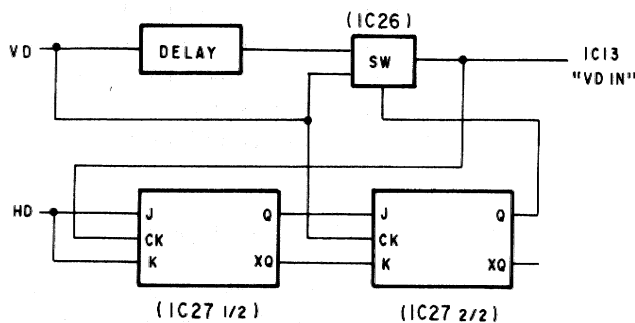


Fig 12-10.

This circuit synchronizes VD with HD, and problem of character jitter is resolved.

Value of $5.4 \mu\text{sec}$. is determined based upon the minimum (about $10.9 \mu\text{sec}$ at 92 kHz) of 1H time and the maximum ($4 \mu\text{sec}$.) of jitter width.

5. TTL-ECL convertor (IC18, 19)

Signals of INT SG, character R/G/B, and BORDER (shadow of characters) are sent to circuit boards of signal system after converted to ECL level because these are high frequency signals.

3-12-8. 96 Pin Connector Interface

pin NO.	name	description	I/O	signal	level	Active state, etc. (SIRCS code: SC)
1a	+5V SUB	power line supplied at MAIN SW ON of main unit	I	DC	+5V	MAIN SW ON
1b	+5.7V	power line supplied at POWER SW ON of commander	I	DC	+5.7V	S. C. = $2E_H$
1c	+5.7V	ditto	I	DC	+5.7V	ditto
2a	+5V SUB	power line supplied at MAIN SW ON of main unit	I	DC	+5V	MAIN SW ON
2b	POWER CONT	control signal to power supply unit	O	DC	TTL	POWER ON: Low (S. C. = $2E_H$), POWER OFF: High (S. C. = $2F_H$)
3a	FAN PROT	FAN protector ON/OFF signal (from PA board)	I	DC	TTL	FAN's abnormal state (stop): Low
3b	D GND	GND to Y board				
3c	D GND	GND to Y board				
4a	D GND	GND to Y board				
4b	Σ Ik PROT	cathode current protector ON/OFF signal (from PA)	I	DC	TTL	abnormal (excessive) cathode current: High
4c	H STOP	H def. system protector ON/OFF signal (from PA)	I	DC	TTL	H deflection stop: High
5a	LENS PROT	not used	—	—	—	
5b	HV PROT	high voltage protector ON/OFF signal (from PA)	I	DC	TTL	abnormal condition in HV system: High
5c	V STOP	V def. system protector ON/OFF signal (from PA)	I	DC	TTL	V deflection stop: High
6a	GIN 2	not used	—	—	—	
6b	BIN 1	not used	—	—	—	
6c	BIN 2	not used	—	—	—	
7a	RIN1	not used	—	—	—	
7b	RIN 2	not used	—	—	—	
7c	GIN 1	not used	—	—	—	
8a	VD	v deflection signal	I	pulse	TTL	
8b	HFHD	H deflection signal (Half HD)	I	pulse	TTL	
8c	H. S (Y, DA)	H sync signal (from Y board to DA board)	O	pulse	TTL	
9a	V INV	floor/pendant/rear discrimination (V direction)	I	DC	TTL	
9b	V INV	floor/pendant/rear discrimination (H direction)	I	DC	TTL	

Table 12-6. (1/4)

pin NO.	name	description	I/O	signal	level	Active state, etc. (SIRCS code: SC)
9c	VS (Y, DA)	V-sync signal (from Y board to DA board)	O	pulse	TTL	
10a	SIRCS	SIRCS code line (from Y board to DA board)	I	pulse	TTL	
10b	S ON G	SYNC ON GREEN (composite sync signal of ext. input)	I	pulse	TTL	
10c	HS (BB, Y)	H-sync signal (ext. input signal) (from BB to Y)	I	pulse	TTL	regardless of polarity
11a	VS (BB, Y)	Y-sync signal (ext. input signal) (from BB to Y)	I	pulse	TTL	regardless of polarity
11b	CP	Clamp pulse	O	pulse	TTL	
11c	LED \overline{WR}	LED display (L board) ON/OFF (PORT/ERROR codes, etc.)	O	pulse	TTL	during data transfer to LED: Low
12a	D5	data (5th bit)	O	pulse	TTL	data value to digital ATT (L/DB/DC boards)
12b	D6	data (6th bit)	O	pulse	TTL	ditto
12c	D7	data (7th bit)	O	pulse	TTL	ditto
13a	D2	data (2th bit)	O	pulse	TTL	ditto
13b	D3	data (3th bit)	O	pulse	TTL	ditto
13c	D4	data (4th bit)	O	pulse	TTL	ditto
14a	DATT \overline{WR}	data transfer to digital ATT (on DB board) ON/OFF	O	DC	TTL	during data output: Low others: High
14b	D0	data (0th bit)	O	pulse	TTL	data value to digital ATT (L/DB DC boards)
14c	D1	data (1th bit)	O	pulse	TTL	ditto
15a	A5	address (5th bit)	O	pulse	TTL	address value to digital ATT (L/DB/DC boards)
15b	A6	address (6th bit)	O	pulse	TTL	ditto
15c	A7	address (7th bit)	O	pulse	TTL	ditto
16a	A2	address (2nd bit)	O	pulse	TTL	ditto
16b	A3	address (3rd bit)	O	pulse	TTL	ditto
16c	A4	address (4th bit)	O	pulse	TTL	ditto
17a	HD	H-deflection signal	I	pulse	TTL	
17b	A0	address (0th bit)	O	pulse	TTL	address value to digital ATT (L/DB/DC boards)
17c	A1	address (1st bit)	O	pulse	TTL	ditto

Table 12-6. (2/4)

pin NO.	name	description	I/O	signal	level	Active state, etc. (SIRCS code: SC)
18a	D GND	GND to Y board				
18b	D GND	ditto				
18c	D GND	ditto				
19a	NC	not used				
19b	FAC (NC)	not used				
19c	CODE 3	input signal discrimination	I	DC	TTL	
20a	V. IN SEL	Select the signal connected to Video input, or not	O	DC	TTL	NOTE 1
20b	VID/OTHER	Input is Video signal, or the signal other than Video	I	DC	TTL	Video: High, Others: Low
20c	SEL 2	choose SLOT-B as Input Select, or not	O	DC	TTL	NOTE 1
21a	SLOT SEL	choose SLOT-A/B as Input Select, or not	O	DC	TTL	NOTE 1
21b	SEL 1	choose SLOT-B as Input Select, or not	O	DC	TTL	NOTE 1
21c	GBR/Y. PB. PR	control to input process circuit on HCTV signal board	O	DC	TTL	GBR: High, Y. PB. PR: Low
22a	TRI/NOT	Input signal has 3-value sync, or not (from BB)	I	DC	TTL	3-value ysync: High, 2-value sync: Low
22b	COLOR/BW	control to input process circuit on HCTV signal board	O	DC	TTL	COLOR: High, BLACK & WHITE: Low
22c	SECAM ON	forced SECAM function ON/OFF	O	DC	TTL	SECAM ON: Low (S. C. = 27H)
23a	CLEAR BLUE	CLEAR BLUE function ON/OFF	O	DC	TTL	CLEAR BLUE ON: Low (S. C. = 28H)
23b	CODE 2	B&W, NTSC-PAL, SECAM discrimination signal	I	DC	TTL	NOTE 2
23c	CODE 1	ditto	I	DC	TTL	NOTE 2
24a	VIDEO/YC	Selected Video signal = composite video, or YC?	I	DC	TTL	VIDEO: High, YC: Low
24b	DVS/NVS	2-step switching of V-SHIFT circuit's variable range	O	DC	TTL	V-SHIFT "NARROW": High, "WIDE": High
24c	ON/OFF (B)	Cut off Blue CRT, or not	O	DC	TTL	CUR OFF: Low
25a	RFB/VIDEO	Selected Video Signal = RFV signal, or VIDEO?	I	DC	TTL	RGB: High, VIDEO: Low
25b	ON/OFF (R)	Cut off Red CRT, or not	O	DC	TTL	CUT OFF: Low
25c	ON/OFF (G)	Cut off Green CRT, or not	O	DC	TTL	CUT OFF: Low
26a	RX	input from RS422 terminal	I	pulse	TTL	
26b	R \bar{X}	ditto (inverted RX)	I	pulse	TTL	

Table 12-6. (3/4)

pin NO.	name	description	I/O	signal	level	Active state, etc. (SIRCS code: SC)
26c	INT/EXT	ext. sync mode, or int. sync mode	O	DC	TTL	ext. sync mode: Low, int. sync. mode: High
27a	TX	output to RS422 terminal	O	pulse	TTL	
27b	$\overline{\text{TX}}$	ditto (inverted TX)	O	pulse	TTL	
27c	DE det	DD/DE boards are installed, or not	I	DC	TTL	DD/DE boards are installed: Low
28a	PL	gate pulse to dark portion of PLUGE signal	O	pulse	TTL	PL output: Low
28b	PH	gate pulse to bright portion of PLUGE signal	O	pulse	TTL	PH output: High
28c	NORM/TEST	TEST mode (int. TEST sig. output), or NORM mode	O	DC	TTL	TEST mode: L (S. C. = 7EH), NORM mode: H (S. C. = 7DH)
29a	SG	internal TEST signal output	O	pulse	ECL	100 IRE: High, 0 IRE: Low
29b	$\overline{\text{SG}}$	ditto (inverted SG)	O	pulse	ECL	100 IRE: Low, 0 IRE: High
29c	$\overline{\text{RCHA}}$	character display (red) output (inverted RCHA)	O	pulse	ECL	100 IRE: Low, 0 IRE: High
30a	CBRT	gate pulse output to darken screen except cursor area	O	pulse	ECL	cursor area: High (normal), others: Low
30b	$\overline{\text{CBRT}}$	ditto (inverted CBRT)	O	pulse	ECL	cursor area: Low (normal), others: High
30c	RCHA	character display (red) output	O	pulse	ECL	100 IRE: High, 0 IRE: Low
31a	BORDER	character (shadow area) output	O	pulse	ECL	character (including shadow): H, others: L
31b	$\overline{\text{BORDER}}$	ditto	O	pulse	ECL	character (including shadow): L, others: H
31c	GCHA	character display (green) output	O	pulse	ECL	100 IRE: High, 0 IRE: Low
32a	BCHA	character display (blue) output	O	pulse	ECL	100 IRE: High, 0 IRE: Low
32b	$\overline{\text{BCHA}}$	character display (blue) output	O	pulse	ECL	100 IRE: Low, 0 IRE: High
32c	$\overline{\text{GCHA}}$	character display (green) output	O	pulse	ECL	100 IRE: Low, 0 IRE: High

NOTE 1

terminal output signal	V-SEL	SLOT SELECT	SEL 1	SEL 2
CCQ	Low	High	High	High
VIDEO	High	High	High	High
SLOT-A	Low	Low	Low	High
SLOT-B	Low	Low	High	Low

NOTE 2

terminal output signal	CODE 1	CODE 2
CCQ	Low	Low
VIDEO	Low	High
SLOT-A	High	Low
SLOT-B	High	High

Table 12-6. (4/4)

3-13. CIRCUIT OPERATION OF KA BOARD

On BB board, AUDIO signal receives control to its level and enters to KA board from pin ① of connector KA-502. On KA board, AUDIO signal passes a buffer (Q502) and enters to an amplifier (IC501, μ PC1241H) which directly drives a speaker. The speaker's negative terminal is connected to $-15V$ line because this IC operates on ($-15V$) and (GND) power supply. Care must be paid

when you connect oscilloscope probes to speaker terminals because this may short-circuit between $-15V$ and GND if other GND probe of the oscilloscope is connected to GND. Q501 is series regulator transistor which prevents ripple component on power line being heard from speaker as hum noise.

3-14. CIRCUIT OPERATION OF BC BOARD

3-14-1. SIRCS signal filter circuit (IC102 to 104, Q102, 103)

SIRCS signals, sent from SIRCS receiver boards (NA, NB) on projector's main unit, enter to BC board via pin 8a and pin 8c of connector BC-1, respectively. Polarity of signals is negative. These signals pass filter circuits. Because these filter circuits are of same configuration, only description of NA board is given here.

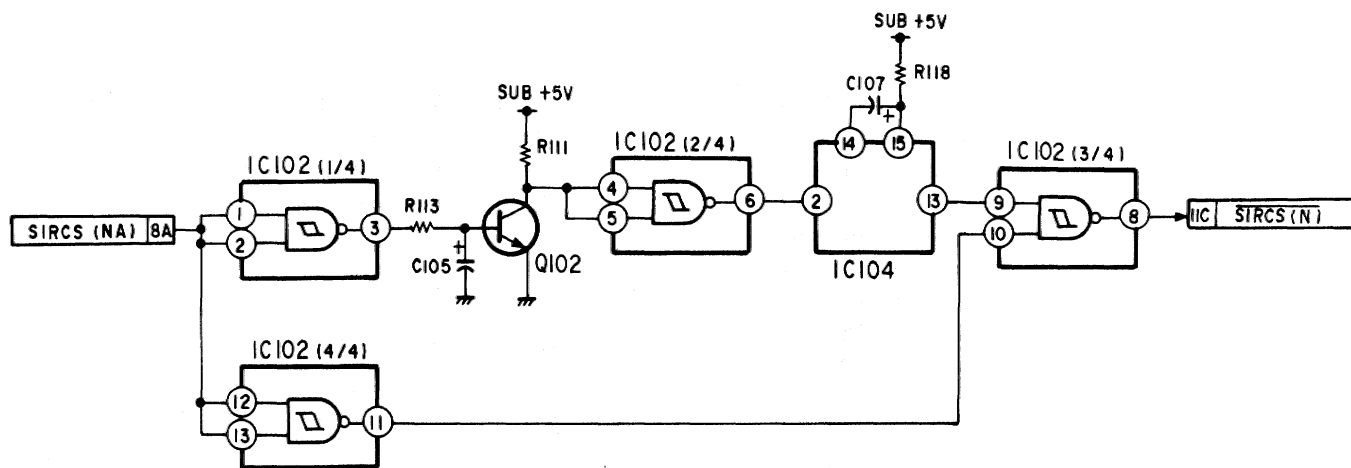


Fig. 14-1.

The filter circuit prevents input signal from being sent to BB board if noises other than SIRCS signal (e.g., noise from fluorescent lamps) are coming in.

If input signal is a SIRCS signal, it is inverted in IC102 (1/4). This starts charging to C105, and Q102 is turned ON. IC102 (2/4) inverts this again, and triggers IC104. IC104 generates positive gate pulse with width of 155 msec., and outputs it from pin ⑬. Only when output from pin ⑬ of IC104 is High, IC102 outputs SIRCS signal inverted by IC102 (4/4) from its pin ⑧.

If input signal is narrow noises other than SIRCS signal, charging to C105 does not occur and Q102 is not turned ON. So, no output appears from pin ⑧ of IC102.

After passed filters, NA and NB signals are ORed by D103 and D104, then sent to BB board.

3-14-2. SIRCS signal switching circuit (IC101, Q101)

This circuit sends SIRCS signal, which processed on INDEX board, to Y board when INDEX board is installed on SLOT A or SLOT B.

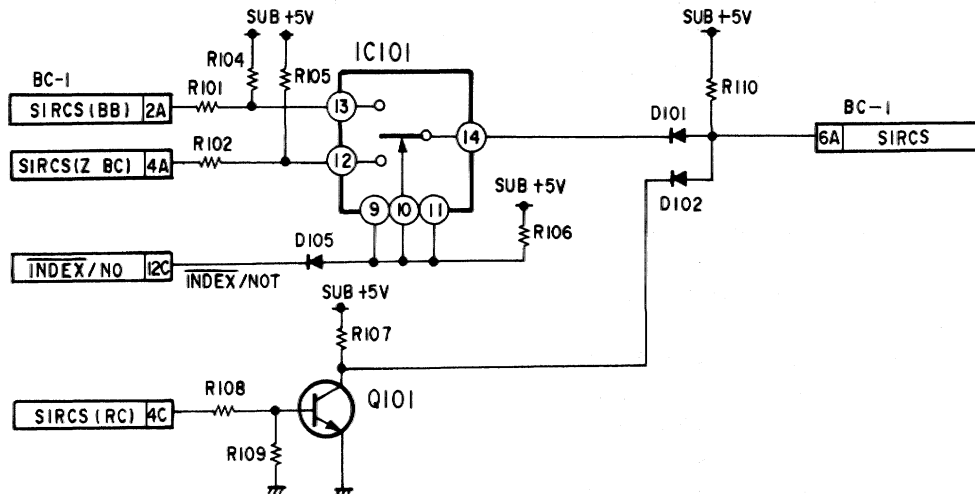


Fig. 14-2.

IC101 outputs SIRCS signal, which is processed in BB board and applied on its pin 13, from its pin 14 if pin 12c of connector BC-1 is OPEN state in normal state of operation. If INDEX board is installed, however, pin 12c is pulled down to GND. In this case, IC101 outputs the signal applied on its pin 12, that is, SIRCS signal sent from INDEX board. Also, to make control from the commander of main unit effective when INDEX board is installed, following 2 signals are ORed by D101 and D102, then sent to Y board:

- (1) signal switched by IC101
- (2) SIRCS signal from the commander of main unit (positive polarity) entered from pin 4c of connector BC-1 and inverted by Q101

3-14-3. INPUT A/B signal switching circuit (RY101 to 103, Q104, 105)

This circuit selects a signal from the one entered from SLOT A or the one entered from SLOT B.

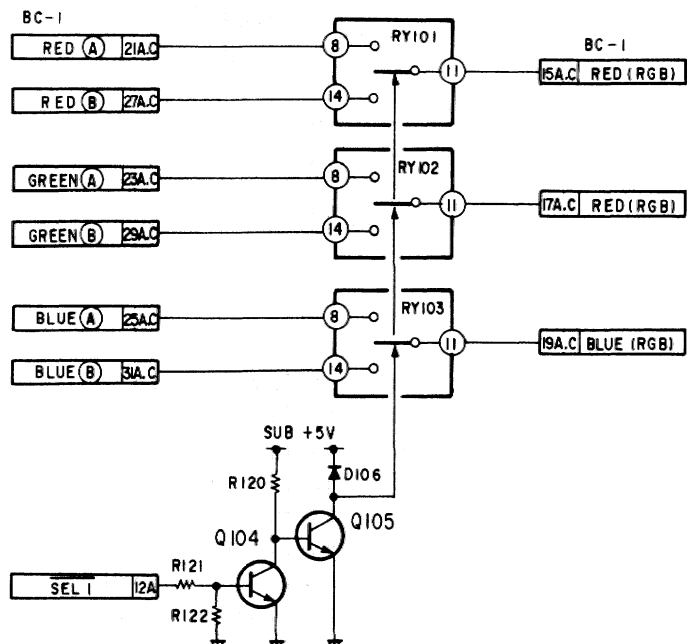


Fig. 14-3.

SEL 1 on pin 12a of connector BC-1 becomes Low when selected SLOT A, or becomes High (+5V) when selected SLOT B. Q104 and Q105 is used to convert these Low/High signals into current sufficient enough to switch RY101 to RY103.

Relays switch to pin ⑧ when INPUT A is selected, and to pin ⑭ when INPUT B is selected to send the selected signal to BB board.

3-15. CIRCUIT OPERATION OF L BOARD

3-15-1. Protector code

This projector is equipped with a self-diagnostics system for analysis of major failures. In this system, ON/OFF signal from failed section is sent to PROTECTOR circuit and CPU simultaneously. PROTECTOR circuit turns the projector OFF, and CPU outputs data corresponding to the failed section onto 8-bit data bus. Connector L-301 is the input to this 8-bit data bus.

IC301 is a buffer. IC302 and IC303 are drive circuits to drive indicator IC304. Thus, failure modes are displayed on IC304.

Mode of failure is displayed on 2-digits of 7-segment LEDs. LEDs on Y board is also turned ON when one of these failure code is displayed.

For details (i.e., failure codes, etc.), refer to 3-16. Self-Diagnostics section.

3-16. SELF-DIAGNOSTICS (TROUBLESHOOTING)

3-16-1. Self-diagnostics

This projector is equipped with a LED display on L board to permit smooth analysis of failure.

Display on LED is in hexadecimal, and Table 16-1. shows relationship between display codes and failure modes.

"01", "02", "04", "08", "10" and "20" indicate independent failure mode, respectively. Other codes are combinations of these independent failure modes.

1. Contents of failure modes

(a) "01" – FAN STOP

At least one of 6 FANs (two for power supplies) used in this projector failed: Failure may exist in FAN itself, or disconnection of a FAN connector.

NOTE:

FAN PROTECTOR does not operate at disconnection of small micro-FAN's connector.

(b) "02" – H STOP (100V down)

H deflection stops because of failure on E board or on other boards: Failure may exist in damaged Hout transistor (Q7 on E board).

Voltage building-up on +100V line is unsuccessful because of damaged transistors (Q10 or Q11) on PA board.

(c) "04" – Σ Ik OVER

Abnormal (excessive) current in CRT: The PROTECTOR is activated at about 4.3mA or more of total cathode current. Failure may exist in failed Video OUT transistors (IC101, IC201, IC301) on CARG/CAB boards, damaged CRT, damaged FBT, or too-high setting of G2 (SCREEN) potentiometer.

(d) "08" – V STOP

V deflection stops because of failure on DC board or other boards (DA or DB, for example):

Failure may exist in damaged Vout ICs (IC4, IC6, IC8) on DC board, etc.

Overload to $\pm 15V$ lines on DC board: Failure may exist in damaged Sub-deflection circuit on DC board, or in over correction to registration (*1).

* 1: If installation of the projector system is incorrect against projector's optical system, and if you perform adjustments of registration forcibly, then overload to $\pm 15V$ lines may occur.

(e) "10" – HV OVER

High-voltage (HV) becomes excessive: PROTECTOR is activated at HV = 34kV ($\pm 0.3kV$). Failure may exist damaged CRT, or damaged HV regulator circuit on PA board.

(f) "20" – POWER DOWN

POWER is turned OFF without control from the commander:

Overload to power supply may cause PROTECTOR in power supply to be activated.

NOTE:

If PROTECTOR in power supply is activated, and POWER to the projector is turned OFF, POWER CONT. line in the projector (POWER ON at High (5V), and POWER OFF at Low (0 V)) remains High state (5V). To turn POWER to the projector ON again, press Power Off key on the commander to pull down POWER CONT. line to Low (0 V) state. Then press Power ON key on the commander.

(g) Failure Display

code	FAN stop	H stop (100V down)	IK over	V stop	HV over	power down
01....	*	—	—	—	—	—
02....	—	*	—	—	—	—
03....	*	*	—	—	—	—
04....	—	—	*	—	—	—
05....	*	—	*	—	—	—
06....	—	*	*	—	—	—
07....	*	*	*	—	—	—
08....	—	—	—	*	—	—
09....	*	—	—	*	—	—
0A....	—	*	—	*	—	—
0b....	*	*	—	*	—	—
0C....	—	—	*	*	—	—
0d....	*	—	*	*	—	—
0E....	—	*	*	*	—	—
0 _....	*	*	*	*	—	—
10....	—	—	—	—	*	—
11....	*	—	—	—	*	—
12....	—	*	—	—	*	—
13....	*	*	—	—	*	—
14....	—	—	*	—	*	—
15....	*	—	*	—	*	—
16....	—	*	*	—	*	—
17....	*	*	*	—	*	—
18....	—	—	—	*	*	—
19....	*	—	—	*	*	—
1A....	—	*	—	*	*	—
1b....	*	*	—	*	*	—
1C...	—	—	*	*	*	—
1d....	*	—	*	*	*	—
1E....	—	*	*	*	*	—
1 _....	*	*	*	*	*	—
20....	—	—	—	—	—	*

Table 16-1.

2. RS422 communication error code

If errors occur in RS422 communication, display different from that of failure modes appears. Display codes and their contents are as follows:

A0: Receive time out error

Too long time interval between received Bytes:
(Transmit/Receive data of RS422 requires 3 Bytes per instruction. Error occurs if time interval between Bytes of received data is too long.)

A1: Handshake error

Discrepancy exists in timing of data transfer with MASTER side.

A2 to AF: Combination of following modes

Table 16-2. shows relationship between codes and combination modes.

Over Run Error

Next data arrives before completion of reading current data.

Parity Error

Parity (odd/even) bit error.

Framing Error

No stop bit is detected.

	Over Run Error	Parity Error	Framing Error
A2	—	—	*
A4	—	*	—
A6	—	*	*
A8	*	—	—
AA	*	—	*
AC	*	*	—
AE	*	*	*

Table 16-2.

Software for normal operation is not affected while error codes are displayed.

Error codes are turned OFF if normal communication is done next time.

3-16-2. Power ON/OFF and Protector Line

1. Power ON/OFF

Power ON/OFF control from the remote commander is done by "POWER CONT." line be pulled-up (High) or pulled-down (Low) (refer to 16-2. Power cont and prot line diagram).

Power CONT. → { High (≅ 5V) → Power ON
Low (≅ 0V) → Power OFF

When the remote commander outputs SIRCS code of "POWER ON", the code passes a signal route shown in Fig. 2-1, then enters to IC9 on Y board. The IC decodes the SIRCS code, and pulls pin ② (Power) down to Low (≅ 0V). Low state on pin ② turns Q3 ON, and "POWER CONT." line becomes High. This turns Q251 ON, and POWER to the projector is turned ON (refer to Fig. 16-2). Sequence of Power Off is the one completely reversal to that of Power On.

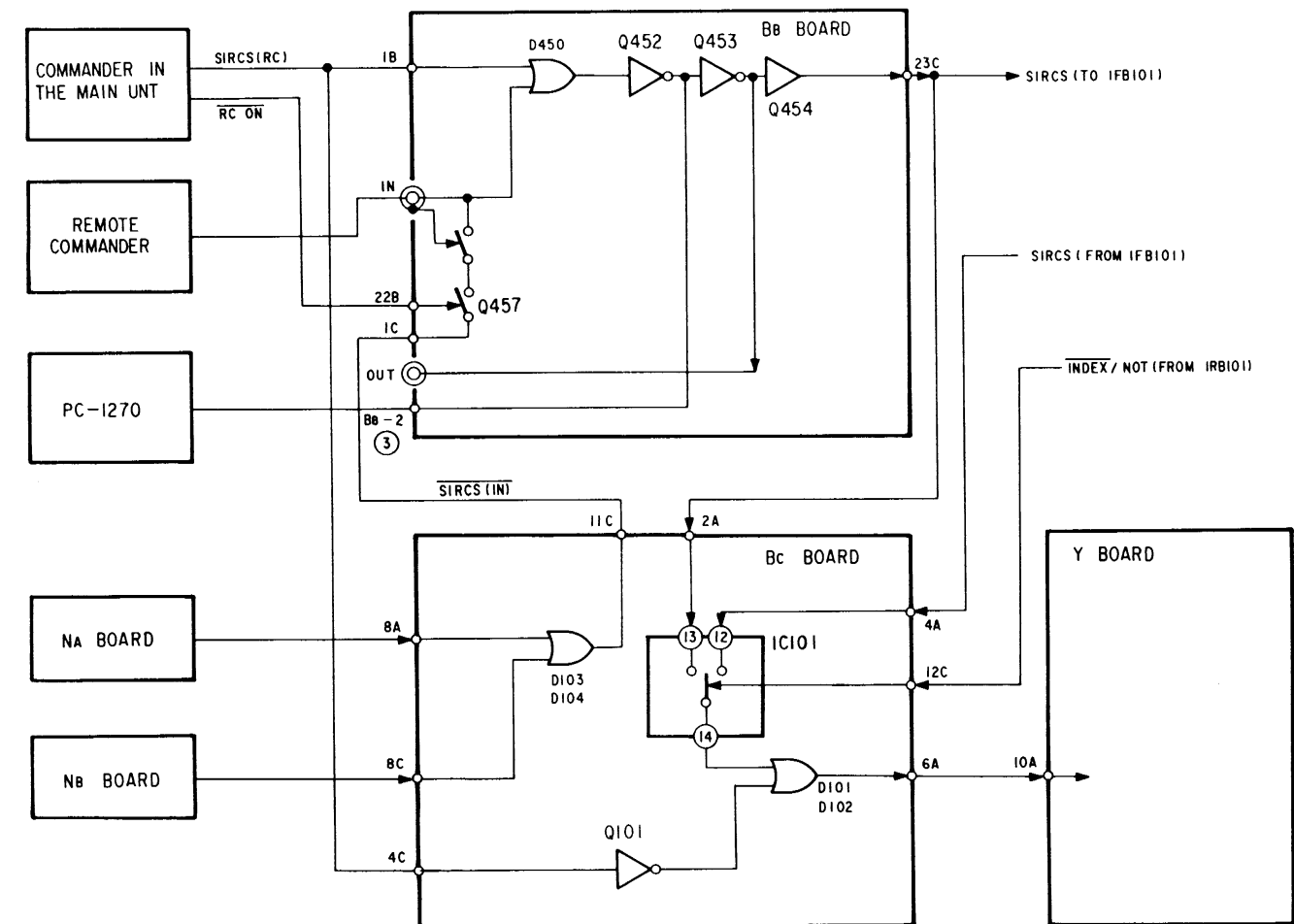


Fig. 16-1 SIRCS line diagram

In addition to control from the remote commander, Power off operation is enabled if something wrong occurs in the projector (refer to Fig. 16-2).

PA board, CA(RG) board, BA/BB boards, and IFB board contain transistors to pull down "POWER CONT." line Low forcibly. If something wrong occurs, these transistors are turned ON to pull down "POWER CONT." line, and the projector is turned OFF.

board	Ref.	function
PA board	Q15	Turns ON when protector is activated
CA(RG) board	Q2, Q4	Turn ON when voltage building-up on $\pm 12V$ power lines is unsuccessful.
BA board	Q25	
BB board	Q404, 405	
IFB board	—	

2. Protector line

There are five protector lines as shown below, and they are in 1-by-1 correspondence with failure modes:

1. FAN STOP line
2. H STOP (100V down) line
3. Σ Ik OVER line
4. V STOP line
5. HV OVER line

Signal polarity on each protector line is normally Low (\approx 0V) except FAN STOP line which is normally High (\approx 5V).

	normal state	abnormal state
1. FAN STOP	High	Low
2. H STOP (100V down)	Low	High
3. Σ Ik OVER	Low	High
4. V STOP	Low	High
5. HV OVER	Low	High

Signal levels on these lines are all entered to PA board and Y board. Signals entered to PA board are ORed (*1) to turn Q15 ON, and turns the projector OFF. Y board monitors abnormal state on signal levels, and sends data to L board to display failure modes.

* 1: Signals are ORed by D24, 25, 28 and 29 on PA board. But signal polarity on FAN STOP line is reversal to other lines. So, Q17 inverts the signal on FAN STOP line before the signal is mixed.

Here is description when H. STOP protector is activated, as an example..

If some failure occurs in E board, and H deflection stops, then Q115 on E board is turned OFF, and H. STOP line is pulled up to High (\approx 5V). Y board detects the High state on H. STOP line, and sends data to L board to display "02" on LEDs of L board. On the other hand, D24 and Q16 become High, and Q15 is turned ON. This forcibly pulls down "POWER CONT." line to Low, and the projector is turned OFF.

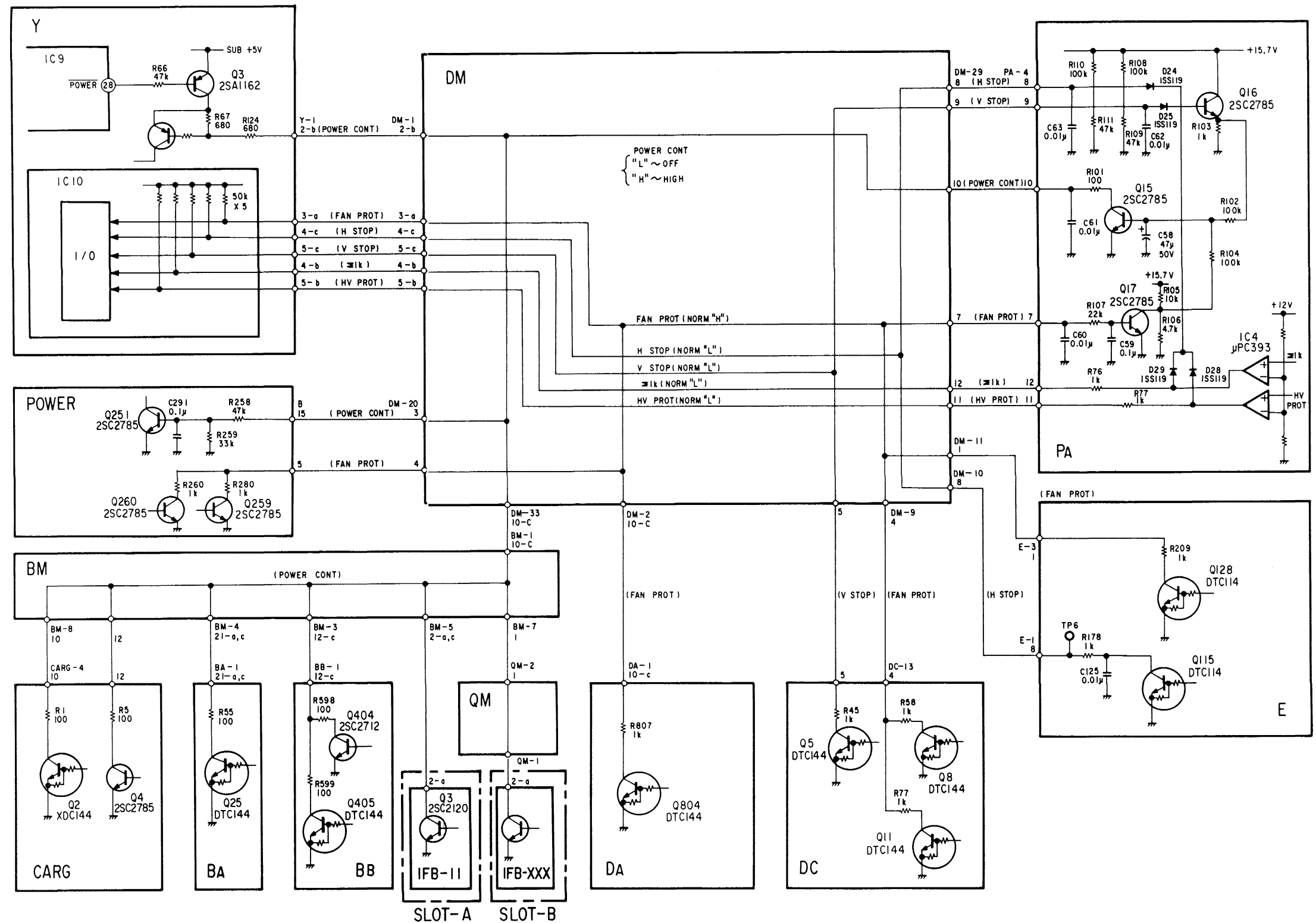


Fig. 16-2 Power cont and prot line diagram

3-17. SOPS-1036

This power supply consists of two half-bridge converters and a self-excited flyback converter (auxiliary power supply).

If the main switch is turned ON, the auxiliary power supply starts its operation first. This supplies voltage to C1 and C2 boards on M1 board, and control IC (IC51) for C1/C2 is enabled. The power supply does not operate at this moment. Power supply on M2 board starts its operation when external ON signal (about 5V) is supplied. When the power supply on M2 board starts its operation and voltage is supplied, a part of which is supplied to pin ③ of C1 board mounted on M1 board. This is ON signal, and the power supply on M1 board starts its operation.

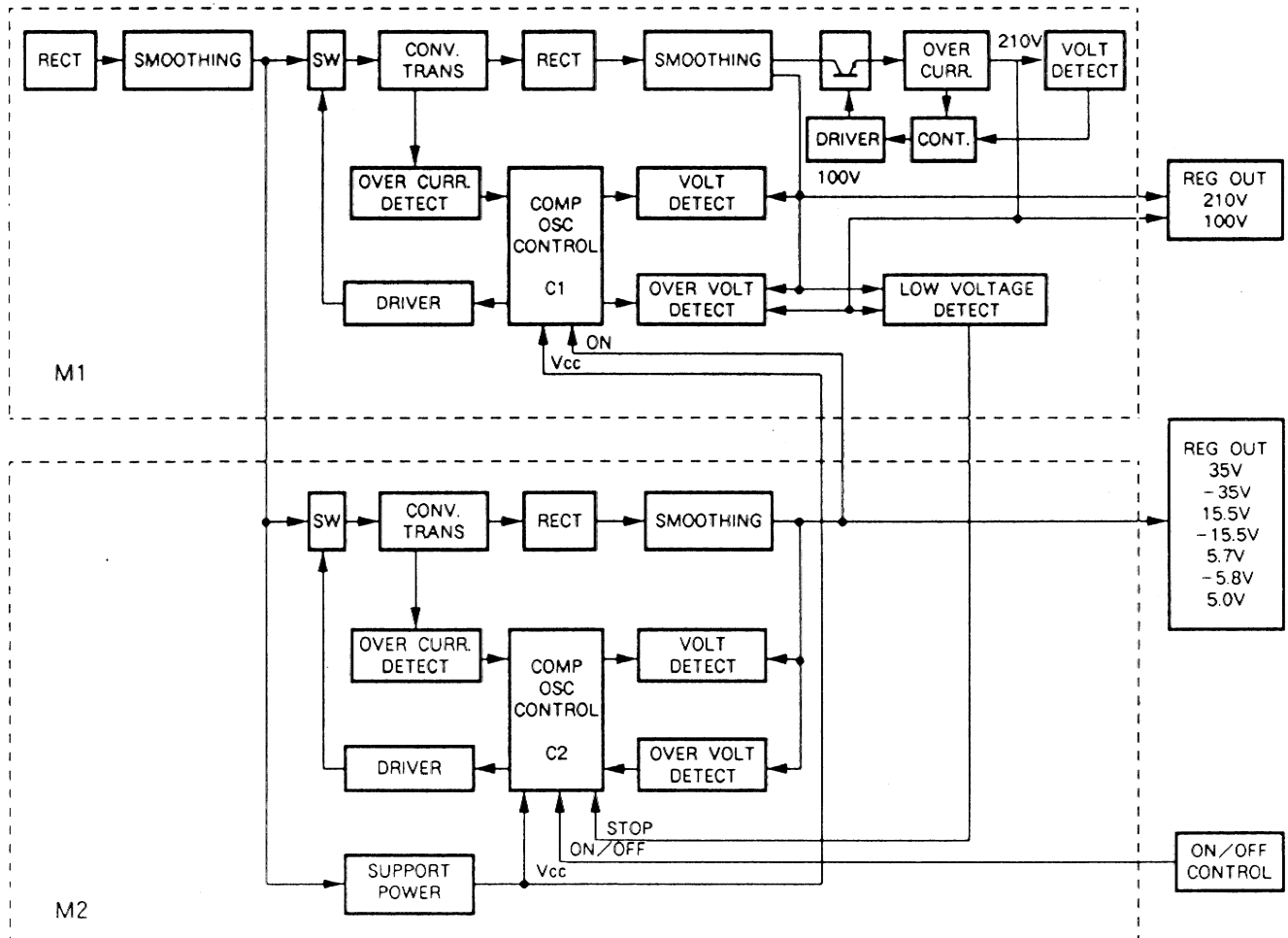


Fig. 17-1

3-17-1. C2 board (control board)

Pin ① and pin ② are input terminals of an error amplifier IC51 which controls output voltage. 5.7V output is divided by R71, R270 and RV251, then is entered to pin ① of IC51. Voltage (5V) supplied from pin ⑭ is divided by R62 and R63, then is entered to pin ②. Pin ④ is "dead-time control" terminal. If this terminal is in "High" state, then ON duty becomes zero.

If ON signal is in "Low" state (ON signal enters via Q251 and Q258), the power supply does not work because pin ④ is held in "High" state. Oscillation frequency is determined by pin ⑤ and pin ⑥. Pins ⑧, ⑨, ⑩ and ⑪ are terminals for output transistor of IC51, and drive the main transistor via T153 and T154. Pin ⑫ is input terminal. Pin ⑬ is reference voltage (5V) output terminal. Pin ⑮ and pin ⑯ are input terminals of an error amplifier for over current protection. Voltage detected by T152 is rectified by D51, 52, 53 and 54, and after filtered by L1 and C53, it enters to pin ⑰.

3-17-2. M2 board

C152, 153, 166, 167, and Q151, 152, and T152 are half-bridge converter. AC voltage output from T151 is rectified by D251, 252, 253, 254, 255 and 256, then filtered by L251, 252, 253, and C265, 266, 267, 268 and 270. D276, 277, 278, 279, and R256, 266, 261, 263 and IC252 are over-current protection circuit. If each output voltage exceeds the reference voltage, pin ① or pin ⑦ of IC252 becomes "High" state. This "High" state is entered to pin ⑨ of IC2, and causes D58 to be turned ON, and Q53 also to be turned ON. Pin ④ of IC5 becomes "High" state, and the converter stops its operation.

3-17-3. C1 board (control board)

Operation on this board is same with that on C2 board.

3-17-4. M1 board

C109, 110, 111, 112, and Q101, 102, 103, and T101 are half-bridge converter circuit. AC voltage output from T101 is rectified by D201, 202, 203, 204, 205 and 206, and filtered by C201, 202, 213, 214, 215 and 216.

Q204, 205, and R232, 233, and Q206, 207, and R234, 235, 236 are over-current protection circuit.

With 10V output, if the voltage divided by R232 and R233 exceeds 5V, Q204 is turned ON, and "High" signal is entered to pin ⑨ of C1 board. This causes D58 to be turned ON, and Q53 also to be turned ON. Pin ④ of IC51 become "High" state, and the converter stops its operation.

IC203, and R247, 248, 249, 250, 251 are low-voltage protection circuit. With 100V output, voltage divided by R247 and R248 is entered to pin ⑥ of IC203 to compare it to the reference voltage on pin ⑤. If voltage on pin ⑥ drops lower than that on pin ⑤, "High" signal is output from pin ⑦ and is entered to pin ③. C227 and R241 is a delay circuit. Pin ① outputs "High" signal. This passes M2 board, and is applied to pin ⑨ of C2 board, then the converter stops its operation.

R201, IC201, R217, 218, and RV202 are series voltage regulator.

R208, 209, 210, 212, 213, 214, 215, 254, and RV201 are over-current protection circuit.