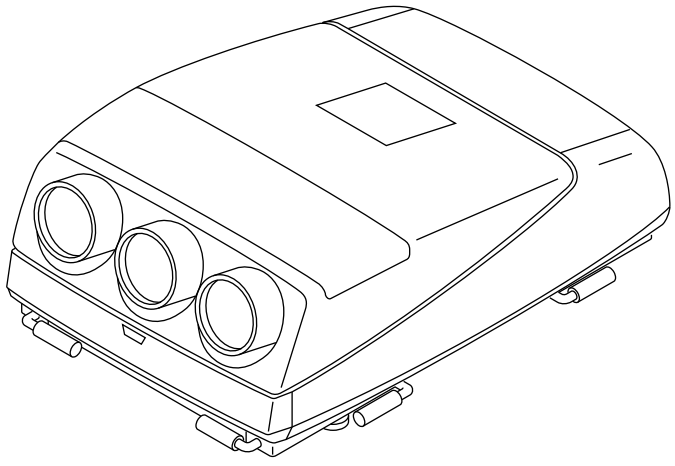
THEORY OF OPERATION

MODEL	DEST.	CHASSIS NO.
VPH-G90U	US/CND	SCC-K81D-A
VPH-G90E	AEP	SCC-K82E-A
VPH-G90M	E	SCC-N96A-A



MULTISCAN PROJECTOR

SONY

⚠WARNING

This manual is intended for qualified service personnel only.

To reduce the risk of electric shock, fire or injury, do not perform any servicing other than that contained in the operating instructions unless you are qualified to do so. Refer all servicing to qualified service personnel.

WARNING!!

AN ISOLATION TRANSFORMER SHOULD BE USED DURING ANY SERVICE TO AVOID POSSIBLE SHOCK HAZARD, BECAUSE OF LIVE CHASSIS.

THE CHASSIS OF THIS RECEIVER IS DIRECTLY CONNECTED TO THE AC POWER LINE.

SAFETY-RELATED COMPONENT WARNING!!

COMPONENTS IDENTIFIED BY MARK ⚠ ON THE SCHEMATIC DIAGRAMS, EXPLODED VIEWS AND IN THE PARTS LIST ARE CRITICAL TO SAFE OPERATION. REPLACE THESE COMPONENTS WITH SONY PARTS WHOSE PART NUMBERS APPEAR AS SHOWN IN THIS MANUAL OR IN SUPPLEMENTS PUBLISHED BY SONY. CIRCUIT ADJUSTMENTS THAT ARE CRITICAL TO SAFE OPERATION ARE IDENTIFIED IN THIS MANUAL. FOLLOW THESE PROCEDURES WHENEVER CRITICAL COMPONENTS ARE REPLACED OR IMPROPER OPERATION IS SUSPECTED.

ATTENTION!!

AFIN D'EVITER TOUT RISQUE D'ELECTROCUTION PROVENANT D'UN CHÁSSIS SOUS TENSION, UN TRANSFORMATEUR D'ISOLEMENT DOIT ETRE UTILISÉ LORS DE TOUT DÉPANNAGE.

LE CHÁSSIS DE CE RÉCEPTEUR EST DIRECTEMENT RACCORDÉ À L'ALIMENTATION SECTEUR.

ATTENTION AUX COMPOSANTS RELATIFS À LA SÉCURITÉ!!

LES COMPOSANTS IDENTIFIÈS PAR UNE TRAME ET PAR UNE MARPUE ⚠ SUR LES SCHÉMAS DE PRINCIPE, LES VUES EXPLOSÉES ET LES LISTES DE PIECES CONT D'UNE IMPORTANCE CRITIQUE PUR LA SÉCURITÉ DU FONCTIONNEMENT. NE LES REMPLACER QUE PAR DES COMPOSANTS SONY DONT LE NUMÉRO DE PIÉCE EST INDIQUÉ DANS LE PRÉSENT MANUEL OU DANS DES SUPPLÉMENTS PUBLIÉS PAR SONY. LES RÉGLAGES DE CIRCUIT DONT L'IMPORTANCE EST CRITIQUE POUR LA SÉCURITÉ DU FONCTIONNEMENT SONT IDENTIFIES DANS LE PRÉSENT MANUEL. SUIVRE CES PROCÉDURES LORS DE CHAQUE REMPLACEMENT DE COMPOSANTS CRITIQUES, OU LORSQU'UN MAUVAIS FONCTIONNEMENT EST SUSPECTÉ.

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SECTION 1
BA BOARD

This board mainly performs the video processing of VIDEO (C-VIDEO, Y/C, component) signals and HDTV (GBR, Y PB PR) signals, and sync processing.

1-1. INPUT SIGNAL SELECTOR

There are the following four input:
- INPUT A : R, G, B, SYNC/HD, VD (BA board)
- VIDEO : VIDEO, Y, C, S (BD board)
- INPUT B : SLOT
- INPUT C : SLOT

Selection of INPUT A or INPUT B/C is performed by IC1, IC2, and IC3 (MAX 4121CSA). The video signal is input from the BD board to the BA board, then the R, G, and B signals are input to IC202, IC207, and IC213 respectively. If the signals other than the R/G/B signals are input to INPUT A or INPUT B/C (SLOT), they are output from IC200, IC206, and IC212, then they are processed as R, G, and B inside the BA board. The processed signals are supplied to the aforementioned IC202, IC207, and IC213. Almost all the internal adjustment signals are input to IC404 as an OSD signal. However, the analog signals for the white balance adjustment, such as 10-step and white signals of vertical rate, are input to IC220 (µPC814G2), their pedestal levels are clamped by IC219 (TC7S66F), IC218 (TC4W53F), and IC221 (TC7S32F), pass through the buffers, then make a selection with the external signals by IC203, IC208, and IC214 (MAX4121CSA).

1-2. SHADING AND GAMMA CORRECTIONS

1-2-1. Right and Left Shading Correction (Color Uniformity)

The R, G, and B CRTs are set in a row. The G CRT is located in the center. The remaining R and B CRTs are located in both sides, and their centers are inclined and oriented toward the center of screen. Consequently, in order to prevent the difference in brightness on the right and left between Red and Blue, multiply the signal waveforms by a saw-tooth waveforms which are generated from the DD board. Phase difference of the saw-tooth waveforms for R and B are 180 degrees.

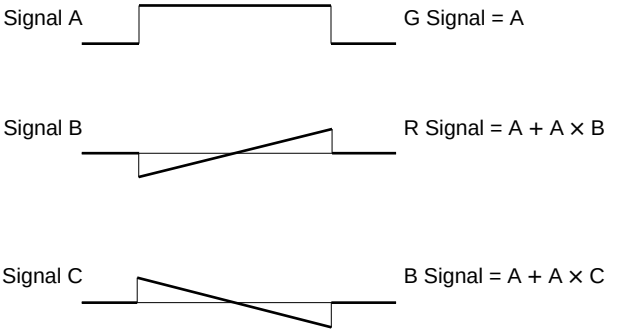


Fig. 1-1

INPUT \ IC REF/PIN NO.		IC1		IC2		IC3		IC200	IC206	IC212	IC202		IC207		IC213		IC203		IC208		IC214	
		①	⑧	①	⑧	①	⑧	⑤	⑤	⑤	①	⑧	①	⑧	①	⑧	①	⑧	①	⑧	①	⑧
INPUT A (SLOT)	RGB	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	L	H	L	H
	Y/R-Y/B-Y	H	H	H	H	H	H	H	H	H	L	H	L	H	L	H	L	H	L	H	L	H
	HDTV-Y/PB/PR	H	H	H	H	H	H	H	H	H	L	H	L	H	L	H	L	H	L	H	L	H
	HDTV-GBR	H	H	H	H	H	H	H	H	H	L	H	L	H	L	H	L	H	L	H	L	H
INPUT B INPUT C (SLOT)	RGB	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	L	H	L	H
	Y/R-Y/B-Y	L	H	L	H	L	H	H	H	H	L	H	L	H	L	H	L	H	L	H	L	H
	HDTV-Y/PB/PR	L	H	L	H	L	H	H	H	H	L	H	L	H	L	H	L	H	L	H	L	H
	HDTV-GBR	L	H	L	H	L	H	H	H	H	L	H	L	H	L	H	L	H	L	H	L	H
	VIDEO	L	H	L	H	L	H	L	L	L	L	H	L	H	L	H	L	H	L	H	L	H
	YC	L	H	L	H	L	H	L	H	H	L	H	L	H	L	H	L	H	L	H	L	H
VIDEO System Terminal	–	L	L	L	L	L	L	L	L	L	L	H	L	H	L	H	L	H	L	H	L	H
W/B TEST SIG	–	–	–	–	–	–	–	–	–	–	–	L	–	L	–	L	H	H	H	H	H	H

Table. 1-1

1-2-2. Hot Spot Correction (Brightness Uniformity)

According to characteristics of projection lens, the center of screen becomes brighter and corners of screen become darker. In order to compensate the above characteristics, multiply a parabolic waveform by the signal.

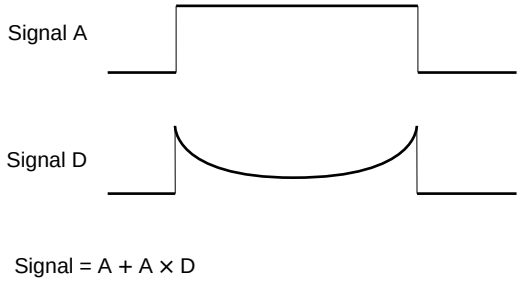


Fig. 1-2

1-2-3. Gamma Correction Circuit

This circuit is composed of IC402. IC402 amplify the signal in the vicinity of 50 IRE according to the input signal amplitude in order to eliminate the difference of gamma characteristics of R, G, and B CRTs.
Gamma correction is controlled by the microcomputer. In Expert and Factory modes, gamma characteristic can be changed by customizing the setting of color temperature.

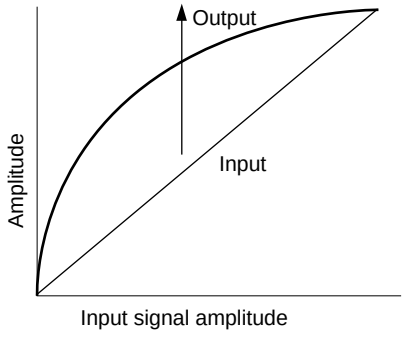


Fig. 1-3

1-3. OSD MIXER/BUFFER CIRCUIT

1-3-1. Pre-amplifier/OSD Mixer (IC404 : LM1283)

IC404 works as a mixer of OSD and video signal, and pre-amplifier. IC404 performs R/G/B drive control, contrast control, and OSD's each color drive control. Selection of OSD and video is performed by the following timing.

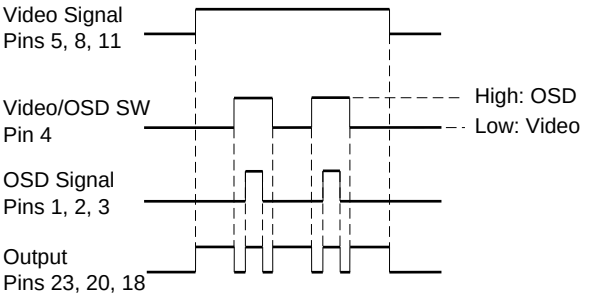


Fig. 1-4

1-3-2. Brightness/Bias Control

An ABG pulse and blanking voltage are determined by the BKG voltage. By adding the ABG pulse and blanking voltage to the video signal, and clamping the blanking voltage, the pedestal level changes, then the brightness can be changed by the BRIGHT and BIAS.
IC600, IC601, and IC602 generate the BKG potential of R, G, and B. In RED, for example, BRIGHT and BIAS control signals output from D/A converters (IC609/IC611 : MP7670) are input to IC600. A calculation result is converted to voltage with IC603 (2/2), and apply to the CA board from pins A24 of CN340.

1-4. ABL/IK PROTECTOR

There are two ABL, Single ABL and Total ABL.

1-4-1. Single ABL

The R/G/B cathode currents (Ik) are detected by the CD board. The detected Iks are pass through the buffers (IC807/IC808/IC809) and amplifiers (IC802 (2/2)/IC805), then they are input to the comparators (Q808/Q816/Q817). If the comparator input voltage is greater than the reference voltage, the comparator transistor turns to ON state, and the Single ABL works.

1-4-2. Total ABL

The sum of each Ik (R/G/B) detected by the PA board is input to comparator (Q814). The total ABL works if the comparator input voltage is greater than the reference voltage at the base of Q813.

The level of both Single ABL and Total ABL will be changed in accordance with the screen size to protect the burning of the CRT. The picture size information is output from the D/A converter (IC2001 : CXA1875AM), and it is input to an amplifier IC803 (TL082CPS (1/2). As a result, base voltages of Q813 and Q817/Q808/Q816 are controlled to apply optimum ABL correction according to the picture size.

1-4-3. Ik Protector

There are the two Ik protectors, and one out of two is processed by the BA board.
The maximum value of each Ik (R/G/B) is detected by Q809/Q810/Q811/Q812. The detected maximum value is compared with the reference value by IC804 (1/2) (µPC393G2). If the detected maximum value is greater than the reference value, Ik protection line goes “High” level to apply protection.

1-5. D/A CONVERTER BLOCK

The D/A converter IC609/IC611 (MP7670) output the contrast and brightness control signals, R/G/B drive bias signals, and limit control signal.

1-6. SYNC BLOCK

The H sync, C sync, and V sync signals input to SYNC/HD and VD connectors on the rear connector panel, are input to Q1/Q3/IC4 (TL082CPS) and Q4/Q6/IC4 (TL082CPS) where they are averaging. The averaged DC value and sync waveform are input to differential line receiver (IC12), they are converted to a TTL signal, then output to the next stage.
When inputting a special sync signal, such as tele-text or PAL-DVD, to the SYNC/HD BNC connector on the rear connector panel, C sync signal is output from IC11 (GS4981-CTA) only when the R/G/B signals are input to INPUT A. The horizontal frequency (fH) of regular video signal through high-vision signal (Tri-sync) can be used, and the optimum sync route is automatically discriminating (Auto). It is possible to change the sync route forcibly (Sync with Video).

1-7. MONITOR OUTPUT BLOCK

IC5, IC8, and IC10 (MAX4223ESA) form a buffer amplifier for the monitor output. By connecting the IFB-12, the signals input to INPUT A can be monitored from the IFB-12. (Only when the slide switch inside the IFB-12 is set to “OUT” position, the selection signal is output from the IFB-12, then the input/output of the signals are switched by relays RY1/RY2/RY3.)

1-8. ±12 V, ±5 V, +9 V

If the voltage of ± 12 V, ± 5 V or + 9 V drops for some reason, the protector works and the power is turned to OFF. The IC2110 (MAX8213) is a protector, and an operating point of protection can be manually set.
The output of IC2110 is open drain. During normal operation, the output of IC2110 is kept in “High” level. If abnormality is detected, it is turned to “Low” level. The output of IC2110 is inverted by Q2100, and is supplied to the Y board. The Y board monitors all protector operations.

1-9. FUNCTIONS OF MAIN ICS

1. CXD2024 (IC1003) : Digital comb filter

IC1003 performs NTSC (3.58 MHz) and PAL 2 dimensional processing by the digital Y/C separation method.
(Normally, only the PAL system is used, but if the comb filter is set to 3 lines at the MENU screen, Y/C separation is also performed for the NTSC (3.58 MHz) system.)
The clock (fsc) output from Pin 23 of IC1402 (TDA9141) is multiplied by 4 times (4 fsc) by IC1004 (NJM2240M) and input to Pin 11 as the operation clock. The video signal input to Pin 25 by this clock is digitally processed, after which the Y signal is output from Pin 31, and the C signal is output from Pin 39.

2. μPD64081 (IC1203) : 3 dimensional comb filter

IC1203 performs 3 dimensional processing for the NTSC (3.58 MHz) system by the digital Y/C separation method. A crystal oscillator for the reference clock is connected between Pins 30 and 31 of IC1203 and this oscillator is used to generate Fsc. This Fsc is then output from the Pin 47 FSCO terminal and input to the Pin 50 FSCI terminal via the buffer. As the Y-ADC circuit in the IC1203 cannot be used, the 8-bit video signal A/D converted by the external A/D converter (μPC659AGS : IC1206) is input from Pin 74 to Pin 67, while the Y signal is output from Pin 84, and the C signal is output from Pin 83.

3. TDA9141 (IC1402) : Chroma Decoder & Sync Processing

IC1402 is controlled by the I²C bus and is used for chroma decoder/sync processing. In this IC, the C-VIDEO signal and Y/C signal can be processed. The C-VIDEO/Y signal is input to Pin 26 and the C signal is input to Pin 25 to automatically differentiate NTSC3.58/NTSC4.43/PAL/PAL-M/SECAM/B&W.
When the input signal is differentiated as the PAL system, a clock is input to IC1003 (CXD2024), and Y/C separation is performed by IC1003. When the input signal is differentiated as the NTSC (3.58 MHz) system, Y/C separation is performed by IC1203 (μPD64081). When the input signal is other than the PAL system or the NTSC (3.58 MHz) system, Y/C separation will be performed by IC1402. The Y/C separated signal is converted to the following Y/U/V signals, and output from Pins 1 (V) and 2 (U).
When the input signal is the PAL or SECAM system, it is 1H delayed by IC201, returned to Pins 3 (U) and 4 (V), processed, and output from Pins 12 (Y), 13 (V), and (14) (U).
The C-VIDEO/Y signal input to Pin 26 is separated to the H sync and V sync, and the H sync is output from Pin 17 while the V sync is output from Pin 11.

4. CXA2101Q (IC1600) : Y/R-Y/B-Y→RGB Controller

The various video parameters are controlled by the I²C bus. User control (COLOR, HUE, SHARPNESS, DYNAMIC PICTURE ON/OFF, SETUP 0/7.5 %) is controlled internally by IC1600. Functions of the IC1600 include setting the detection axis and improving the chroma transient It also converts signals to the RGB signals and outputs them.
This IC1600 incorporates a sync separation circuit and sync automatic differentiation circuit, and it performs HDTV tri-state SYNC sync processing.
The Y/R-Y/B-Y signals converted from the VIDEO and Y/C signals are input to Pins 69 (Y), 68 (B-Y), and 67 (R-Y). The Y/R-Y/B-Y signals of the component input are input to Pins 5 (Y), 4 (B-Y), and 3 (R-Y). The G/B/R signals of the GBR input are input to Pins 17 (G), 16 (B), and 15 (R). The Y/Pb/Pr signals of the HDTV (YPbPr) input are input to Pins 11 (Y), 10 (Pb), and 9 (Pr). The 2Y/2R-R/2B-Y DRC processed by the BB board are input Pins 23 (2Y), 22 (2B-Y), and 21 (2R-Y). The signal selected is subjected to various control processings, converted to the R, G, and B signals, and output from Pins 35 (R), 37 (G), and 39 (B). The SYNC signal is input to Pins 66 (HS) and 65 (VS) for VIDEO and Y/C, input to Pins 1 (HS) and 2 (VS) for component, input to Pins 13 (HS) and 14 (VS) for HDTV (GBR), input to Pins 7 (HS) and 8 (VS) for HDTV (YPbPr), and input to Pins 19 (HS) and 20 (VS) for DRC ON. The SYNC signal corresponding to the input signal selected is output from Pins 29 (HS) and 28 (VS). If the HS and VS signals are not input during HDTV, the sync separated HS and VS signals will be output from S ON G and S ON Y.

5. CXA2119 (IC1712), DRC Interface

IC1712 performs selection of the color difference signal sent to the BB board (DRC processing) and matrixes the RGB signals to the color difference signal during 15 kRGB.

Signals are input to Pins 1 (Y), 2 (B-Y), and 3 (R-Y) for VIDEO and Y/C, to Pins 5 (Y), 6 (B-Y), and 7 (R-Y) for component, and to Pins 9 (R), 10 (G), and 11 (B) for 15 kRGB, matrixed to the respective color difference signal. The signal selected is then output from Pins 16 (Y), 17 (B-Y), and 18 (R-Y).

When converting from the RGB signal to color difference signal, the signal is input from Pin 10 (SSCP output) of the TDA9141 (IC1402) to Pin 8 as the clamp pulse used for the matrix circuit.

6. PCF8574 (IC2000, 2002, 2004) I/O Port

The I/O port (IC2000, IC2002, and IC2004) is controlled by the I²C bus, and outputs the “High/Low” signal to control the various ICs.

7. CXA1875 (IC2001, 2003, 2005), DAC/SW

DAC/SW

IC2001, IC2003, and IC2005 are controlled by the I²C bus, and outputs the High/Low signal for controlling the various ICs and signals used for DC volume (0 to 5 V).

1-10. PATH OF VIDEO SIGNAL

1. Path of Video Signal

The video signal and Y/C signal from the exclusive video board (BC board) are input to Pins 5, 1, and 3 of CN351, and input to Pins 43, 45, and 47 of IC1002. The video signal and Y/C signal from INPUT-B are input to Pins 25 (VIDEO), 27 (Y), and 29 (C) of CN341, and input to Pins 2 of IC1, IC2, and IC3. The input signal is switched to INPUT-A, output from Pin 6, input to Pins 1, 3, and 5 of IC1002, and one of these signals is selected.

When the Y/C input is selected, the Y signal and C signal are output from Pins 37 (Y) and 39 (C) respectively.

When the video input is selected, the video signal is output from Pin 34, and input to Pin 1 of IC1001 (NJM2235M) via Q1004.

When other than the PAL system and NTSC (3.58 MHz) system, Pin 7 of IC1001 (NJM2235M) outputs the signal input to Pin 1 of IC1001.

For the PAL system, the video signal is input to Pin 25 of IC1003 (Comb Filter) via the 7 MHz LPF (FL1001), Y/C separated, and output from Pins 31 (Y) and 39 (C) of IC1003.

The Y signal and chroma signal output are passed through the 7 MHz low pass filter FL 1002 and FL1003, after which the Y signal is input to Pin 3 of IC1005 and the chroma signal (c) is input to Pin 3 of IC1006.

For the NTSC (3.58 MHz) system, the video signal is output from Pin 23 of IC1002 and input to Pin 4 of IC1206 (A/D converter) via the 7 MHz low pass filter (FL1201).

The A/D converted signal is input to IC1203 (3 dimensional comb filter), Y/C separated, after which the Y signal is output from Pin 84 of IC1203 and the chroma signal is output from pin 83. The Y and chroma signals are passed through the 7 MHz low pass filter FL1203 and FL1204, after which the Y signal is input to Pin 1 of IC1005 and the chroma signal is input to Pin 1 of IC1006.

The PAL system and NTSC (3.58 MHz) system Y signal and chroma signal are switched by IC1005 and IC1006 and output from Pin 7. As misoperation preventive measures for black and white signals, IC1006 (CHROMA SW) selects the Pin 5 (No Input) side. The Y signal and chroma signal output from Pin 7 are input to Pins 31 and 29 of IC1002, after which the Y signal is output from Pin 37 and the chroma signal is output from Pin 39.

The Y signal is input to Pin 26 of IC1402 via IC1001, and the chroma signal is input to Pin 25 of IC1402.

The video signal or Y/C signal input to IC1402 is converted to the Y.U.V signal, after which the Y signal is

output from Pin 12, the R-Y signal is output from Pin 13, and the B-Y signal is output from Pin 14. The Y signal is input to the SECAM trap circuit. If the input signal is the SECAM/PAL-M/NTSC 4.43 signal, Q1417 turns ON, the 4.25 MHz components are eliminated, and the cross color components are suppressed. On the other hand, the R-Y signal and B-Y signal are both phase inverted by IC1414 (μPC814) and attenuated. The Y signal is then input to Pins 67, 68, and 69 of IC600 directly. As for the video signal processed by IC1600, the R signal is output from Pin 35, the G signal is output from Pin 37, and the B signal is output from Pin 39. The normal video output level is about 0.7 V p-p, but to prevent excessive output of signals, Q1609, Q1610, and Q1611 limit the level to about 0.9 V, after which the signals are input to IC202, IC207, and IC213 composing the RGB and video switchers.

2. Path of Component (Y/R-Y/B-Y), HDTV (GBR, Y PB PR) Signals

The video signals input from INPUT-A or INPUT-B are selected by IC1, IC2, IC3, IC200, IC206, and IC212, and supplied to the buffer Q1604 (Y/G/Y), Q1603 (R-Y/R/PR), and Q1602 (B-YB-Y/B/PB). The buffer output is input to Pin 5, 3, 4, 17, 16, and 15 and Pins 11, 10, and 9 of IC1600 (CXA21011Q), after which various operations are performed to convert the signals to R, G, and B signals.

1-11. PATH OF SYNC PROCESSING

1. When the video signal is selected

The signal output from Pin 7 of IC1001 is extracted the macro vision signal in the vertical period by Q1425, and input as the video signal to Pin 26 (Video/Y) of IC1402 (TDA9141). The input signal is sync separated, and the H sync signal is output from Pin 17 while the V sync signal is output from Pin 11. The H sync and V sync signals are supplied to IC1600 (CXA2101) and IC1811 (SN74HC157ANS), the H sync signal is output from Pin 12C of CN340, the sync on green from Pin 13B, and the V sync signal from Pin 12A.

2. When the component signal is selected

The Y signal input to INPUT-A or INPUT-B is selected by IC2/IC206, passed through the buffer Q1604, passed through the amplifier composed Q1808, Q1809, and Q1813, passed through the clamp circuit composed of Q1806, Q1811, Q1812, and Q1807, and input to Pin 7 of the sync separation circuit (IC1801 : CXA2016). The HS signal will be output from Pin 18 of IC1801. The output signal is passed through the H/V mix circuit composed of IC1806 and IC1814, input to Pin 5 of IC1001 (NJM2235M), selected, and output from Pin 7. The output signal is processed in the same way as the video signal. For component signals, the H/V mixing operations will not be performed.

3. When the HDTV (GBR, Y.PB.PR) signal is selected

When the HDTV signal is selected, the video signal input to Pins 17 (G) and 11 (Y) of IC1600 is sync separated. If the external sync signal is input, IC1802 switches between INPUT-A and INPUT-B, the CS/HS signal is output from Pin 3 and is input to Pins 7 and 13 of IC1600, while the VS signal is output from Pin 7, and is input to Pins 8 and 14. As the sync separation from the external sync signal has priority, if no external sync signal is input, the sync signal is sync separated from the video signal, the HS signal is output from Pin 29 while the VS signal is output from Pin 28. Hereafter, the same operations as the video signal will be performed.

4. When the RGB signal is selected

The HS/CS signal input to TB1 (5BNC terminal : INPUT-A) is selected from the normal sync separation circuit composed of Q1, Q2, Q3, IC4, and IC12, or the sync chip clamp sync separation circuit for the CENELEC signal and tri-state sync. The signal selected is input to Pin 3 of IC1802 via the buffer (Q12/Q13), it is then selected again with the HS/CS signal supplied to Pin 2 from INPUT-B and INPUT-C, and output from Pin 4. The selected output is input to Pin 13 of IC1811, switched to the synchronization of the video system, output from Pin 12, and output to Pin 12C of CN340.

The VS signal input to TB1 (5BNC terminal : INPUT-A) is sync separated in the normal sync separation circuit composed of Q4, Q5, Q6, IC4 and IC12, input to Pin 6 of IC1802, selected with the VS signal input from INPUT-B and INPUT-C to Pin 5, and output from Pin 7. The signal selected is input to Pin 10 of IC1811, switched to the synchronization of the video system, output from Pin 9, and output from Pin 12A of CN340.

The sync separation of the video signal is input to Pin 7 of IC1801 via the same circuit as the component signal, sync separated, and output from Pin 19. The output signal is then input to Pin 3 of IC1811, switched with the synchronization of the video system, output from Pin 4, and output from Pin 13B of CN340.

1-12. PROCESSING PATH AT DRC ON

The following describes the path of the signal when DRC is ON.

1. Video signal processing path (See Fig. A)

When the video signal and Y/C signal are input, the Y, R-Y, B-Y signals from Pins 12, 13, and 14 of IC1402 are output. The R-Y signal and B-Y signal are inverted by IC1414, level-adjusted, and input to Pins 1, 3, and 2 of IC1712.

When the component signal is input, the signal is passed through the buffer composed of Q1604, Q1603, and Q1602, and input to Pins 5, 7, and 6 of IC1712. In the same way, when 15 kRGB is input, the signal is passed through the buffer composed of Q1604, Q1603, and Q1602, input to Pins 9, 10, and 11 of IC1712, and matrixed with the Y, R-Y, and B-Y signals inside IC1712. The Y, R-Y, and B-Y signal generated are switched, and output from Pins 16, 18, and 17 of IC1712, sent to Pins 30, 26, and 28 of CN346, and supplied to the BB board.

Of the video signal DRC processed in the BB board, the Y signal is input to Pin 13 of CN346, the R-Y signal is input to Pin 9, and the B-Y signal is input to Pin 11. These signals are then sent to Pins 23, 21, and 22 of IC1600, subjected to various video signal processes, and converted to the R, G, and B signals.

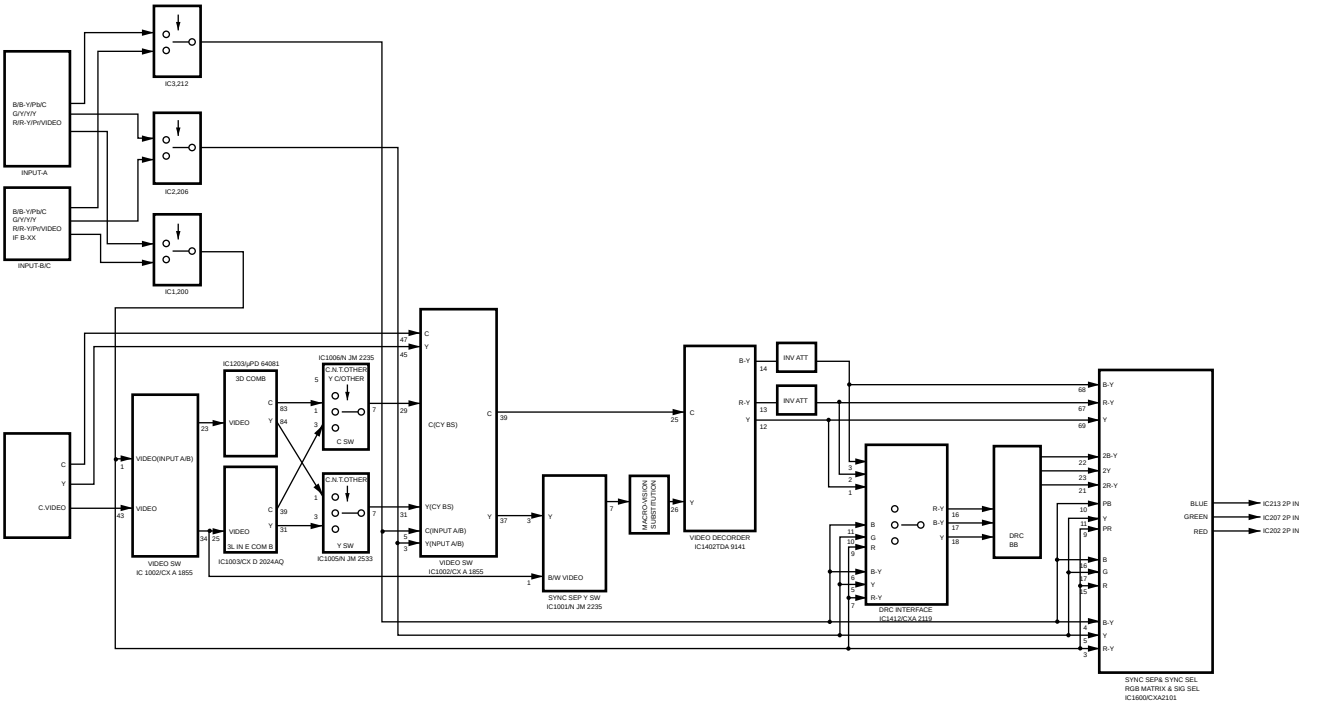


Fig. A Video Signal Processing Path

2. Sync processing path (See Fig. B)

When the video signal and Y/C signal are input, the sync signal sync separated by IC1402 is generated. Next, the HS signal is output from Pin 17 of IC1402, while the VS signal is output from Pin 11, and they are then passed through the buffer IC1413, after which the HS signal is output from Pin 24 of CN346 while the VS signal is output from Pin 23 to the BB board.

HS (2.fH) and VS (fv) signals fed back from the BB board are input to Pin 7 and Pin 6 of CN346 respectively. These signals input to Pin 19 (HS) and 20 (VS) of IC1600, switched and output from Pin 29 and 28 of IC1600.

When the component signal or 15 kRGB signal is input, the Y signal is selected by IC2 and IC206, and is input to Pin 7 of IC1801 (CXA2016 : sync separation) via the buffer Q1604, amplifier composed of Q1808, Q1809, and Q1813, and the clamp circuit composed of Q1806, Q1811, Q1812, and Q1807. The HS signal is then output from Pin 18 of IC1801, input to pin 5 of IC1001 (NJM2235M) via the H/V mix circuit composed of IC1806 and IC1814, selected, and output from Pin 7. Hereafter the signal is processed in the same way as the video signal. When the component signal is input, the H/V mix circuit will not operate.

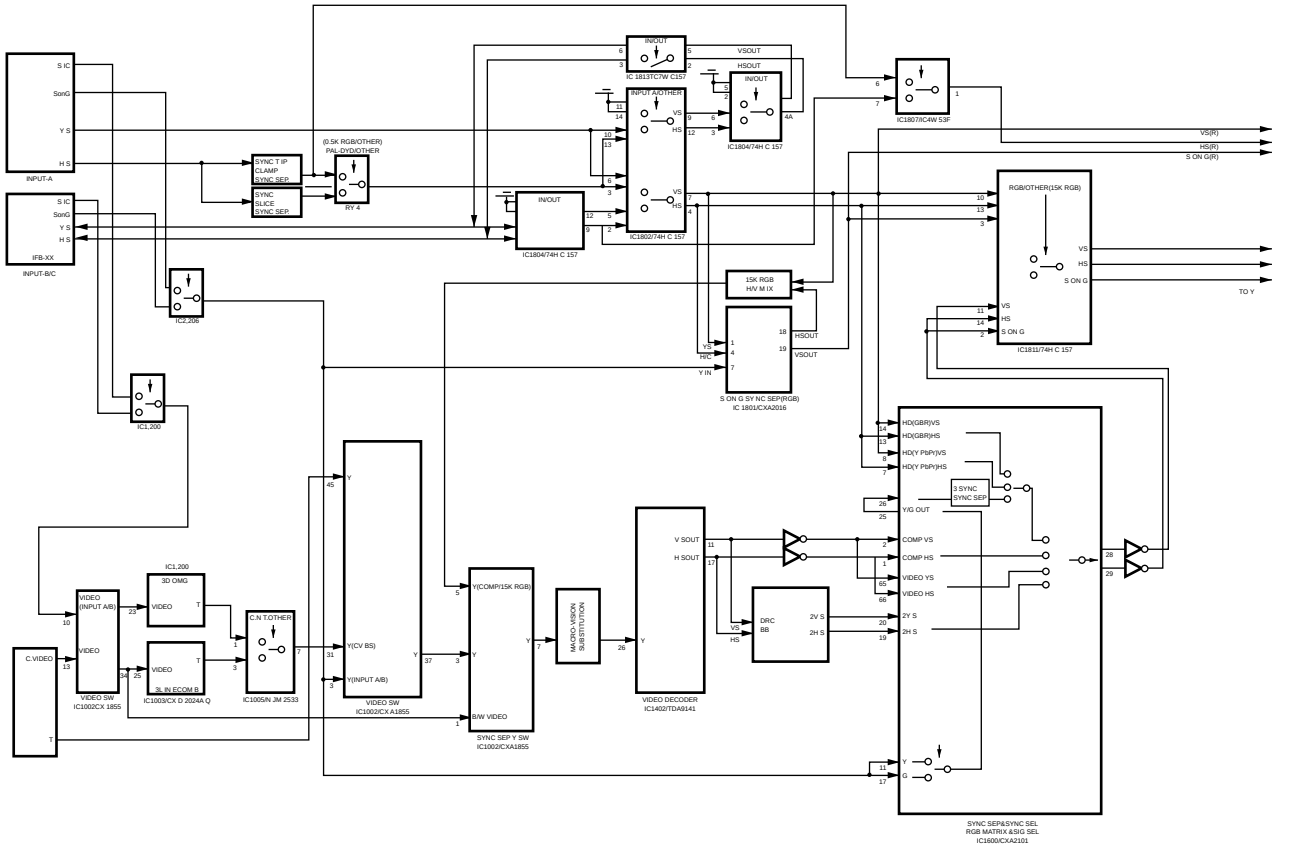


Fig. B SYNC Processing Path

SECTION 2
BB BOARD

2-1. OUTLINE

The BB board performs DRC processing of the color difference signals of the video system (C-VIDEO, Y/C, component, 15 kRGB).

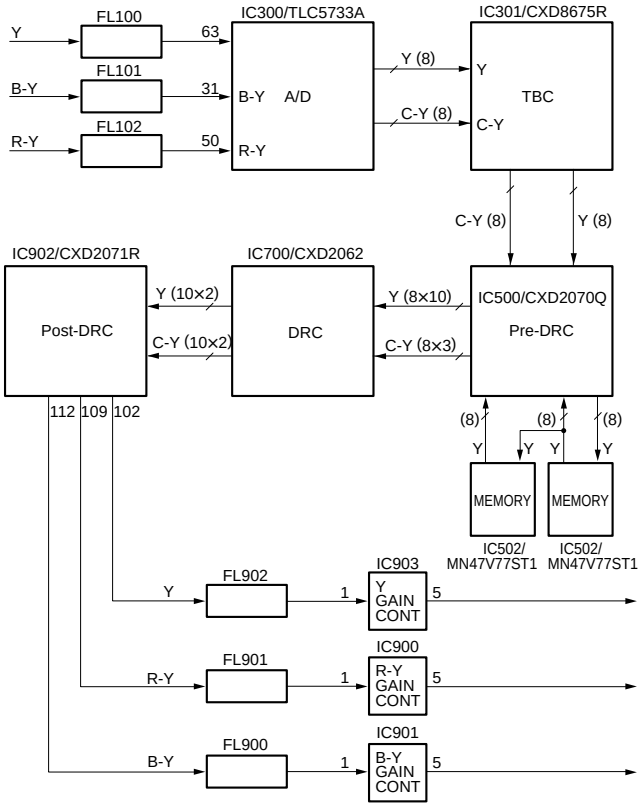


Fig. 2-1

2-2. A/D CONVERSION CIRCUIT

The C-VIDEO, Y/C, component and 15 kRGB signals converted to the color difference signal by the BA board are input to the BB board from Pins 30 (Y), 28 (B-Y), and 26 (R-Y) of CN360, passed through the low pass filter FL100 (Y), FL101 (R-Y), and FL102 (B-Y), and input to Pins 63 (Y), 31 (B-Y), and 50 (R-Y) of the A/D converter (IC300 : TLC5733A). The A/D converter (IC300) divides the voltage from the lower reference potential (VRB) to the upper reference potential (VRT) of the A/D converter by 256 and converts into the digital signal. The digital signal output from Pins 6 to 13 of IC300 and Pins 17 to 24 is input to the TBC (IC301 : CXD8675R).

2-3. TIME BASE CORRECTOR

IC301 (CXD8675R) reduces jitters in signals containing considerable jitter components such as a VCR playback signal.

2-4. DRC (DIGITAL REALITY CREATION) CIRCUIT

DRC (digital reality creation) process is performed by IC500 (CXD2070Q), IC700 (CXD2062Q) and IC902 (CXD2071R). Most DRC operations are performed by IC700 (CXD2062Q). IC500 (CXD2070Q) performs pre-DRC operations while IC902 (CXD2071R) performs post-DRC operations.
The DRC level is switched to HIGH, MID, or LOW by Pins 155 (NOMV) and 153 (BRMI) of IC902. The signal switched is then output from Pins 6 and 7 of IC1 (I^2 controller : CXA1875).

DRC Level	BRMI (153 pin)	NOMV (155 pin)
HIGH	LOW	LOW
MID	HIGH	LOW
LOW	HIGH	HIGH

Table. 2-1

2-5. SYNC SIGNAL

The V sync signal input from Pin 23 (VS) of the BB board from the BA board is input to Pin 67 of IC301, the phase of the H sync signal input to Pin 24 (HS) of CN360 is corrected by IC303 (TC74HC123A), and input to Pin 135 of IC301.
The sync signal is DRC processed in the circuit composed of IC301, IC500, IC700, and IC902, the H sync signal double speed processed is output from Pin 142 of IC902, and the V sync signal is output from Pin 145. The V sync and H sync are converted from 3.3 V p-p to 5 V p-p in IC107 (TC7SET08FU) and IC106 (TC7SET08FU) respectively, and sent from Pins 7 (HS) and 6 (VS) of CN360 to the BA board.

SECTION 3
CAR, CAG, CAB BOARDS

3-1. OUTLINE

The CAR, CAG, and CAB boards are composed of the same circuits. Reference numbers other than connectors and jacks are also exactly the same.
These boards insert the ABG pulse and blanking voltage into the signal input from the BA board. The signal is then divided into grid G1 and cathode (K), amplified, and sent to the CD board.

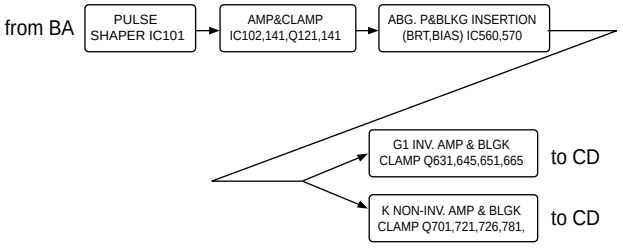


Fig. 3-1

3-2. PULSE GENERATION

The CAR, CAG, and CAB boards are input with the four pulses (5 V p-p)-clamp pulse, HD pulse, VD pulse, and blanking pulse. Based on these input pulses and control voltages, the required pulses are generated by IC101 inside the CAR, CAG, and CAB boards. The following shows the phase relation of each pulse.

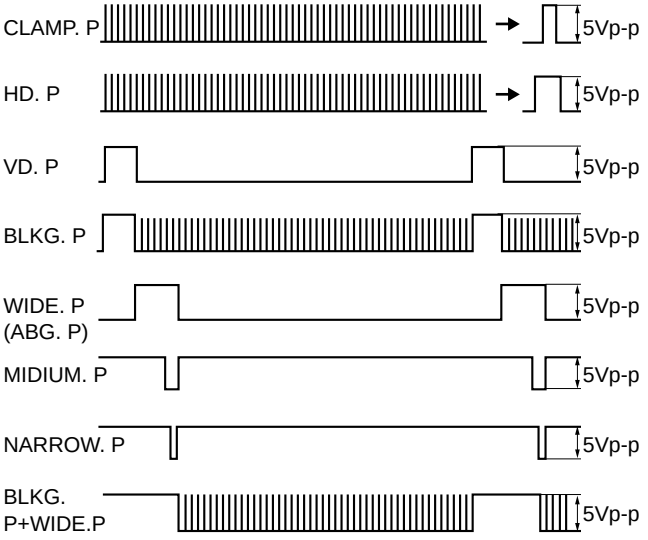


Fig. 3-2

3-3. PEDESTAL CLAMP CIRCUIT

The signal input from the BA board is amplified to 2 V p-p (GAIN : Max, CONT = Max) to 4 V p-p by IC102. The pedestal clamp circuit is composed of IC141, Q121, and Q141. The pedestal of the signal of TP511 and TP512 is adjusted to 2 V by RV145.

3-4. ABG PULSE AND BLANKING VOLTAGE

The ABG pulse and blanking voltage is determined by the BKG voltage supplied from the BA board. The BKG voltage is changed according to the brightness and bias. The ABG pulse is a G2 control pulse, and it supplies a constant current between the ABG pulses to maintain G2 at a constant. The blanking voltage is equivalent to the black level.

The voltage difference between the ABG pulse and blanking voltage is kept at a constant all the time. This is realized by supplying the designated constant current to R564 and maintaining the voltage difference between the outputs of Pins 1 and 7 of IC560 at a constant.

The outputs of Pins 1 and 7 of IC560 are input to the switcher IC570. The ABG pulse is input to Pin 5, the voltage of the inputs to Pins 6 and 7 of IC570 are switched by the input pulse as a trigger, to generate the ABG pulse and blanking voltage. The ABG pulse and blanking voltage is input to the Q511 base while the video signal is input to the Q510 base. The ABG pulse and blanking voltage are inserted into the video signal by the OR gate composed of D511.

When the blanking voltage changes according to the brightness and bias, so do the ABG pulse and blanking voltage. As the pedestal level of the video signal is always fixed, the voltage difference between the pedestal level and blanking voltage changes. Consequently, when the ABG pulse and blanking voltage are inserted into the video signal, the blanking voltage is clamped by the small signal circuits of G1 and cathode (K). As a result, the apparent pedestal level appears as if it has changed, although in fact the brightness and bias have changed.

3-5. G1 BLANKING

The G1 side is a inverse amplifier composed of Q631, Q645, and RV623. It amplifies the 4 V p-p signal to about 1.5 times.

When a signal is input to the Q631 base, current flows to the emitter. Q645, R632, and R633 make up the current source. Consequently, when the Q631 emitter current changes, the fluctuation becomes the Q645 collector current, and the inverse amplified waveform is output to RV632. The amplified signal is extracted for the voltage between the V blanking period, compared with the reference voltage by IC661 (1/2), the DC level of the signal is controlled by Q671, and the blanking voltage is clamped.

Q625 and D625 is a G1 white peak limiter. By OR gating Q651 and Q625, when the voltage drops to the specified value, Q651 goes OFF, Q625 turns ON, and the limiter operates. Adjustments are performed by RV622.

3-6. BLANKING OF CATHODE SIDE

As the signal is delayed by the G1 inverse amplifier, signals are also delayed at the cathode (K) side by IC595. This adjusts the phases of G1 and the cathode (K).

Like G1, the cathode (K) side is a non-inverse amplifier composed of Q701, Q721, and RV718. It amplifies 4 V p-p signals by about 1.5 times. When signals are input to the Q701 base, the Q701 emitter voltage is changed. As a result, current between emitters of Q701 and Q702 changes. As the Q701 base is fixed, a constant current is also supplied to R717. Consequently, the changes of the Q701 emitter becomes the changes of the Q721 collector current. The Q721 collector resistor is output with amplified waveform. The amplified signal is input to the CD board, and the video peak output is fed back to the CA board. The fed back signal is compared with the reference voltage by IC781, the DC level of the signal is controlled, and the blanking voltage is clamped at a fixed value.

To output images separately for the CAR, CAG, and CAB boards, set the switch S796 to OFF. The DC level is adjusted by RV796. Q741 and D738 form the VPS limiter circuit. By subjecting the outputs of Q736 and Q741 to the OR gate in D738, when the Q736 voltage rises above the specified value, Q736 goes off and Q741 turns ON. As a result, the VPS limiter operates.

The VPS limiter controls the limit voltage input from the BA board using the D/A converter. It suppresses VPS by adjusting this voltage.

SECTION 4
CBR, CBG, CBB BOARD

4-1. OUTLINE

The CBR, CBG, and CBB board is composed of the same circuits. Reference numbers other than the connector are also the same.
The CBR, CBG, and CBB boards supplies the G1 and cathode (K) signal input from the CD board as the drive voltage to the CRT via the CRT socket. G2 voltage and heater voltage are also supplied from the PE board, and they are supplied to the CRT via the CBR, CBG, and CBB boards.

SECTION 5
CDR, CDG, CDB BOARDS

5-1. OUTLINE

The CDR, CDG, and CDB boards are composed of the same circuits. Reference numbers other than connectors are also exactly the same.
The CDR, CDG, and CDB boards amplifies the G1 signal and cathode (K) signal input from the CAR, CAG, and CAB boards. The amplified G1 signal and cathode (K) signal are sent to the CBR, CBG, and CBB boards to drive the CRT.

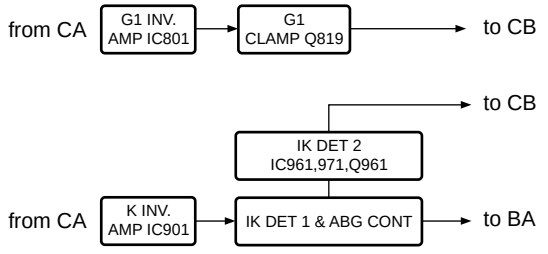


Fig. 5-1

5-2. G1 AMPLIFIER CIRCUIT

The G1 signal input from the CAR, CAG, and CAB boards is amplified by about 15 times by IC801. The amplified signal is sent to the circuit composed of IC802, Q815, Q819, Q821, D832, and D833, the blanking voltage is clamped at about −80 V using the V blanking period, and sent to the CBR, CBG, and CBB board. Clamp adjustments, amplitude adjustments, and limiter adjustments at the G1 signal side are performed by RV682, RV623, and RV622 of the CAR, CAG, and CAB boards.

5-3. K AMPLIFIER CIRCUIT

Like the G1 side, the G1 signal input from the CAR, CAG, and CAB boards at the cathode (K) side is amplified to about 15 times by IC901. The level of the blanking voltage output from IC901 is detected by R921 to R923, and fed back to the CAR, CAG, and CAB boards. The small signal amplifier of the CAR, CAG, and CAB boards and video amplifier of the CDR, CDG, and CDB boards are subject to feed back to maintain the blanking voltage at a constant all the time. Adjustments of the blanking voltage and amplitude can be performed by RV785 and RV718 of the CAR, CAG, and CAB boards.
The signals are passed through Q948 (Ik detection 1) for detection of the cathode current (Ik), passed through the photocoupler IC961 (Ik detection 2) for cathode current (Ik) detection, and supplied to the CBR, CBG, and CBB boards.

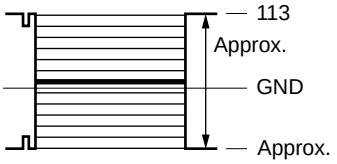


Fig. 5-2

5-4. IK DETECTION 1 CIRCUIT

In the video period, the MEDIUM pulse becomes a “High” level, and Q974 turns ON. As a result, the collector current (Ik) of Q948 (Ik detection 1) is detected by R960, passed through the buffer IC990 (2/2). And sent to the BA board. The current input to the BA board is used for an ABL and Ik protector.
During the V blanking period, the MEDIUM pulse becomes the “Low” level, and Q974 goes off. The collector current (Ik) of Q948 (Ik detection 1) is detected by R960 and R961, amplified by two times by IC990 (1/2), and Ik is detected by IC981 by the NARROW pulse. The result of Ik detection is supplied to the Y board to control G2. In the Y board, the result of Ik detection is monitored for 20 minutes after the power was turned on, feed back is imposed so that the result of Ik detection remains at a constant value to control the G2 voltage.
After 20 minutes, data is output from the Y board in accordance with the result of Ik detection.
At the time, ABG.P is set to OFF state.

5-5. IK DETECTION 2 CIRCUIT

To compensate the temperature characteristics, the Ik detection 2 circuit (IC961) incorporates two photocouplers.

The cathode side is inserted with a photocoupler 1, the same current as that which flows there (Ik) flows to photocoupler 2, and feed back is imposed by IC971 (2/2). The cathode current (Ik) is detected by the current flowing to the photocoupler 2. The value detected by R975 and RV975 is compared with the reference value in IC971 (1/2), and the comparison results are sent to the Y board as the CRT protector.

SECTION 6
DA BOARD

6-1. OUTLINE

The DA board generates AFC, V hold, and registration waveforms.

6-2. AFC

Pin C21 of CN170 is input with the 2µsec H sync signal of the YA board. The H sync signal is input to Pin 1 of IC110 (µPC1377C) and used as the reference signal of the AFC system. The HD signal returned from the deflection system is input to Pin A29 of CN170 from the E board. The HD signal is input to Pin 3 of the H phase shift IC (IC106 : MC-8639A) via the buffer composed of Q120 and Q121. IC106 is incorporated with a 3-stage monostable multibivrator, where the 50 % duty rectangular wave is generated in the initial stage and 50 % ±10 % rectangular wave in the second stage. In the third stage of the monostable multibivrator, the 50 % rectangular wave is generated (Pin 8 of IC106).
The rectangular wave duty in the second stage can be varied by 50 % +10 % using the external control voltage. As a result, the 50 % duty rectangular wave is output after a delay of about 1H (changes by ±10 % according to the external control) from the input. The rectangular wave is input to Pin 3 of IC110, and used as the HD (pseudo HD) for AFC to control the phases of Pin 8 of IC106 and Pin 1 of IC110 so that they are always synchronized.

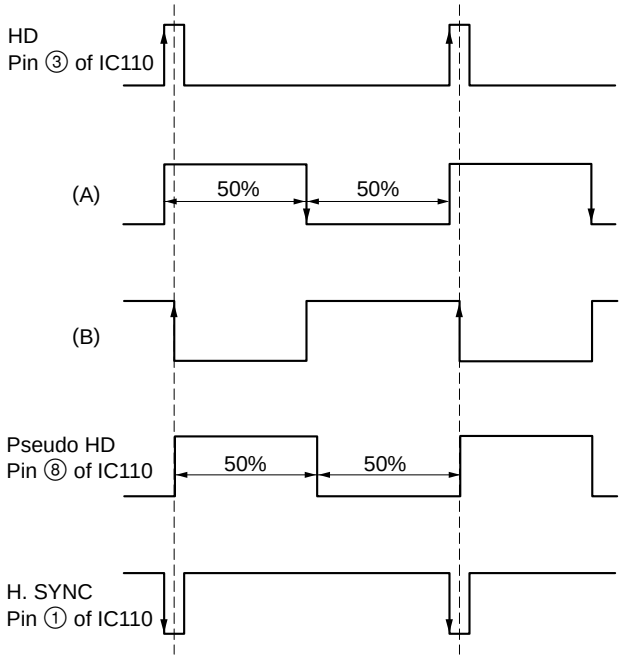


Fig. 6-1

In the multi-scan AFC system, the H sync is F-V converted by IC101 and IC104, and the current proportionate to fH is supplied to C137 and C138 in the current mirror circuit composed of Q109 and Q110. Pin 5 of IC110 is incorporated with a voltage detector and switch. When the Vcc voltage rises above 2/3, the switch turns on, electric charge of C137 and C138 is discharged. The switch goes off when the Vcc voltage discharges to 1/3.
This operation is repeated and the free oscillation (f0) is performed for the input fH.
The horizontal oscillation pulse for horizontal deflection is generated by free oscillation, and output from Pin 10 of IC110 (µPC1377C). The horizontal oscillation pulse is supplied to the E board, and becomes the drive pulse for horizontal deflection.
The H sync input to Pin 1 of IC110 and the error difference voltage of the pseudo HD input to Pin 3 are output from Pin 4, and fed back to pin 5.
The (a) area shown in the figure is a time constant circuit determined by C137, C138, and internal resistor of the IC. This time constant becomes f0 error when the frequency becomes high, resulting in deviation. Therefore f0 is corrected by IC107 (µPC814G2)/Q108.
For the video signal, as the sync changes when the VCR is fast forwarded and the AFC may deviate in some cases, a fixed voltage is supplied by Q115 to determine f0.

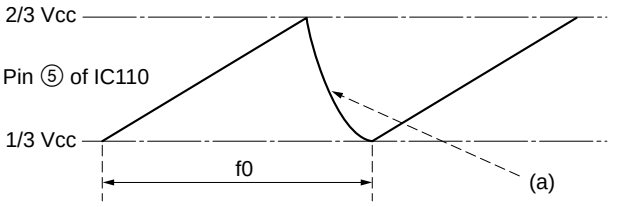


Fig. 6-2

6-3. V HOLD

Pin C 16 of CN170 is input with V sync from the YB board. The V sync is waveform shaped by IC103, input to IC110, to becomes the trigger pulse for the V hold. The V sync input to IC103 is F-V converted at the same time by IC103. The F-V converted voltage is converted to current by the constant current circuit composed of IC109 and Q107, and the current of Pin 17 of IC110 is controlled. The capacitor connected to Pin 18 of IC110 is discharged from pin 17. As a result, the free run frequency is determined according to the discharge time.

When no signal, it is detected as no F-V conversion output. When IC108 (µPC393G2) becomes “Low” level, R129 is grounded, and free runs at the time constant determined by C135 × R149. When the trigger pulse generated from the V sync is input during this free run, it is synchronized to the V sync from Pin 12, and the VD signal is output.
The VD signal is used as the trigger of the registration waveform by IC451. The VD signal is output from Pin C 11 of CN170, used as the trigger of the MG focus waveform by the DE board, and used as the saw wave trigger for vertical deflection in the DF board.

6-4. AD/HD CIRCUITS

This unit has a simulation mode for special optical systems. In the simulation mode, the retrace time of the horizontal saw wave (H.SAW) is constant in respect to the tracing time. Consequently, when fH changes, the retrace time also changes. In the normal mode, as the retrace time is always constant, when the waveform is generated at the same timing, the center of the waveform deviates.

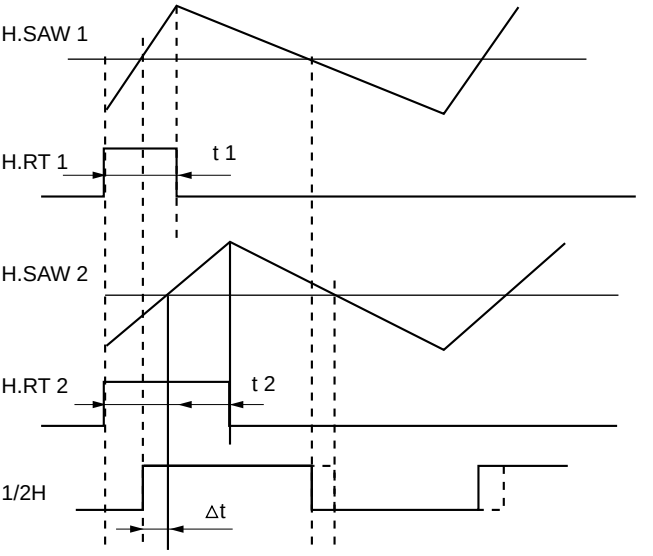


Fig. 6-3

As a result, the center of the registration correction deviates, disabling the desired correction. The phase of the registration waveform output amplifier on the DC board also delays. In the AD/HD circuit, to correct “phase delay” and “retrace time deviation”, a HD pulse whose phase is more advanced than the normal HD pulse is generated.
IC114 forms a monostable multibivrator set with a longer time constant and is triggered at the rising edge of the 1/2H pulse.
The monostable multibivrator composed of IC116 (1/2) is triggered by the falling edge of the retrace (HRT) pulse, and the time width pulse (A.TP) for correcting “phase delay” is generated. At the falling edge of this pulse, IC116 (2/2) is triggered to generate the reset pulse, and the monostable multibivrator IC114 (1/2) is reset.
As a result, the 1/2H pulse rising edge is positioned at the 1/2 point of the retrace (H.RT) pulse width to generate the “1/2H.RT+A.TP” width pulse (AD.W).

The monostable multibivrator composed of IC114 (2/2) is triggered at the falling edge of the HD12 V pulse, but the time constant is controlled by the Q122 current.
The output from the $\overline{Q}$ terminal of the monostable multibivrator IC114 (2/2) is input to IC155 (2/2), the earlier mentioned "1/2H.RT+A.TP" width pulse and rectification voltage are compared, and the Q122 current is controlled so that the difference voltage becomes 0 V.
As a result, IC114 (2/2) outputs the "1H-1/2H.RT+A.TP" width negative pulse, to become a positive pulse whose phase is advanced by "1/2H.RT+A.TP" from the falling edge of the apparent HD 12 V pulse. (Refer to Fig. 6-4.)

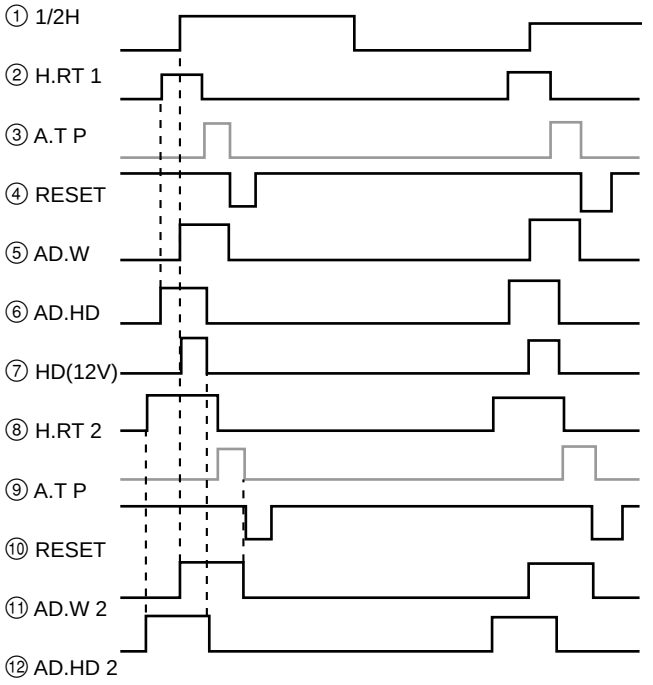


Fig. 6-4

When the retrace time changes (same fH), the time, if the phase equivalent to 1/2 of the retrace time difference before and after the change changes, the centers of the waveforms match. The trace time difference before and after the change is the same as the difference of the retrace time. Taking the retrace time before change as "H.RT1" and the retrace time after change as "H.RT2", the difference before and after the AH.HD pulse becomes (1/2H.RT 1 + A.TP) − (1/2H.RT 2+A.TP) = 1/2 (H.RT 1-H.RT 2), so that the center position of the waveform can be maintained.

6-5. REGISTRATION WAVEFORM GENERATOR

The vertical waveform for correcting the registration is generated by IC451. IC451 generates horizontal and vertical basic waveform, but to reduce the registration noise, only the vertical waveform is used. The horizontal waveform is generated by a different circuit.

6-5-1. Basic Rectification Circuit

The following describes the basic rectification circuit used in the DB board.
Fig.6-5 shows the half-wave rectification circuit. When ac voltage is input to the Q1 base, only the positive polarity is output from the Q3 emitter. As the Q2 base is ground via R2, it becomes 0 V. When the Q2 emitter voltage is about to drop below "0-VBE" V, current flows to the Q2 base, and Q2 turns ON. When Q2 turns ON, the Q2 emitter voltage will not fall below "0-VBE".
To equalize the Q1 and Q2 base voltages, Q1/Q2 uses pair transistors with the same VBE and hFE characteristics. For Q1 and Q2, to reduce the VBE changes caused by the Q1 and Q2 temperature characteristics, the same constants are used for R1 and R2 and set so that the base current becomes equal. Q3 corrects the DC components changed by the changes in the VBE. By equalizing the R3 and R4 constants, the Q1 and Q3 collector current (IC) is made the same, to compensate the voltage (VBE) decreased by Q1.
The PNP transistor is used for Q1 and Q2, while a NPN transistor is used for Q3.
These operate as half-wave rectification circuits with negative polarity.

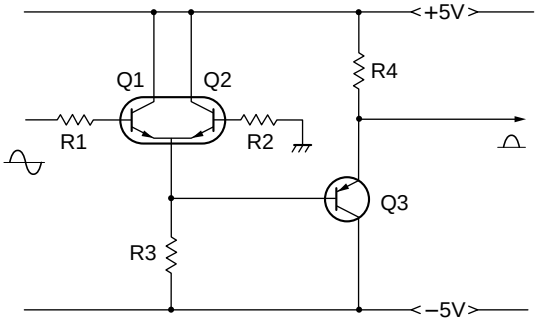


Fig. 6-5

6-5-2. V Basic Waveform

The VD pulse is input to Pin 5 of IC451 as the trigger of vertical components. Table 6-1 shows the trigger waveform and output waveform. Pin 25 of IC451 is a vertical amplitude control terminal, and is input with 0.5 V to 1.25 V. Inside IC451, AGC is imposed on the sawtooth waveform, and the parabola waveform and V sine waveform are generated by the internal multiplier based on the sawtooth waveform.

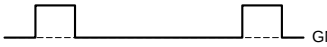
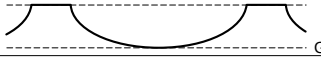
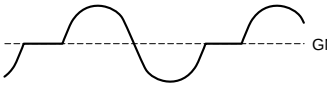
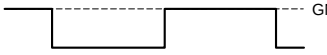
VD. IN	⑤	 GND
V. SAWTOOTH (+)	⑨	 GND
V. SAWTOOTH (−)	⑩	 GND
V. PARA (+)	⑪	 GND
V. SIN	⑬	 GND
V. SO	④	 GND

Table. 6-1

6-5-3. H.SAW Waveform

The H.SAW waveform is generated by the mirror integration circuit composed of IC305. The input of IC305 is connected to the analog switcher IC302, the voltage supplied during the tracing and retracing operations is switched to determine the length of these operations. The output of IC305 is integrated by IC306, the integrating output is input to IC305 during tracing by the analog switcher IC302. In the above loop, the average value of the voltage of the one positive and negative periods output from IC305 is controlled to become 0 V.
In the normal retracing period, the H size voltage amplified by IC352 and IC354 is input to IC305 via the analog switcher composed of IC311 and IC302.
The switching of the trace and retarce of the analog switcher IC302 is controlled by IC308 (JK flip flop).
IC308 (JK flip flop) is triggered by the AD/HD pulse, selecting the IC311/IC302, and mirror integration is performed by IC305 using the current proportionate to the H size voltage during the retrace period.
At this time, the output of IC305 is divided and buffered by R322, R323, and IC307, and compared with the H size voltage amplified by IC352 and IC354 by the comparator (IC309). As IC308 (JK flip flop) is reset by the compared output, the H.SAW waveform is controlled so that the retrace time becomes constant by the peak voltage proportionate to the H size voltage.

In the simulation mode, the integrated voltage generated by IC306 during the retrace period is inverted, switched by the analog switch IC311, and input to IC305.
As a result, the H.SAW waveform with constant trace/ retrace ratio matching the resistance (R302, R380, R225) connected to the input of IC305 is generated.

6-5-4. H Parabola Waveform Generation Circuit

The horizontal parabola waveform is generated by multiplying the H.SAW waveform by the multiplier (IC303). When the H.SAW waveform is multiplied simply, as parabola waveform is also generated in the retrace period (see Fig. 6-6-②) the retrace period is switched by the DC voltage by the analog switcher (IC302), and output to the buffer (IC402).
This DC voltage must be proportionate to the peak voltage of the parabola waveform, but because the parabola waveform is generated by multiplying the H.SAW waveform, the H.SAW waveform is a peak voltage proportionate to the H size voltage. Consequently, the DC voltage is generated by multiplying the H size voltage by IC301. Also as the peak voltage and DC offset of the H.SAW waveform are affected by the inconsistencies of the multiplier (IC303), adjustments are required.

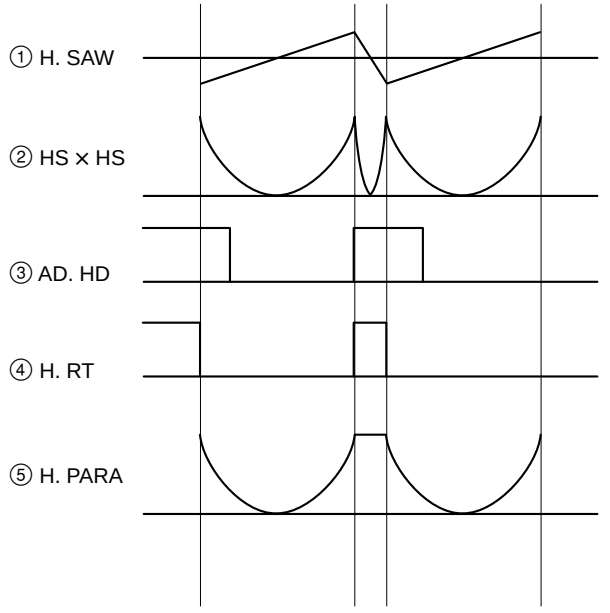


Fig. 6-6

6-5-5. H Sine Waveform Generation Circuit

The H.SAW waveform is half-wave rectified by the circuit composed of Q401 to Q404 (See section 6-5-1. Basic Rectification circuit.). The positive polarity (+) side of the waveform is input to the + terminal of IC405 (1/2) and the - terminal is connected to the − terminal of the ope-amplifier to obtain the waveform whose first half is inverted from 1/2H of the H.SAW waveform to the + side (Fig. 6-7-②). The level is also shifted by IC407 and IC405 so that this waveform is balanced centering around 0 V (see Fig. 6-7-③).
Next, the retrace period is switched so that the DC becomes 0 V by the switcher IC403 (Fig. 6-7-⑤), this waveform and the H.SAW waveform are multiplied by IC406, to generate the H sine waveform (see Fig. 6-7-⑥). The H sine waveform is passed through the analog switcher again, and the DC offset of IC406 will be absorbed during the retrace period. IC313 (2/2) controls so that the + side of the H sine waveform and voltage of the − side become balanced.

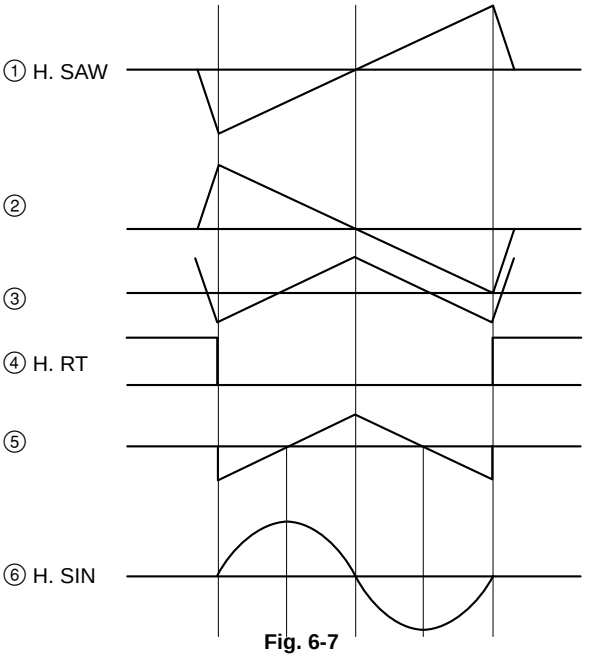


Fig. 6-7

SECTION 7
DB BOARD

7-1. OUTLINE

The DB board generates the top, bottom, left, and right pin cushion and key stone from the basic waveform generated by the DA board, and the secondary waveform required for registration correction of the zone shown in Fig. 7-1. It also generates the curve blanking pulse in the simulation mode.

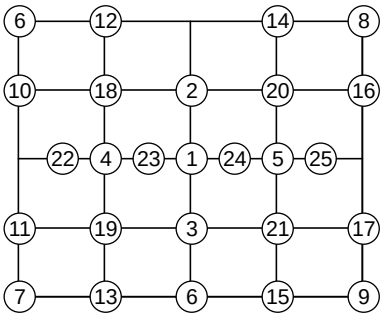


Fig. 7-1

7-2. SECONDARY WAVEFORM CIRCUIT

The secondary waveform circuit is composed of the following circuits.

- Multiplier for horizontal components and vertical components of the basic waveform
- Multiplier output amplifier
- Analog switcher for multiplication waveform time axis (1/2H or 1/2 V) separation
- Half-wave rectification circuit (basic circuit 1)

It is also possible to use only one part of the above circuit as required.
The following table shows the input basic waveform names, semiconductor references used, and output waveform.

Input Signals	Multiplier	Switch	Half-wave Rectifier	Others	Output Signals	Compensation
H.SIN/V.SIN	IC102	IC101	Q105, 107	–	X10	Zone 19
			Q106, 108	–	X9	Zone 18
			Q101, 104	–	X11	Zone 20
			Q102, 103	–	X12	Zone 21
H.SIN/V.P	IC202	IC201	Q205, 207	–	X6	Zone 15
			Q206, 208	–	X4	Zone 13
			Q201, 203	–	X5	Zone 14
			Q202, 204	–	X3	Zone 12
H.P/V.SIN	IC302	IC301	Q305, 307	–	X2	Zone 11
			Q306, 308	–	X1	Zone 10
			Q301, 303	–	X8	Zone 17
			Q302, 204	–	X7	Zone 16
H.S/V.S	IC402	–	–	–	VKEYS	V KEY
		IC401	–	Buffer IC501 (1/2)	KL	Left Key
			–	Buffer IC501 (2/2)	KR	Right Key
			Q405, 407	–	U3	Zone 7
			Q406, 408	–	U1	Zone 6
			Q401, 403	–	U2	Zone 8
			Q402, 404	–	U4	Zone 9
H.S/V.P	IC601	–	Q601, 603	–	PR	Right Pin
			Q602, 604	–	PL	Left Pin
H.P/V.S	IC604	–	–	–	VPIN	V PIN
			Q605, 607	–	PB	Bottom Pin
			Q606, 608	–	PT	Top Pin
HIS 1/SINL	IC703	–	Q705, 707	–	W1	Zone 22
			Q706, 708	–	W2	Zone 23
HIS 1/SINR	IC701	–	Q701, 703	–	W3	Zone 24
			Q702, 704	–	W4	Zone 25
H.SIN	–	–	Q709, 710	–	SINL	Zone 4
			Q711, 712	–	SINR	Zone 5
V.SIN	–	–	Q501, 503	–	SINT	Zone 2
			Q502, 504	–	SINB	Zone 3
U1/U2	–	–	–	IC503 (2/2) Addition	KT	Top Key
U3/U4	–	–	–	IC503 (1/2) Addition	KB	Bottom Key

Table. 7-1

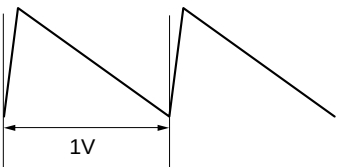
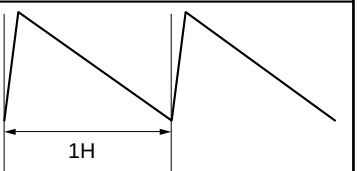
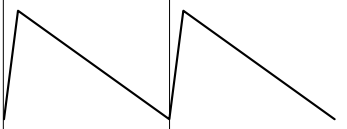
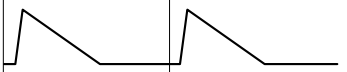
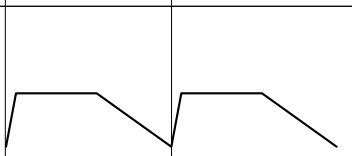
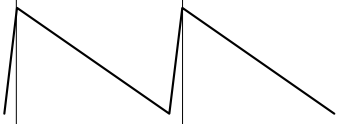
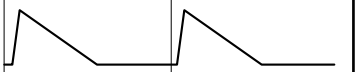
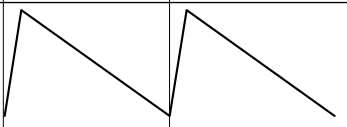
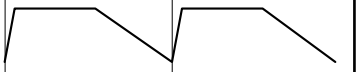
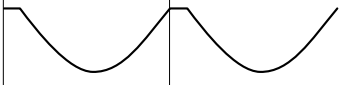
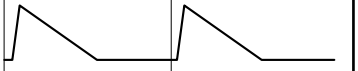
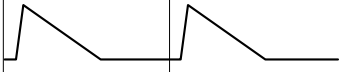
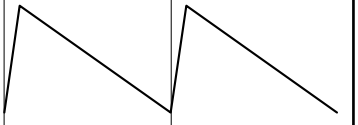
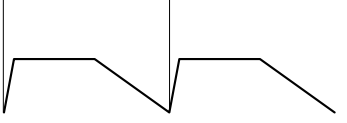
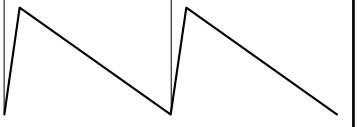
Functions	Output Signals	V period	H period
V Key	VKEYS		
V Pin	VPINS		
Top Pin	PT		
Bottom Pin	PB		
Left Key	KL		
Right Key	KR		
Left Pin	PL		
Right Pin	PR		
Top Key	KT		
Bottom Key	KB		

Table. 7-2

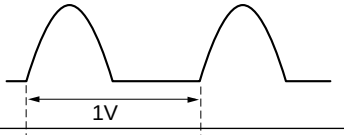
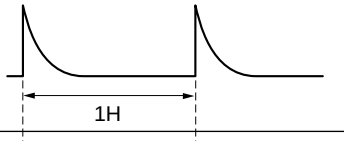
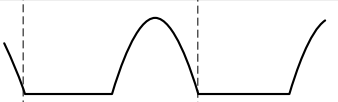
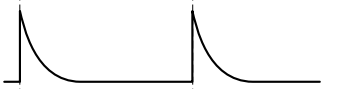
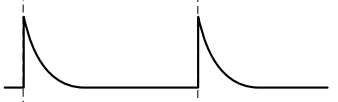
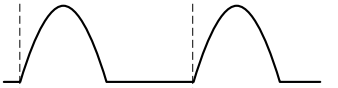
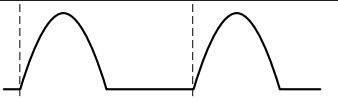
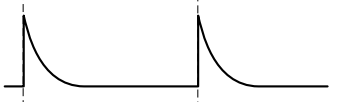
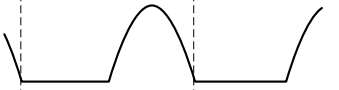
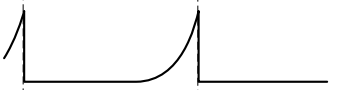
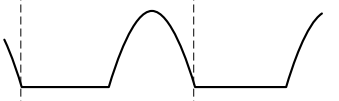
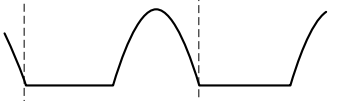
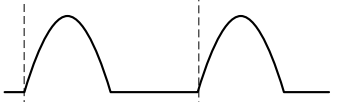
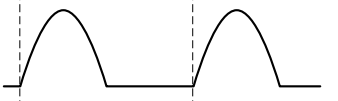
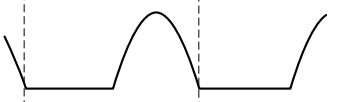
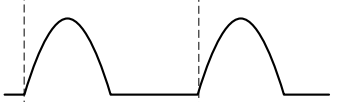
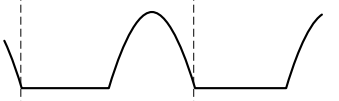
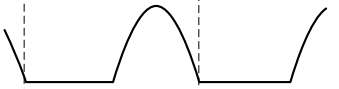
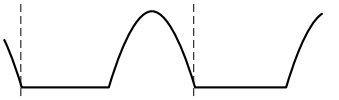
Functions	Output Signals	V period	H period
ZONE 10	Pin ⑫ of IC24 × 1		
ZONE 11	Pin ⑧ of IC24 × 2		
ZONE 12	Pin ⑧ of IC25 × 3		
ZONE 13	Pin ⑫ of IC25 × 4		
ZONE 14	Pin ㉑ of IC24 × 5		
ZONE 15	Pin ㉕ of IC25 × 6		
ZONE 16	Pin ㉕ of IC24 × 2		
ZONE 17	Pin ㉑ of IC24 × 2		
ZONE 18	Pin ⑫ of IC26 × 2		
ZONE 19	Pin ⑧ of IC26 × 2		
ZONE 20	Pin ㉕ of IC26 × 2		
ZONE 21	Pin ㉑ of IC26 × 2		

Table. 7-3

7-3. CURVE BLANKING CIRCUIT

This circuit controls the top and bottom blankings in the simulation mode in the same way as the registration pin cushion and keystone. It is used in curve screen 3D, etc.
The V.SAW waveform is half-wave rectified by the basic circuit 1 composed of Q901 to Q904. The positive polarity side of the waveform is input to the no-inverse (+) terminal of the ope-amplifier (IC908) while the negative polarity side of the waveform is input to the inverse (−) terminal of the ope-amplifier. As a result, the first half of the V.SAW waveform is inverted to the positive polarity side from the negative polarity (Fig. 7-2-②). The next waveform is level shifted to the negative direction by IC908 (Fig. 7-2-③). The level-shifted waveform is half-wave rectified by IC909, D901, D902, and the front 1/4 and back 1/4 triangle wave (Fig. 7-2-③) is generated. The triangle wave is converted to the H period step-waveform (Fig. 7-2-⑤) by the sample hold circuit composed of IC909, IC910, and IC912 and the first half and second half of the V period are separated by the analog switcher IC902, and input to the comparator (IC906).
The comparison input of the comparator (IC906) is input with the waveform generated by adding the “H.PAR”, “H.SAW”, and “DC” controlled by the DA converter of the DD board via the buffer (IC905). As a result, a pulse whose width changes proportionately to the comparison input for every 1H (Fig. 7-2-⑦) is generated in the comparator output. This pulse is AND gated with the blanking pulse by IC907, and used as the blanking pulse to perform curve blanking.

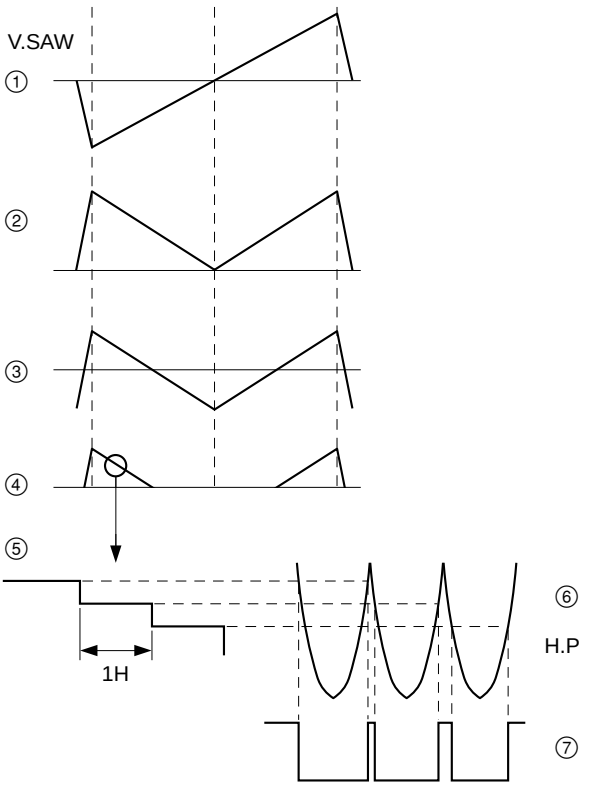


Fig. 7-2

SECTION 8
DC BOARD

8-1. OUTLINE

The DC board is composed of the R/G/B H sub drive circuit, V sub drive circuit, and protector circuit.

8-2. SUB DEFLECTION DRIVE CIRCUIT

The sub deflection drive circuit adopts a power IC (IC1 : 4STK392-220) with three built-in drive amplifier channels to simplify the circuit configuration. One power IC is provided for the H sub and V sub each.
The power IC (IC1) is separated into the preamplifier power supply (Pins 3 and 4) and drive amplifier power supply (Pin 7/11, Pin 12/16, and Pin 21/25). The "+50 V" dc current is supplied to the VCC (+) side, while the "−50 V" dc current is supplied to the VCC (−) side. Pin 2 of the power IC (IC1) is a masking terminal for the drive output. It momentarily becomes the no-output state by Q2 (V side) and Q12 (H side) when the power is turned on.
The drive amplifier in the power IC (IC1) for the sub deflection drive circuit uses the general power ope-amplifier. The power amplifier, sub deflection coil, and resistor for deflection current detection make up the non-inverted amplifier.
The non-inverted (+) input terminals (Pins 5, 18, 19) of the built-in amplifier of the power IC is input with the sub correction wave form signal from the DD board, and the output voltage of the drive amplifier is controlled so that the voltage of the detection resistor becomes the same as the input voltage of the non-inverted (+) input terminal.

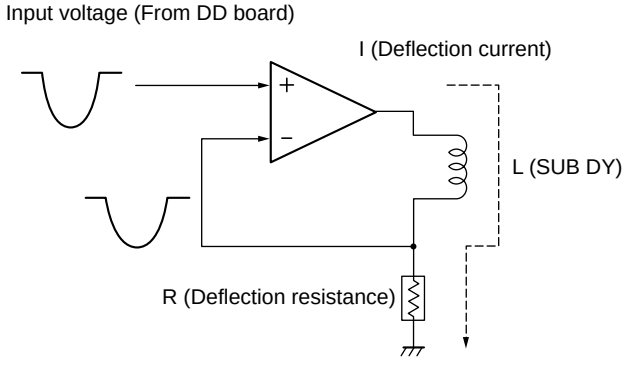


Fig. 8-1

8-3. PROTECTOR CIRCUIT

The +50 V line protector is composed of R115, R126, Q11, and IC2 (LM393P : 1/2), IC3 (LM393P : 1/2) to configure the current detection protector. When the +50 V line consumption current exceeds a certain value, the voltage of R127 increases proportionately to the current amount, and the protector is imposed by IC2 and IC3 according to this voltage value. There are two types of protector. One is the over IK protector which detects the sub excessive correction in the normal operation state and the second is the DC protector which detects excessive current when a problem occurs in the sub drive circuit. The +50 V line consumption current amount of both protectors is monitored, and when the current becomes around 2.3A, the over IK protector operates. When it becomes about 2.5A, the DC protector operates. When the over IK protector operates, a message is displayed on the screen and the CPU controls so that no more corrections are performed. When the DC protector operates, the power of this unit is turned off immediately.

The −50 V line side operates in the same way. The OR gate with the +50 V line side is acquired by IC2 and IC3.

SECTION 9
DD BOARD

9-1. OUTLINE

The DD board is mounted with a D/A converter for electronic control so that operations can be carried out using the remote commander such as registration, etc.

The waveform generated in the DA board and DB board is controlled by the electronic control of this board, and used for registration correction, curve blanking control, and uniformity correction.
This board is controlled by the 8-line serial bus.
The DD board is mounted with thirty D/A converter ICs. Which ICs are used is determined by the combination of the LD pulses (four) and SDA signals (three) supplied from the YB board.

9-2. D/A CONVERTER

MP670AS is adopted for the D/A converter of the DD board. It incorporates eight D/A converters which are controlled by the 3-line serial bus -SDA, CLK, and LD. The serial data (SD) for control is 12 bits long. It is synchronized with the rising edge of the clock (CLK) and sent. The serial data transferred is 12 bits and it is latched by inputting the positive polarity LD pulse.

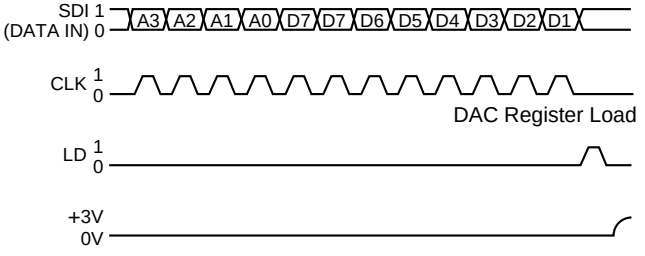


Fig. 9-1

SDI	CLK	LD	$\overline{PR}$	Input Shin Register Operation
X	L	L	H	No Operation
X	I	L	H	Shift One Bit in from SDI (Pin 20)
				Shift One Bit out from SDO (Pin 18)
X	X	L	L	All DAC Register × 80 N
X	L	H	H	Load Serial Register Data Into Dac (X) Register

Table. 9-1

The serial data (SD) is sent by MSB. The higher 4 bits (A3 to A0) is used as the address bit. Of the eight D/A converters incorporated, one is specified. The lower 8 bits (D7 to D0) are used as the data bits, and determine the output gain of the D/A converter specified by the address bit.

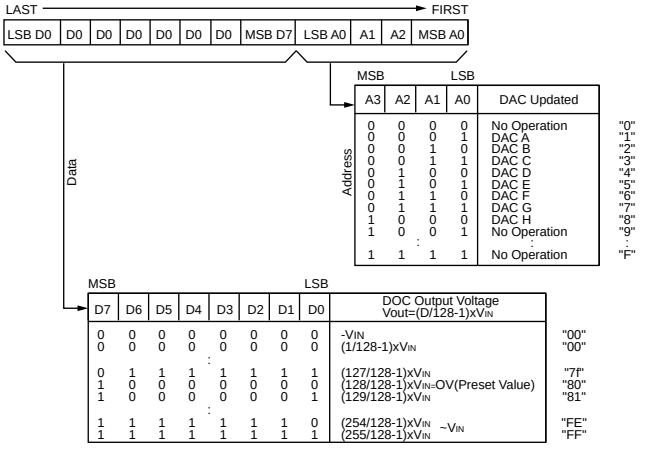


Fig. 9-2

When the data is “FF”, the output of the D/A converter become “Vin” which is more or less equivalent to the input. When the data is “80”, the output of the D/A converter becomes “0 V”. When the data is “00”, the output of the D/A convertor is inverted to become “−Vin”. During this time, the output of the D/A converter is more or less linear, and changes by “Vin /127” at a time per bit. If the voltage is within ±3 V, the Vin can be processed regardless of whether it is DC or AC.
One examples of the output when the SAW waveform is input is shown in Fig. 9-3.

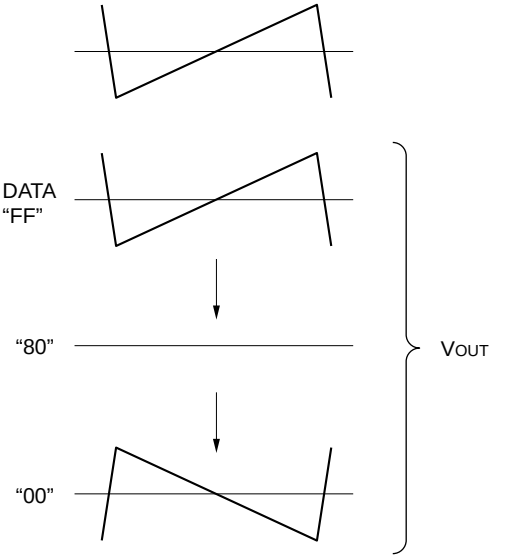
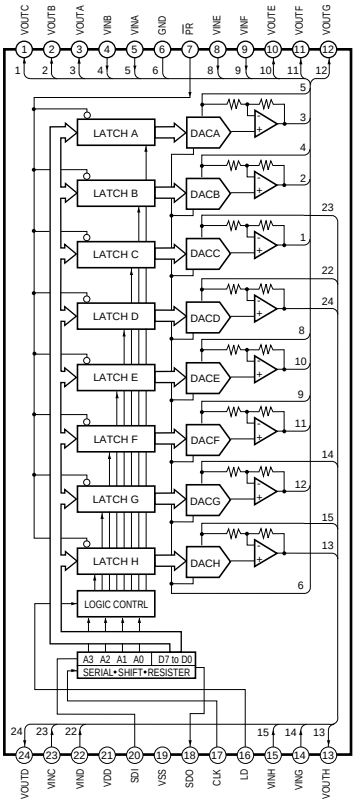


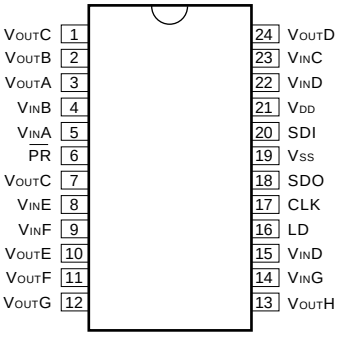
Fig. 9-3

Pin 7 of the D/A converter (MP670AS) is the reset terminal. When the power of the unit is turned on, Pin 7 is set to “Low” by the reset circuit (IC116, IC322 : RHSVLA3AA) and imposed with power on reset. When reset is imposed, the built-in D/A converter data is set to “80” and all outputs become “0 V”.

The registration waveforms generated in the DA board and DB board are input to the D/A converter, and based on the address and data supplied form the YA board, they are output at different amplitudes.

The waveform output are added as the sub DY components of the R, G, and B curve blanking control components, and uniformity correction components, and output from the inverse buffer amplifier (DA828AR) composed of IC313 to IC317, IC323, and IC324.





Pin No.	Name	Description
1	VOUTC	DAC C Output
2	VOUTB	DAC B Output
3	VOUTA	DAC A Output
4	VINB	DAC B Reference Input
5	VINA	DAC A Reference Input
6	GND	Ground
7	$\overline{PR}$	Preset Input, Active Low
8	VINE	DAC E Reference Input
9	VINF	DAC F Reference Input
10	VOUTE	DAC E Output
11	VOUTF	DAC F Output
12	VOUTG	DAC C Output

Pin No.	Name	Description
13	VOUTH	DAC H Output
14	VING	DAC G Reference Input
15	VINH	DAC H Reference Input
16	LD	Load DAC Register Strobe. Active High Input
17	CLK	Serial Clock Input
18	SDO	Serial Data Output
19	VSS	Negative Power Supply
20	SDI	Serial Data Input
21	VDD	Positive Power Supply
22	VIND	DAC D Reference Input
23	VINC	DAC C Reference Input
24	VOUTD	DAC D Output

Fig. 9-4

9-3. SELECTION OF D/A CONVERTER

Six D/A converter ICs are serial-connected. Taking this state as one group, 3 groups form one group. Including the other boards, there are altogether 5 groups.
The D/A converter is controlled from the YA board for each of these groups. Consequently, since 12 bits (8 bit control data + 4 bit address data) are required for each D/A converter, which means that 72 bit serial data will be required for the six D/A converters. These D/A converters are also controlled by the 4-bit (LD0 to LD3) signals and clocks serving as the group selection and reading signals.

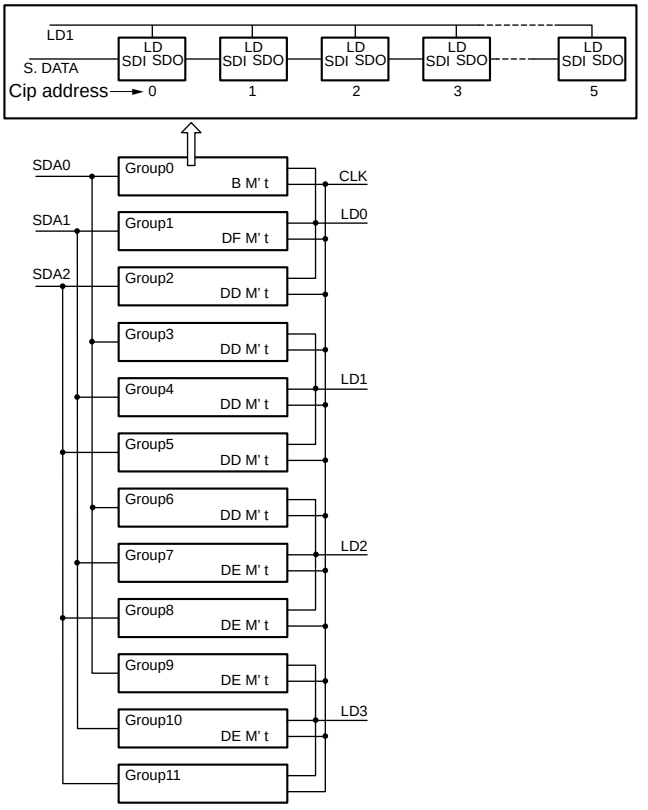


Fig. 9-5

SECTION 10
DE BOARD

10-1. OUTLINE

The DE board generates waveforms of MG focus/4-pole/6-pole, adjusts the waveform levels of the D/A converter, adds the waveforms, etc.

10-2. WAVEFORM GENERATOR

MG focus/4-pole/6-pole adjustments include the “all” adjustment for changing the overall screen, and the “zone” adjustment for adjusting 8 points on the screen.
The MG focus, 4 poles and 6 poles waveforms are basically the same as the registration adjustment waveforms. However as the center position of the deflection system and that (screen center) of the focus system do not necessarily coincide due to the projection system of the unit, the registration correction waveform of the deflection system cannot be used. Consequently, the phase of the HD pulse used as the timing pulse is shifted by the voltage of the “H phase” to generate the MG.HD pulse, and this MG.HD pulse is used as the trigger pulse to create the synchronized correction waveform.
The waveform generator uses the same IC (CXA1470AS : IC) as the registration circuit. It generates a 1/2H pulse and 1/2 V pulse whose phase is shifted by 1/2 period against the H parabola, V parabola waveform, MG.HD pulse, and MG.VD pulse. The above waveform is input to the multiplier (IC4, IC17 : CXA1726AM) and created.

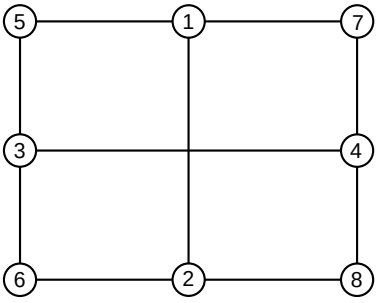


Fig. 10-1

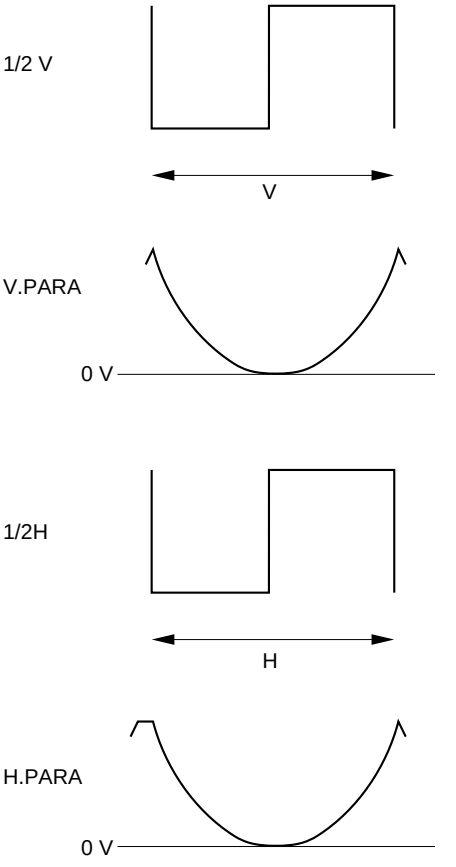


Fig. 10-2

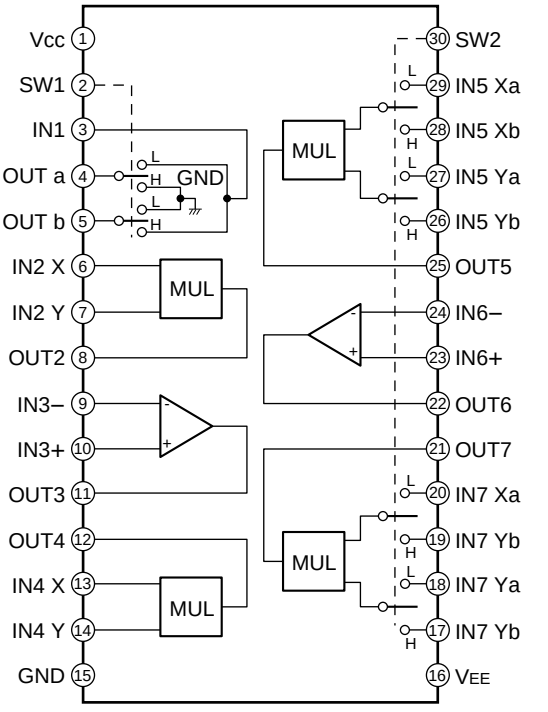


Fig. 10-3

10-2-1. MG.HD Circuit

The monostable multivibrator IC12 (1/2) is triggered at the falling edges of the AD.HD (12 V) pulses. The width of the output pulse is controlled by the current of the current mirror (Q4) circuit. The current of the current mirror (Q4) circuit is controlled proportionately to the MG.PHASE (H) by IC13 (1/2) and Q7, and the MG.P.W pulse with pulse width proportionate to the MG.PHASE (H) voltage is output.
The monostable multivibrator IC12 (2/2) is triggered at the falling edges of the AD.HD (12 V) pulses. The output pulse width is controlled by the current of Q10. The $\overline{Q}$ output of the monostable multibivrator IC12 (2/2) and the Q output of the monostable multivibrator IC12 (1/2) are rectified respectively, and compared as voltage by IC13 (2/2), and the current of Q10 is controlled so that the voltage difference becomes 0
As a result, the negative pulse with 1H-MG.P.W pulse width is output from the monostable multibivrator IC12 (2/2), to become the positive polarity MG.HD pulse with phase advanced by MG.P.W pulse from the rising and falling edges of the AD.HD (12 V) pulse.

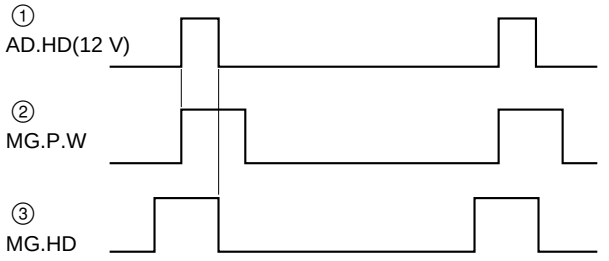


Fig. 10-4

10-2-2. Waveform Generation Circuit

Normally, the CRT horizontal direction focus voltage characteristics are of the parabola form, but in this unit, the characteristics of the center of the CRT and center between two ends are of the trapezoid (bathtub) shape near the voltage at the center. Therefore the H parabola waveform is processed to the bustub shape by the waveform generation circuit (IC17).
The H parabola waveform is input to Pins 26 and 28 of IC17. And multiplied. As the waveform is too flat if only multiplied, the multiplied waveform and H parabola waveform are added to the ope-amplifier (Pins 22 to 24 of IC17) and processed to the bustub shape waveform.

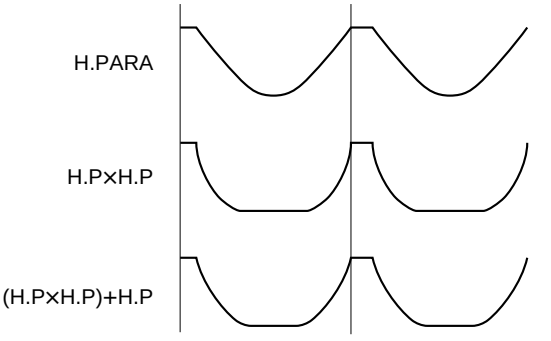


Fig. 10-5

The processed waveform is input to the multiplier composed of IC17 and IC4, input to the analog switcher to generate the waveform for “Zone 2 to Zone 9”.

10-3. D/A CONVERTER OUTPUT CIRCUIT

To operate the MG focus, 4 poles, and 6 poles using the remote commander, the waveform generated in the wave form generation circuit is adjusted by the D/A converter functioning as the electronic control, added, and output.
The waveforms controlled by IC100 to IC103, IC106 to IC108, IC111 to IC113, IC117 to IC119, IC123 to IC125, and IC129 to IC131 are added by IC105, IC110, IC115, IC116, IC121, IC122, IC127, IC128, and IC133, and output.
Refer to the section on the DD board for details on the operations of the D/A converter.

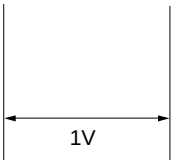
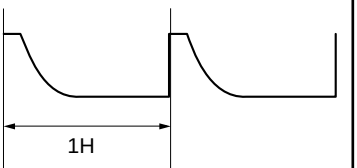
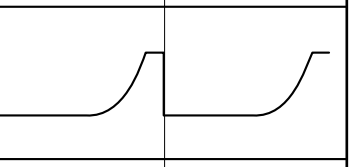
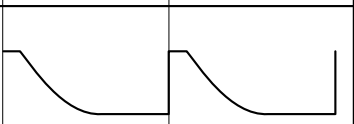
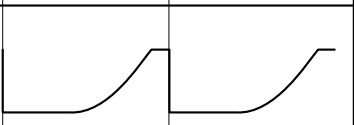
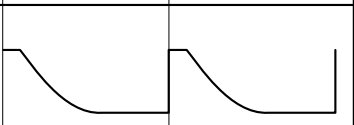
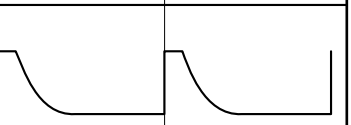
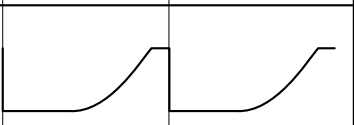
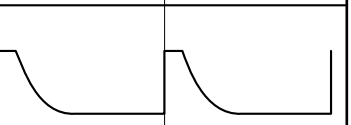
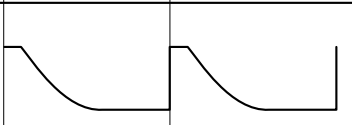
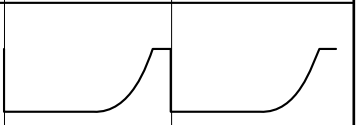
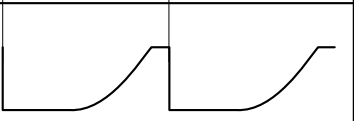
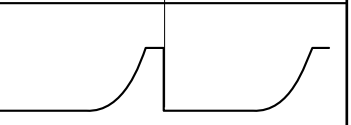
Functions	Signals	V period	H period
Zone 2	M. H. PARA L		
Zone 3	M. H. PARA R		
Zone 4	M. V. PARA T		
Zone 5	M. V. PARA B		
Zone 6	M. H. PARA L + M. V. PARA T		
Zone 7	M. H. PARA L + M. V. PARA B		
Zone 8	M. H. PARA R + M. V. PARA T		
Zone 9	M. H. PARA R + M. V. PARA B		

Table. 10-1

SECTION 11
DF BOARD

11-1. OUTLINE

The main functions of the DF board are as follows;
- Generation/control/output of vertical deflection waveform
- Control of 2-pole/4-pole voltage for MG focus

11-2. GENERATOR OF VERTICAL OUTPUT (VOUT) WAVEFORM

The vertical parabola (V.PARA) waveform and vertical sine (V.SIN) waveform of the vertical output (V out) is generated by the registration IC (IC3 : CXA1470AS). This IC also generates the vertical sawtooth (V.SAW) waveform, which is also generated in a different circuit because of the generation of pairing in the interlace during DRC operations.

The vertical sawtooth wave (V.SAW) generation circuit is composed of the mirror integration (IC1) circuit, level shift circuit, V.SIZE bias circuit (IC4), integration circuit (IC20), Q2, Q6, reset circuit (IC10), and analog switch (IC11). The monostable multivibrator (IC10) is triggered by the vertical trigger pulse (V.TRIG) to generate an approximately 200 µsec reset pulse (Fig. 11-1-①).

The reset pulse is input to Q2. When Q2 turns on, the C4 of the mirror integration circuit composed of IC1 (1/2) and C4 is short-circuited, and reset. When no more reset pulse is input, C4 is recharged by the constant current and a right-ascending sawtooth wave is output from IC1 (1/2). When the next reset pulse is input, the sawtooth wave is reset to 0 V.

As a result, 0 V is output constantly during the reset period and a sawtooth positive voltagewaveform is output during the trace period from Pin 1 of IC1 (1/2) (Fig. 11-1-②).

The sawtooth wave is supplied to the inverse input terminal of the ope-amplifier (IC1 : 2/2). The non-inverse input terminal of the ope-amplifier (IC1 : 2/2) is supplied with a voltage generated by adding or amplifying the V SIZE COARSE voltage and V SIZE FINE voltage at IC4, after which this voltage is subjected to waveform-inverting and level-shifting (Fig. 11-1-③). As a result, the voltage of the reset period is proportionate to the vertical size (V. SIZE) voltage, and during the trace period, a sawtooth wave changed from "+" to "−" voltage is generated. The sawtooth wave is then output as the vertical sawtooth (V.SAW) wave via the inverse buffer (IC2 : 2/2). The vertical sawtooth (V.SAW) wave is fixed at 0 V by the analog switcher (IC11) during the reset period (Fig 11-1-④) and input to the integration circuit (IC20).

The output of the integration circuit (IC20) is input to the mirror integration circuit (IC1) via R17/R18 to make a loop configuration (IC1→IC2→IC11→IC20). As a result, a vertical sawtooth (V.SAW) wave whose "+" and "−" peak voltages are equal and is proportionate to the vertical size voltage.

The vertical sawtooth (V.SAW) wave, vertical parabola (V.PARA) waveform generated in IC3, and vertical sine (V.SIN) waveform are level-adjusted and added by the electric volume of the D/A converter, and the vertical linearity (V.LIN) and S-shape corrected vertical output wave (Vout) are input to the vertical deflection output circuit.

For details on the D/A converter, refer to the DD board.

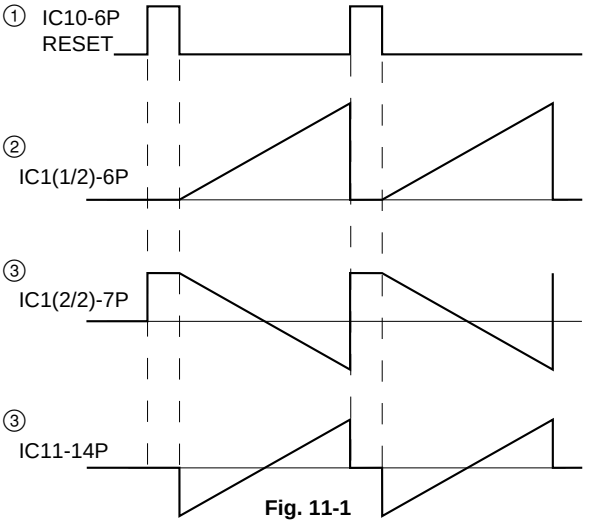


Fig. 11-1

11-3. VERTICAL DEFLECTION OUTPUT

The vertical deflection output circuit is composed of IC101, IC104, and IC106 (LA876NZA). As the circuits of the R, G, and B channels are the same, only that of the G channel is described below.
When the vertical output (V.OUT) waveform which has been level-adjusted by the D/A converter circuit is input to Pin 6 of IC104 as a current, as Pin 5 of IC104 is a GND terminal, the waveform shown in Fig. 11-2-C is fed back, and Pin 6 of IC104 is grounded. As a result, the current shown in Fig. 11-2-B is output from Pin 2 to generate the voltage waveform shown in Fig. 11-2-D. E is a pulse power supply which is output when errors of the input waveform (Fig. 11-2-C) are detected inside LA7876NZ, and the power voltage becomes triple by D106, C118, D107 and C119.

11-4. CHANGES IN VERTICAL POLARITY

The vertical polarity is changed using the relay.
When the switch (S2001) of the EC board is switched from NOR (SUB6 V) to INV (GND), the switching information is input to Pin A23 of the connector CN230, RY100, RY101, and RY102 are switched, and the direction of the current flowing to the vertical deflection york is inverted.

11-5. VERTICAL DEFLECTION STOP CIRCUIT (V.STOP)

The deflection pulse output from Pin 3 of IC101, IC104, and IC106 is waveform-shaped by Q100, Q103, and Q104, and the deflection output is monitored. As the circuit configuration of channels R, G, and B of the deflection output monitor is the same, only that of channel G is described in the following.
If C114 is not mounted, the pulse waveform shown in Fig. 11-2-E appears in the Q103 collector. When C114 is mounted, the waveform is integrated by C114 and the sawtooth waveform shown in Fig. 11-2-F appears. When an error occurs in the vertical deflection output, the pulse shown in Fig. 11-2-D is not output, and the Q103 collector becomes "+B". As a result, the capacitor is recharged as shown in the dotted lines in Fig. 11-2-F, the comparison voltage of Pin 5 of IC103 (µPC393G2) is exceeded, Pin 7 of IC103 becomes "High" level, and the vertical deflection stop (V.STOP) is detected.

In order to prevent malfunction when input signals are switched, the blanking is applied to the output of Pin 7 of IC103 through the buffer amplifier IC110. The vertical deflection stop (V.STOP) output is delayed by the time constant circuit composed of IC110, IC152, and R192. The vertical deflection state is monitored by the YA board.

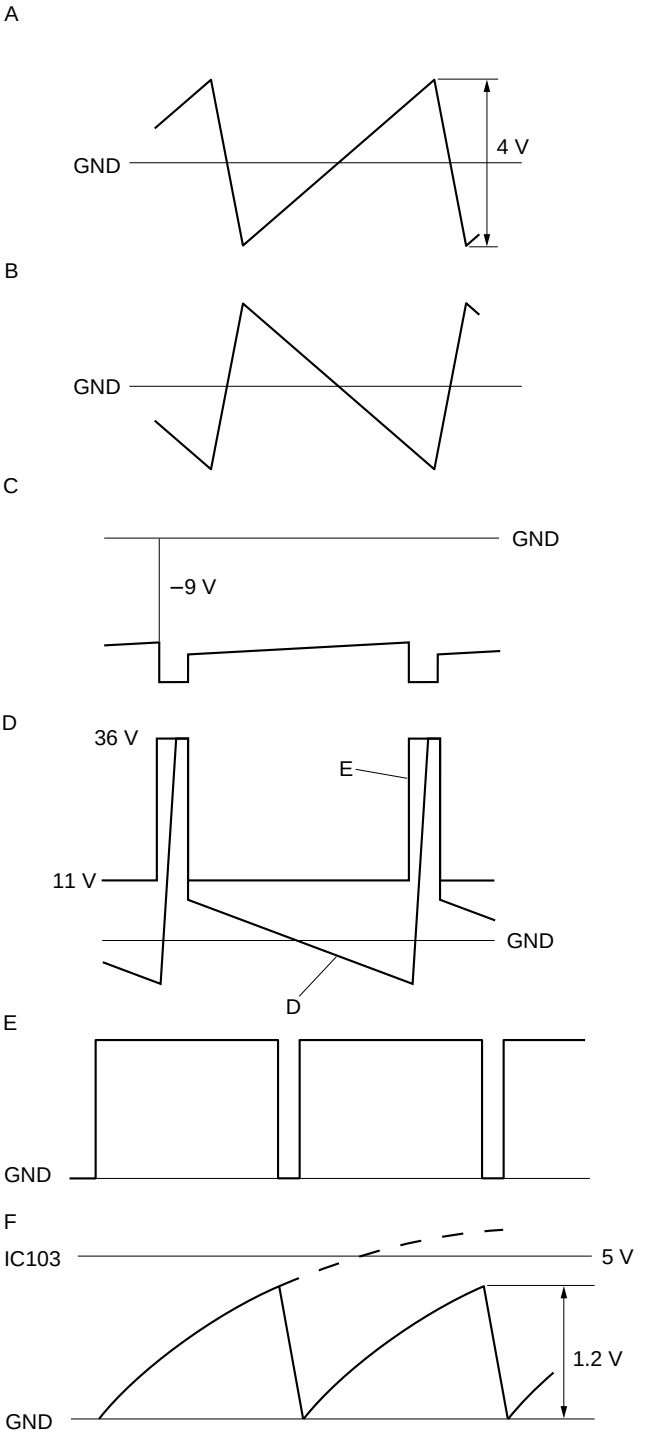


Fig. 11-2

11-6. 2-POLE/4-POLE OUTPUT CIRCUIT

The DF board is mounted with a controller and output of the 2-pole/4-pole correction circuit. As this unit is provided with 2PH/2PV and 4PH/4PV each for all the R, G, and B channels, 12 circuits are mounted, all of which have the same circuit configuration. In the following, only the green horizontal 2-pole (2PH) circuit is described.
The control signal of the green horizontal 2-pole is output from Pin 2 of the D/A converter IC209 by the DC voltage. The correction signal is voltage-divided by R232 and R242, and input to the 2-pole output circuit. The 2-pole output circuit is composed of an amplifier (composed of IC206 (2/2)) and buffer (composed of Q210 and Q212) to form a feedback loop. When the correction signal is input to Pin 3 of IC206 (non-inverse input), the current flowing to the 2-pole winding is converted to voltage by R238, and input to Pin 2 (inverse input) of IC206. As a result, the correction voltage signal is converted to current, and supplied to the 2-pole winding.

SECTION 12
E/EA/ED/PD/PE BOARDS

12-1. FV CONVERSION

Pins 2 of IC7 (µPC4558C) of the EA board is input with the horizontal keystone/pin cushion (H.KEY/PIN) signal from Pin 9 of CN750 and horizontal size (voltage = ±approx. 2.2 V dc) signal from Pin 10 and added. Furthermore, Pin 2 of IC7 is supplied with the reference power via R46 and R47.
This output is sent to the following 3 blocks.

1. To Pin 2 of IC8 (µPC4558C) via R18
   During the open loop, this is used as the main control unit.
2. To Pin 6 of IC7 via R36
   Compared with the horizontal size feedback signal and the error is input to Pin 2 of IC5 (µPC814C), amplified and integrated by R37, R30, and C7, and input to Pin 2 of IC8 via R38. Used to correct and control the error of the closed loop.
3. To Pin 4 of IC2 (MC1495BP) via IC1 (µPC4558C)
   Becomes the modulation waveform for H.KEY and H.PIN mudulation (PIN.MOD)

As the power supply voltage (PIN.MOD) used for horizontal deflection is nonlinear in respect to the horizontal frequency (fH), control by the above Step 1 and Step 2 is required.

(a) For the horizontal pin cushion and keystone modulation (PIN.MOD) voltage (H.KEY, etc.), the higher the horizontal frequency, the greater the amplitude value of the voltage (Δ PIN/MOD) must be set to.
Example
fH = 31.5 Hz : Δ PIN.MOD = 5 V
fH = 63.0 Hz : Δ PIN.MOD = 10 V

(b) When the horizontal frequency (fH) is low, as the consumption current of the horizontal output increases, the drop in voltage by R1, R65, and R69 cannot be ignored. Consequently, the characteristics of the deflection current are curbed from the results of (a) and (b).

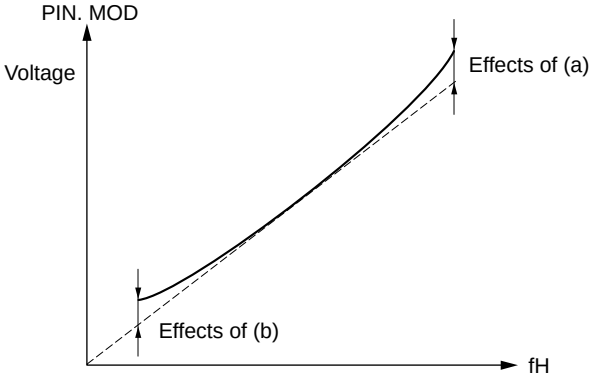


Fig. 12-1

The straight line in Fig. 12-1 is the curb when the deflection current is constant. If a feedback loop structure with a long time constant where load power supply→PIN.MOD→SIZE detection is adopted to realize this, the sudden change in the horizontal frequency (signal switching) cannot be dealt with.

In this unit, only the difference between the dotted line and real line in Fig. 12-1 can be used as the feedback. The dotted line is used for F/V conversion to control with the open loop. The open loop and close loop voltage input to Pin 2 of IC8 is integrated by R38 and C6, and Q3 is switched by the DC voltage generated via R19 by the DC voltage generated. As the drive pulse, a horizontal oscillation pulse sent from the DA board is input to Pin 4 of IC6 via R51, waveform-shaped, and supplied to Pin 7 of IC6. The pulse with a width of 5 µsec pulse (see Fig. 12-2) is output from Pin 7 of IC6 and supplied to the Q3 gate via C12. As a result, a horizontal size voltage and a pulse proportionate to the horizontal frequency (fH) are output from the Q3 drain.

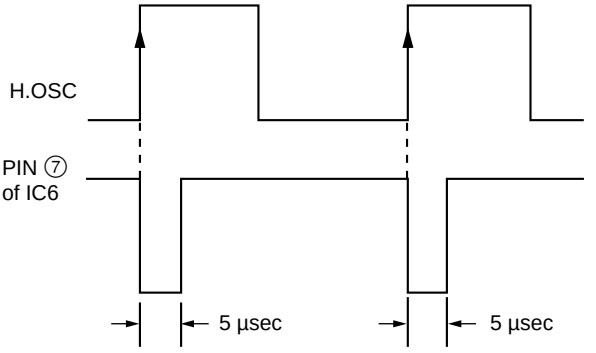


Fig. 12-2

The generated pulse is sent to the integrated circuit composed of R28, C9, R29, and C10 via the buffer IC5 (2/2), and output from Pin 71 of IC4 as the F-V conversion voltage. The appropriate TP1 voltage is as follows;

- fH = 15 kHz, H.SIZE : Min = 0.8 V / Max = 1.2 V
- fH = 31.5 kHz, H.SIZE : Min = 1.2 V / Max = 1.7 V
- fH = 64 kHz, H.SIZE : Min = 2.5 V / Max = 3.5 V
- fH = 106 kHz, H.SIZE : Min = 3.7 V / Max = 5.5 V
- fH = 150 kHz, H.SIZE : Min = 5.2 V / Max = 7.8 V

The F-V conversion voltage, Pin 7 of IC8 voltage, and negative power supply feedback voltage are added and sent to the PD board amounted with a load power circuit as the F-V voltage from Pin 7 of IC4. The current adding is DC matched with the load power circuit, and the load power voltage is controlled vt the F-V voltage.

12-2. PIN MOD

IC2 (MC1495BP) is a four quadrant multiplier. It constantly imposes modulation at the same rate for changes in the horizontal frequency (fH) and horizontal size (H. SIZE).
Fr instance, when the horizontal frequency (fH) is doubled, in order to keep the deflection current constant, the PIN MOD voltage must also be double.

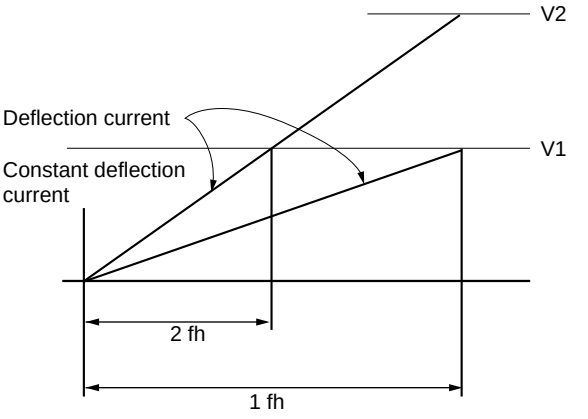
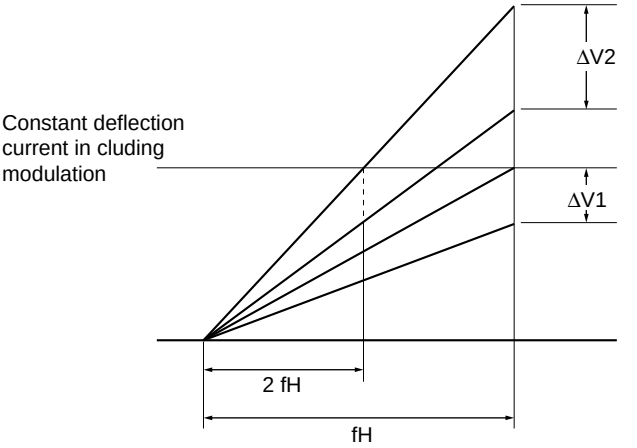


Fig. 12-3

The deflection current is proportionate to the pin cushion modulation (Pin MOD) voltage. As shown in Fig. 12-4, if only Δ V1 is modulated at a certain horizontal frequency (fH), to modulate at the same rate at double horizontal frequency (fH), there is a need to double the pin cushion modulation (PIN MOD) voltage as well. Consequently, the voltage for modulation must be proportionate to the frequency (fH) and horizontal size (H.SIZE).



ΔV2 = 2ΔV1

ΔV1 : Modulation voltage

Fig. 12-4

Pin 4 of IC2 (MC1495BP) is input with modulation waveform such as horizontal keystone (H.KEY) and horizontal pin cushion (H.PIN). Pin 9 of IC2 is input with the voltage proportionate to the PIN MOD OUT voltage which is then output from Pin 14. The output of Pin 14 of IC2 is amplified by IC3 (MC1436CP) and output as the PIN MOD signal from Pin 14 of CN750 via the buffer Q1 and Q2, and sent to the E board. The Pin MOD signal is cut by C42 and clamped to the potential of the negative power supply by D21. L8, L9, and L15 are filters for reducing the ripples of the negative power supply.
Q19 is a circuit which improves when the horizontal frequency (fH) is changed (from low to high).
The modulation waveform clamped to the negative power potential is input to Pin 3 of IC3 (MC1436CP1) buffer via R73. D28 to D31 shift the level of the clamp waveform by 4VF, to prevent the distortion of the peak of the PIN MOD signal. The power for IC3 is created from LOT on the PE board and approximately ±24 V is generated mainly around the PIN MOD voltage.
D26 and D27 prevent the latchup of IC3 when power is supplied. When power is supplied, if the signal input exceeds the power supply voltage due to the difference in timing between the signal input to IC3 and start of the power supply voltage, IC3 is latched up. The modulation waveform output from Pin 1 of IC3 is input to the Q17 and Q18 gates via R57 and R58. Q17 and Q18 are a FET for the PIN MOD output. D15 to D20 are used for protecting Q17 and Q18. R1, R65, and R69 prevents the parabola voltage generated between the ends of the S-shape correction signal from affecting the PIN MOD circuit side.

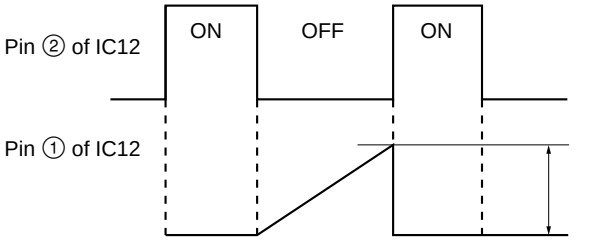
12-3. HORIZONTAL DRIVE (H DRIVE)

The main circuits of the horizontal drive are as follows.

12-3-1. Horizontal Drive Variable Power Supply
12-3-2. ON-ON Horizontal Drive Circuit
12-3-3. IB2 Constant Circuit

12-3-1. Horizontal Drive Variable Power Supply

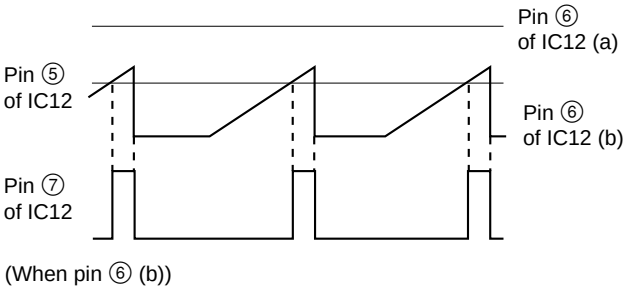
When the horizontal size changes suddenly from minimum to maximum, or if the hfe characteristics of the horizontal output transistor are inconsistent, in order for the horizontal drive circuit is always driven optimumly, a variable voltage for driving at 60 V to 150 V will be required. However, as the voltage supplied to the E board is 115 V, voltage above 115 V is generated using a boosting type switching regulator.
When the drive voltage is below 115 V, the series regulator composed of Q1009 and Q1012 operates. The series regulator is controlled by the 1B2 constant circuit described later. When the series regulator is operating, Q1011 goes off.
When drive voltage above 115 V is required, the switching regulator starts operating.
The output of the horizontal oscillation circuit of the EA board is input to Pin 2 of IC12 (µPC393C) via R109 and the Q11/Q19 buffer.



Constant amplitude at all times regardless of fH = Approx. 4 V p-p

Fig. 12-5

Pin 1 of IC12 (μPC393C) is Low level and therefore 0 V during the ON period shown in Fig. 12-5. During the OFF period, Pin 1 of IC12 is open, and therefore C38 is discharged via Q13. During the next ON period, the voltage recharged to C38 is discharged via R113.
Since the amplitude is made constant all the time, Q20 and Q21 are compared and the constant power supply Q13 is controlled. Q20 (emitter follower) is peak-rectified, to configure a comparison circuit with Q21. As the time constant of R118 and C39 are sufficiently long for the input signal, it functions only as a diode between the Q20 base and emitter, and operates as a peak rectifier by comparing the peak of the Q20 base voltage and reference voltage of the Q21 base and feeding back the comparison results (difference) to the Q13 base. As the time constant by R89 and C29 is also long, the Q13 base is more or less a DC.
Consequently, the peak voltage of the Q13 collector is also maintained at a constant.
The output is input to Pin 5 of IC12, and the DC voltage output from the IB2 constant circuit described later is input to Pin 6 of IC12.
The relation between the output waveform of Pin 7 of IC12 and Pins 5 and 6 is shown in Fig. 12-6.



(When pin ⑥ (b))

Fig. 12-6

When the voltage of Pin 6 of IC12 is higher than that of Pin 5, Pin 7 of IC12 will remain Low level all the time. When lower, Pin 7 will become High level. The output of Pin 7 of IC12 is passed through the buffer (Q9 and Q22) and sent to the ED board as the drive control pulse from Pin 4 of CN751. The drive control pulse from supplied from the ED board is input to the Q1011 gate via C1012 and R1036. Q1011 is a FET for the switching regulator. When Q1011 starts operating, Q1009 and Q1012 remain completely ON.

The following describes the basic operations of the boosting switching regulator.

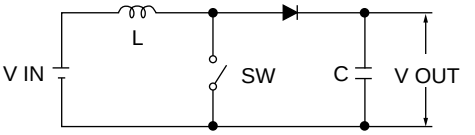


Fig. 12-7

(1) When the switch is OFF, VOUT = VIN.
(2) When the switch is ON, the energy for the time it is ON will be charged to the inductor (L).
(3) When the switch goes OFF the next time, the energy accumulated in the inductor (L) will be superimposed to the input voltage V1. This relation can be expressed by the following equation;

$$V_{OUT} = \frac{T_{ON} + T_{OFF}}{T_{OFF}} V_{IN}$$

Consequently, because Q1011 controls the ON period, a voltage higher than 115 V can be obtained.
This voltage is used as a driving voltage.

12-3-2. ON-ON Horizontal Drive Circuit

This unit adopts a ON-ON type horizontal drive circuit. When the capacitance of C1010 is large, IB1 is maintained at a constant in respect to the changes in the horizontal frequency.
With the ON-ON method, current is also supplied to the secondary side when current is supplied to the primary side of the horizontal drive transformer (HDT) to turn ON the output transistor.
The horizontal oscillation signal is input to the Q1013 gate via the buffer (Q11 and Q19) of the EA board. D1013 is a clamp diode. D1007 is a diode which turns OFF Q1013 as quickly as possible. D1008, D1009, D1010, and D1014 are protection diodes.

The horizontal drive voltage is as shown in Fig. 12-8. During the ON period, current is supplied from Q1007 and Q1010 and during the OFF period, current is absorbed by Q1013.

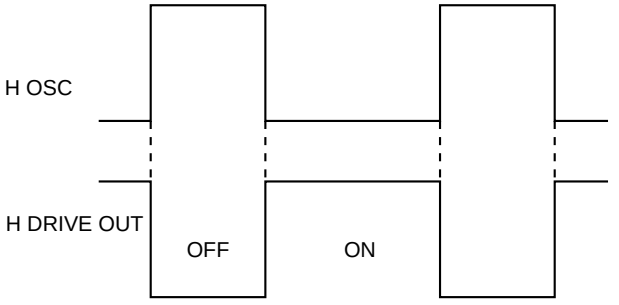


Fig. 12-8

12-3-3. IB2 Constant Circuit

The following describes the IB2 detection circuit;
The horizontal drive transformer (T1 : HBT) is mounted to the E board. The base current of the horizontal output transistor is supplied to the secondary side of T1. But as it is proportionate to the currents of the primary and secondary sides of T1, the current flowing to the primary side of T1 is detected as IB2. The detection of the current is performed by L1007, R1027, R1031, and R1033. In the following, operations are described assuming that L1007 is not used.

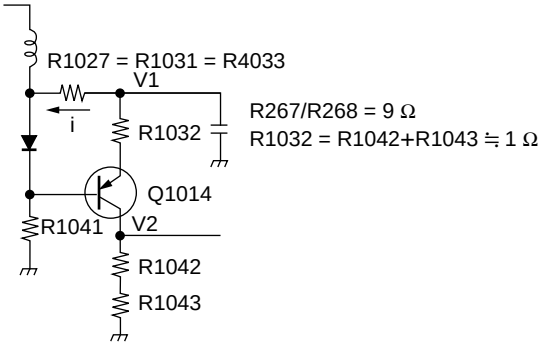


Fig. 12-9

When the voltage and current are set as shown in Fig. 12-9, the Q1014 base voltage becomes V1-9 i-0.6 and the Q1014 emitter voltage becomes V1-9 i. Consequently, the current flowing to R1032 becomes 9/1000 × i, and this current flows to R1042 and R1043.
Consequently, V2 becomes as follows.

$$V2 = 509 \times \frac{9}{1000} i \fallingdotseq \frac{9}{2} i$$

R1027//R1031//R1033 = 9 Ω
R1032 = 1 kΩ
R1042 + R1043 = 509 Ω

The Q1014 collector is output with the voltage proportionate to IB2. D1006 is a diode for compensating the temperature of the voltage (V_{BE}) between the Q1014 base and emitter.
The circuit actually used is L1007, which sets the frequency characteristics for the detector, and corrects the optimum IB2 point according to the difference in the horizontal frequency (fH). This voltage is sent to the EA board as the IB2 DET signal, and input to the Q17 base via R104.
Q17 and Q18 are differential amplifiers. The Q18 base is input with the voltage obtained by voltage-dividing the horizontal pulse from the secondary side of the horizontal output transistor (HOT) at R96, R105, and R123. The horizontal pulse contains the horizontal output transistor hfe inconsistencies and horizontal size inconsistencies.

Consequently, by comparing IB2 and horizontal pulse and maintaining the relation of both at a constant at all times, the horizontal output circuit can be driven at the optimum state all the time.
The comparison is performed as follows.
If time constants of R122 and C40 are sufficiently great for the input signal of the Q17 and Q18 bases, the Q17 and Q18 base and emitter can be taken as a normal direction diode. This means that the IB2 detection voltage peak value and horizontal pulse peak value is DC-compared.
If the horizontal pulse is greater than the IB2 detection voltage, the Q17 V_{BE} decreases, the Q17 collector current decreases, the Q12 base voltage increases, the Q12 emitter current decreases, and the Q12 collector voltage decreases. The Q12 collector output is supplied to Pin 6 of IC12 and the Q15 base.
IC12 (2/2) is the IC for the horizontal drive circuit mentioned earlier and for variable power supply control. Q15 and Q16 compose the differential amplifier. When the Q15 base voltage decreases, the Q15 emitter current decreases, the Q15 collector voltage increases, the Q15 collector output is supplied to the series regulator (Q1009, Q1012) base of the ED board via R89, the output voltage of the series regulator increases, the voltage amplitude of the primary side of the horizontal output driver increases, and IB2 increases.
When the horizontal pulse is smaller than the IB2 detection voltage, operations are opposite to the above, the voltage amplitude of the primary side of the horizontal drive transistor (HDT) decreases and IB2 also decreases.

12-4. HORIZONTAL SIZE FEEDBACK, HORIZONTAL SIZE MAXIMUM/ MINIMUM PROTECTOR, LINE OUTPUT TRANSFORMER, +B LINE CURRENT PROTECTOR

The horizontal size feedback circuit feeds back the voltage obtained by peak-rectifying the horizontal pulse of the secondary side of the horizontal output transformer (HOT) at D6/C16 to Pin 6 of IC107 (µPC4558C) as the detection voltage.

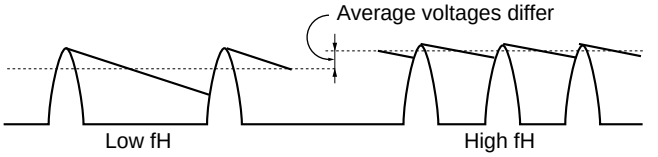


Fig. 12-10

Although the Q8 output has the same level as the horizontal pulse, the average voltage level changes according to the frequency difference. When the discharge time is long, the voltage difference disappears, but as the discharge time is determined by the horizontal frequency (fH), theoretically, this method is not possible. In this unit, the discharge current is controlled according to the horizontal frequency (fH) to maintain the voltage at a consistent level. When the horizontal frequency (fH) is low, the discharge current is made small. When the horizontal frequency is high, the discharge current is made high. The Q8 emitter is connected to the PIN MOD output circuit via R70, R74, R76, and R78. The absolute voltage of the PIN MOD circuit becomes small when the horizontal frequency (fH) is low and becomes large when high.

Example :

- fH = 15 kHz : PIN MOD output = −20 V
- fH = 150 kHz : PIN MOD output = −150 V

The Q8 collector current (discharge current) becomes as follows;

$$Ic = \frac{-0.6 - \text{PIN.MOD output}}{\text{R273 to R276}}$$

Note : The PIN MOD output is − voltage.

As indicated above, when the PIN MOD output is high (absolute value is small), the collector current becomes small. When low (absolute value is large), the collector current becomes large. Consequently, the average voltage in which the horizontal pulse level is equal becomes constant regardless of the relation with the horizontal frequency (fH).
The voltage detected is fed back to Pin 6 of IC7 (μPC4558C), the input signal is compared with the feed back signal, and the comparison difference is supplied to IC8 (μPC4558C) (1/2) via IC5 (1/2) and R38.

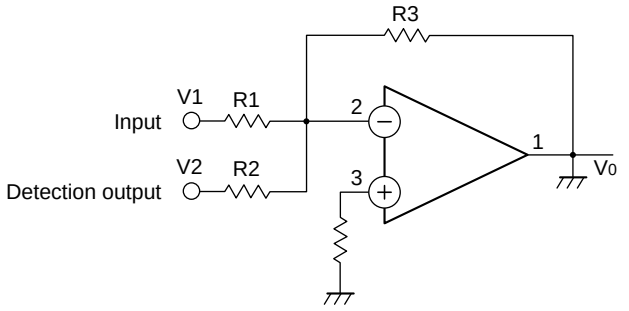


Fig. 12-11

R3/R1 and R3/R2 are constants, ignore them and obtain the output from V1 and V2.
By reversing the polarities of V1 and V2, the output V0 when |V1| = |V2| becomes 0. When not equal |V1| ≠ |V2|, the voltage of |V1−V2| is expressed by the output V0 as the difference. This difference is equivalent to the loss of R1, R65, and R69 when the horizontal frequency (fH) is low, and becomes the voltage equivalent to the PIN MOD when the horizontal frequency (fH) is high.

The following describes the horizontal size maximum and minimum protector.
6. 85 V is supplied to Pin 3 of IC9. Pin 6 of IC9 is supplied with 1.7 V. As the horizontal size detection voltage is input to Pins 2 and 5 of IC9, when the detection voltage is above 6.85 V (when the horizontal size is excessively large), or when the detection voltage is below 1.7 V (when the horizontal size is excessively small), Pins 1 and 7 of IC9 become Low level. This output is supplied to Pin 13 of IC6 (horizontal stop circuit : HD14538BP) of the EA board. When Pin 1 or 7 of IC9 becomes Low level, the horizontal stop circuit operates and the power supply goes off.

12-5. HORIZONTAL DRIVE OUTPUT CIRCUIT/HORIZONTAL STOP CIRCUIT

The horizontal drive output signal is generated as follows; The negative polarity horizontal pulse output from Pin 11 of T2 (horizontal output transformer : HOT) of the E board is supplied to the EA board and the DC components are cut by C25. Next, R70, D9, and L1 are imposed with bias, switched by Q7, and output via buffers Q4 and Q6. To make the pulse width of the horizontal drive pulse as wide as possible, the following process is performed.
As the horizontal pulse contains ringing components, when sliced normally, the ringing components become glitch. If the slice level is dropped to eliminate the ringing effects, the horizontal drive pulse width becomes narrow.

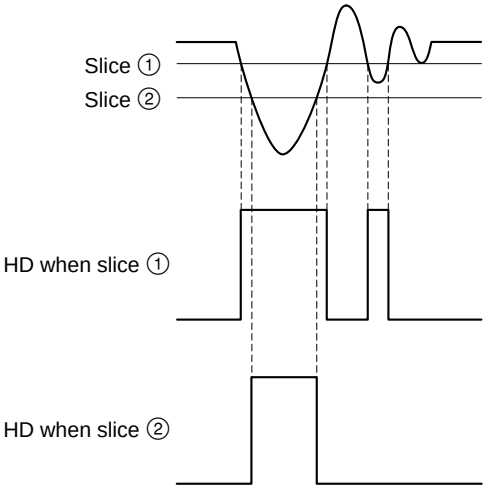


Fig. 12-12

This circuit generates the horizontal drive pulse with large pulse width and no glitch using L1.
If an inductor (L) is inserted at the cathode side of the diode, the electric charge recharged to the capacitor (c) during the OFF period of the diode becomes the following waveform because the rear edge rises due to the inability of recharging immediately when the diode turns ON.

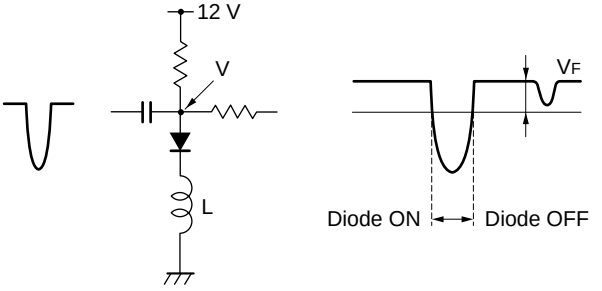


Fig. 12-13

Horizontal Stop Circuit/EA Board

The B terminal of the monostable multivibrator (IC6) is input with the horizontal drive (HD) signal. When the external CR time constant is set longer than the horizontal period (100 kΩ × 100 pF = 100 ms), as long as the horizontal drive signal is input to the B terminal, the Q output terminal remains the High level. The Q output is input to the Q5 base via D8. Consequently, normally Q5 is in the ON state. But when the horizontal stop terminal becomes High, the power supply goes off. The clear terminal is supplied with the IC9 output. The IC9 output is set to Low level by the horizontal size maximum and minimum protector circuit, and the output (Q) of IC6 also becomes Low level and the power supply goes off. C18 sets the Q5 base to the High level all the time when the power is turned ON.

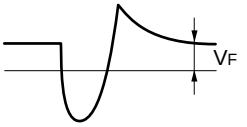


Fig. 12-14

12-6. HORIZONTAL CENTERING CIRCUIT

As the horizontal centering circuit structure is the same for R, G, and B, only that of channel R is described in the following. R5, R8, R10, R13, R15, and R17 of the E board is a horizontal centering current detection resistor. The both ends voltage of these resistors is fed back to IC1010 (1/2) (µPC4558G2) of the ED board and the horizontal centering current is converted to voltage. In IC1010 (2/2) it is compared with the horizontal centering control voltage so that a constant centering current flows all the time. C1027 and C1028 are capacitors for preventing oscillation. Q2 and Q5 are FETs for driving.

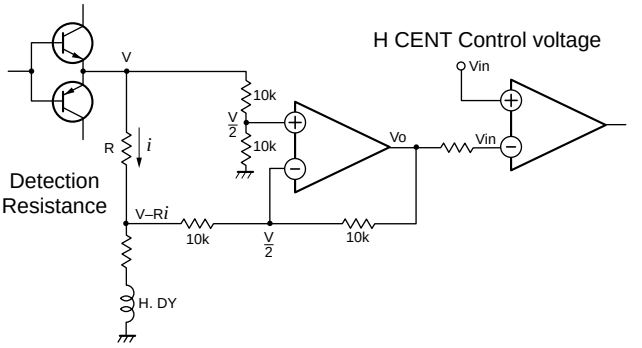


Fig. 12-15

$$V\text{-}Ri = \frac{V}{2} = Vo = Vin,\ Ri = \frac{V}{2}$$

$$Vin = Ri$$

$$\therefore i = \frac{V_{IN}}{R}$$

12-7. HORIZONTAL OUTPUT CIRCUIT

Q22 and Q23 are main horizontal outputs. C33, C43, and C44 are resonance capacitors. D33 and D34 are damper diodes.
In this circuit, horizontal centering power is supplied to the main deflection york without floating the power for the horizontal centering by using the minus voltage for the PIN MOD power supply.
D32, C45, R80, R82, R84, and R86 compose a pulse stopper circuit. They prevent the collector output level of the horizontal output transistor from becoming high due to discharge, etc., to prevent damage of the horizontal output.

12-8. HORIZONTAL LINEARITY CORRECTION CIRCUIT

Horizontal linearity tends to shrink to the right part due to the effects of the Vcc saturation voltage of the horizontal output transistor. As the deflection current remains the same even if the frequency changes, the Vcc saturation voltage of the horizontal output transistor is constant. The absolute minus power supply of the horizontal output circuit increases as the frequency increases. Therefore the rate of Vcc saturation voltage of the horizontal output transistor governing the minus power supply when the frequency is low is large compared to when the frequency is high. This means that the lower the frequency, the more shrinked the right part.
To perform correction only with the sub deflection york (SUB DY), the correction waveform becomes the horizontal parabola wave, heat generated by the IC for sub output (SUB OUT) increases, as does the power consumption.
Part of the correction of the horizontal linearity (H.LIN) is performed by the horizontal linearity coil (HLC).
The horizontal linearity coil (HLC) is a saturable inductance with a large inductance on the left side of the screen and a small inductance on the right side.

12-9. HV IMAGE BENDING CORRECTION CIRCUIT

When the high voltage changes, the electric filed in the CRT changes. As a result, even if the same deflection power is applied. When the high voltage is high, the screen size becomes small, when the high voltage is low, the screen size becomes big. This appears in the form of high voltage image bending.
To correct high voltage image bending, in this unit, the high voltage value detected by the HV detection circuit is returned to the deflection circuit to control it to the deflection size corresponding to the high voltage value.
The detection of the high voltage value is performed by the PA board by the same detection circuit (IC101 (1/2) : TL082CP) as the HV regulator. The dc components of the detected voltage (HV DET) are cut, amplified by IC302 (1/2) (µPC4558C) and input to IC1 of the EA board for the demodulation. In IC1, the voltage (modulation components) is added to the horizontal keystone and pin cushion (H.KEY/PIN) signal, and processed for horizontal size modulation in the vertical period.

12-10. LENS PROTECTOR (PD BARD)

Removing the lens with the power on will irradiate X ray above the reference value from the CRT screen, and as a result have adverse effects the human body.
For this reason, the protector is made to function when the lens is removed as shown in Fig. 12-16 and turn off the power. Normally, the lead wire from the lens protector is fixed to the screw fixing the lens, and the potential of the lead wire terminal is grounded. Even if the R,G,B screw loosens, or drops, the Q520 base becomes High level, Q529 turns ON, Q517 goes off, and the protector operations.

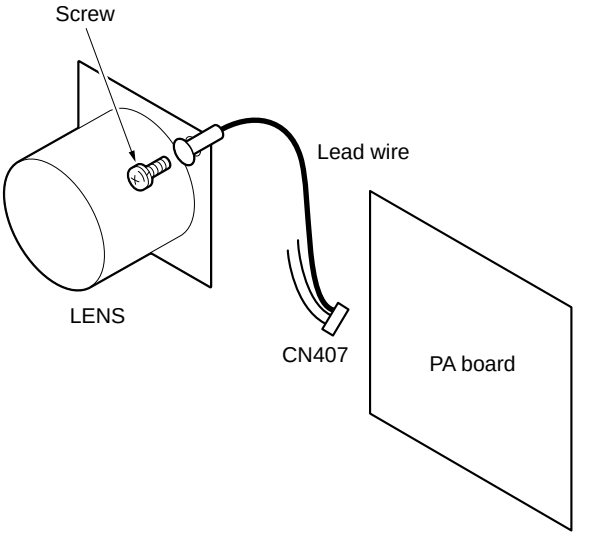


Fig. 12-16

12-11. LOT (LINE OUTPUT TRANSFORMER) CIRCUIT (PE CIRCUIT)

In the LOT circuit, the voltage used for horizontal deflection (E board), power supply voltage of the video output, and heater and G2 voltage are generated by the LOT (Line Output Transformer).
In the PE board, the approximately 15 kHz internal oscillation (INT OSC) signal sent from the IC503 (MC14572UB) of the PD board is supplied. Q504 is input with the internal oscillation signal as the drive pulse. Q504 is a transistor for the pre-driving. The Q504 output drives Q500 via the drive transformer T500. The Q504 output drives Q500 via the drive transformer T500 and switches Q500. Using the resonance pulse of the primary side inductor (L) and capacitor (C515) of LOT, the voltages for the secondary side of the LOT are generated. Q503 is a 115 V line current protector circuit. R500 is a detection resistor. The operating point of Q503 is set at 0.6 V = 1.5 Ω xi when Q502 turns ON.
Consequently, the current is I = 400 mA. When excessive current flows during malfunctions, Q502 turns ON, Q503 goes off, and High level is sent to the YA board to protect the LOT.

12-11-1. Minus Power Supply (PD Board)

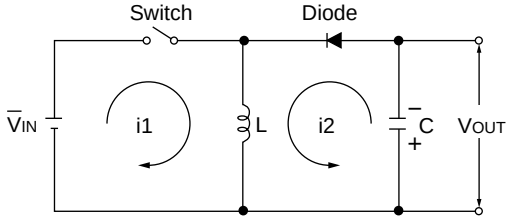


Fig. 12-17

The PD board is input with the voltage obtained by F-V converting the horizontal deflection frequency in the EA board. The converted voltage is input to Pin 1 of the switching regulator IC507 (μPC1394C) via R613. IC507 compares the voltage of Pin1 and that of Pin 14, and the error components are output from Pin 13. The error output is input to Pin 12 of IC507 via the filter composed of R599 and C544. Taking the 63 kHz internal oscillation signal (INT OSC 2) input to Pin 10 of IC507 from Pin 11 of IC507 as the trigger, the sawtooth wave is output. The voltage of Pin 12 of IC507 and the sawtooth wave of Pin 11 are compared, and the results are output from Pin 7. By changing the duty ratio of the output waveform of Pin 7, the output voltage of the minus power supply can be controlled.

The pulse output from Pin 7 is switched by Q530, and input to Pin 5 of T502 via the buffer Q528 and Q529. Q526 is switched by the pulse from T502.
The load decreases when the power is turned off. As the output of the minus (negative) power supply increases, switching is stopped when +12 V is dropped by Q525. Q527 prevents Pin 1 of IC507 from becoming minus voltage when the power is ON. R607 and R608 are resistors for detecting current. When excessive current flows due to abnormal load, switching is stopped by IC507.

The principle of the polarity inverse type switching regulator is as follows;

(1) When the switch is ON (T_{ON}) for a certain period, i1 flows to the inductor (L), and at this time, the changes in the current become as follows;

$$V_{IN} = L \times \frac{di}{Dt} \quad di = \frac{V_{IN}}{L} \, dt$$

$$i1 = \frac{V_{IN} \bullet T_{ON}}{L}$$

(2) Next, when the switch goes OFF (T_{OFF}), the diode turns ON again, i2 flows, and the energy accumulated in the inductor (L) is transferred to the capacitor (c).
The changes in current are as follows;

$$i2 = \frac{V_{OUT} \bullet T_{OFF}}{L}$$

(3) As changes in the constant state are equivalent, i1 = i2.

$$\frac{V_{IN} \bullet T_{ON}}{L} = \frac{V_{OUT} \bullet T_{OFF}}{L} \quad \therefore V_{OUT} = \frac{V_{ON}}{T_{OFF}}$$

12-11-2. G2 Regulator Circuit (PE Board)

In this unit, the brightness of the screen background can be adjusted by varying the voltage of the CRT screen (G2). In the G2 regulator circuit, the G2 control voltage supplied from the YA board can be varied independently for R, G, and B.

The G2 regulator circuit has one circuit each for the R, G, and B (total 3 circuits).
The following describes the circuit for R (red).
The G2 control (R) voltage supplied from the YA board is input to the inverse amplifier (IC504 : μPC4558C) via R528. In the inverse amplifier, the G2 control voltage is inverse-amplified, supplied to the buffer Q510 to drive Q509 (G2 output transistor). Using the primary side pulse (G500 collector pulse) of the LOT as the power supply of G2, the pulse is rectified to DC by R518, D511, and C521 to generate approximately 1000 V. Q511 of the Q509 emitter is a transistor which is operated to set the G2 voltage to 0 V rapidly. The Q509 base is connected to a G2 hold down circuit when the horizontal and vertical deflection composed of D514, D515, and D508 is stopped and the ON/OFF spot killer circuit which decreases G2 when the G2 hold down circuit and the 12 V line is raised and fallen, it serves to protect the CRT screen from sticking.

12-11-3. FAN Circuit (PE Board)

This unit controls the rotation of the fan motor by detecting the temperature. Example;
When the temperature is below 25 C :
Fan motor voltage = Approx. 10.5 V
When the temperature is above 49 C :
Fan motor voltage = Approx. 13.5 V

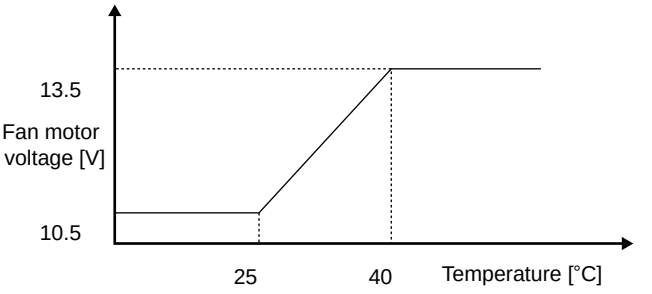


Fig. 12-18

IC2 is a temperature sensor. The output voltage of the temperature sensor changes lineally against the temperature. Consequently, the voltage of the fan motor changes as shown in the figure above in the range from 25 C to 40 C.
The ideal diode circuit is composed of IC3 (2/2) and D4. If the input (Vin) is a minus voltage, the output (Vout) becomes 0V. If it is a plus voltage, Vin = Vout, the output voltage of this circuit is input to IC6 (1/2) and the voltage of the fan motor is controlled.
IC6 (1/2), Q3, and Q5 is a series regulator circuit. The fan motor voltage is voltage-divided, fed back to Pin 3 of IC6 to generate the difference with the input voltage is input to Pin 1 of IC6. The base current of Q5 is controlled by the difference voltage to maintain the fan motor voltage at a constant.

SECTION 13
EBQ/EBH BOARD

13-1. OUTLINE

The EBQ board is mounted with an AQP (Axis Quadruple) circuit for correcting the distortion of the beam spot in the vertical direction of the surrounding area, and a DQP (Diagonal Quadruple) circuit and a DHP (Diagonal Hexaple) circuit for correcting the beam spot in the diagonal direction of the surrounding area.
The EBH board is mounted with an AHP (Axis Hexaple) circuit for correcting the distortion of the triangular beam spot in the surrounding area and center. As both boards have the same circuit configuration, only the EQB board will be described below.
The EBQ board is mounted with R, G, B output circuits (6 each) for supplying the correction current to the AQP and DQP windings in the focus magnet. IC200 incorporates an AQP amplifier for R, G, and B while IC300 incorporates an DQP amplifier for R, G, and B.
In the following, the green AQP circuit is described.

13-2. GREEN AQP CIRCUIT

The AQP correction signal input from CN131 is voltage-divided, noise-eliminated, by R202, R203, and C201, and input to Pin 6 of IC200. Pins 6, (non-inverse input), 7 (inverse input), and 20 (output) of IC200 form a type of ope-amplifier. The current flowing to the AQP winding is converted to voltage by R212, this voltage is input to Pin 7 to form a feedback loop, and the input voltage waveform is converted to the current waveform, and supplied to the AQP winding.

13-3. EBQ PROTECTION CIRCUIT

In the EBQ board, ±25 V is used as power. When current over 1A is supplied to the power supply due to some reason, the power supply automatically goes off. The current flowing to the power supply is detected by R105 and R108. When current above 1A is supplied to the power supply, Q100 and Q101 turn ON. When Q100 and Q101 turn ON, the comparator IC100 (1/2) input becomes “Low” level, and IC100 (2/2) output becomes “High”, and the power of this unit goes off.

SECTION 14
EBR, EBG, EBB, EBA, & EBC BOARDS

14-1. OUTLINE

The EBR, EBG, and EBB boards, and these sub-boards (EBA board and EBC board) are composed of horizontal and vertical magnet focus output circuits. As these boards have the same circuit configuration, the following description applies to all.

14-2. VERTICAL MAGNET FOCUS OUTPUT CIRCUIT

The vertical period parabola signal input from CN150 is converted to current waveform by the vertical magnet (V.MG) output circuit composed of the error amplifier IC252 (1/2) and IC253, and supplied to the vertical winding of the focus magnet.

14-3. HORIZONTAL MAGNET FOCUS OUTPUT CIRCUIT

The horizontal period parabola signal input from CN150 is sent to the EBC board. The parabola signal is level-shifted and gain-adjusted by IC500 in the EBC board (1/2), and input to the limiter circuit composed of Q500, Q501, Q502, and Q503 via the inverse amplifier IC500 (2/2). The limiter circuit imposes limit so that no excessive current is supplied to the horizontal winding of the focus magnet. Q500 and Q501 limit the plus side while Q502 and Q503 limit the minus side. The limited signal is input to the horizontal magnet focus output circuit. The horizontal magnet focus output circuit is composed of IC501 of the EBC board and amplifier (Q204, Q205) of the EBG board, and buffer (Q206, Q207). It inputs the input waveform for correction to Pin 2 of IC501, and inputs the current waveform flowing to the horizontal winding of Pin 3 to form a feedback loop. As a result, the input parabola voltage waveform is converted to current waveform, and parabola current is supplied to the horizontal winding.

14-4. PULSE POWER SUPPLY CIRCUIT

The horizontal magnet focus output circuit has a large power consumption, and therefore when the horizontal frequency (fH) is below 55 kHz, only ± 15 V is used as the power supply. When above 55 kHz, the output voltage waveform is checked, and +15 V is used as the power supply when below 10 V (−15 V when above −10 V). When above 10 V, the power supply voltage is switched so that the power supply becomes +50 V (−50 V when below −10 V).

The following describes operations when the power supply is the plus voltage.

The EBA board is supplied with the output waveform from the horizontal magnet focus output circuit. The waveform supplied is frequency-divided, and input to the comparator IC420. The comparator determines if the level of the waveform is above 10 V or below 10 V, and turns ON and OFF the power switching circuit of the EBG board. When the horizontal frequency (fH) is below 55 kHz, Q421 turns ON, and Q202 goes OFF.

SECTION 15
PA BOARD

15-1. INTERNAL OSCILLATION CIRCUIT (VCO)

The high voltage circuit of this unit is a unique asynchronous VCO (Voltage Controlled Oscillator) circuit. It is compatible with the wide-range multi-scan. The VCO (Voltage Controlled Oscillator) circuit is composed of IC152 and the oscillation frequency changes according to the changes of the high voltage load. The oscillation frequency becomes high when the high voltage load is light (all black signal) and becomes low when the high voltage load is heavy (all white signal, etc.). The oscillation frequency is controlled by the input voltage of Pin 13, and the 50 % duty rectangular waveform is output from Pin 8. RV150 is a VCO offset adjustment control. When the control voltage of Pin 13 is 2.00 V, it adjusts the output frequency to 54.5 kHz.
The oscillation output is input to Pin 2 of the monostable multivibrator IC153 and a high voltage drive pulse is generated with the off period (approx. 10 µsec.) by the time constants of R158 and C157. The high voltage drive pulse is input to the photocoupler PH500 via Q152 and Q155. The photocoupler PH500 electrically insulates the drive block (high voltage generation circuit) in the later stage with the circuit in the previous stage.

15-2. HIGH VOLTAGE GENERATION CIRCUIT

The high voltage drive pulse output from Pin 6 of PH500 is passed through the buffer (Q500, Q501) and amplified by Q502. The amplified pulse is then passed through Q503 and Q504, Q505 and Q506, and Q507 and Q508 to cut DC components, input to the three FBT comparator gate terminal composed of FET to switch the FET.
The basic structure of the high voltage generation circuit is the same as the conventional LC resonance circuit. Q600, Q601, and Q602 composes a converter by FET and D609 and D610 is a damper diode. C607 and C608 is a resonance capacitor. L601, L602, L603, and L604 compose a dummy inductor, while C610 and C611 compose a capacitor for S-shape correction.
The inductance of the dummy inductor is 420 µH. As four dummy inductors (L601, L602, L603, and L604) are parallel-connected, the inductance is about 105 µH. The inductance of the flyback transformer (FBT) is 965 µH. To produce high output, four are parallel-connected to produce about 241 µH in total. The total inductance of the resonance circuits is about 73 µH . Two 16000Pf resonance capacitors are parallel-connected, and the capacitance is 32000 pF.
The high voltage circuit switches the inductance (L) and capacitance (c) using the converter, and inputs the approximately 1 kV resonance pulse (Vcp) generated at that time to the flyback transformer (FBT). This pulse is then boosted by 10 times at the secondary side to obtain the high voltage. This resonance pulse (Vcp) is determined by the inductance (L) of the resonance circuit, capacitance (C), power supply voltage (E), and switching frequency (fH) as shown below.

Equation 1)

$$Vcp = \frac{E\ (1/fH - Tw)}{2\sqrt{LC}}$$

However

Equation 2)

$$Tw = \frac{1}{\pi\sqrt{LC}}$$

(Tw : Resonance pulse width)

In reality, the above equation cannot be established due to the effects of stray capacity, and the Vcp and Tw for the all black signal (CRT cutoff) are as follows.
Vcp ≒ 1000 V
Tw ≒ 6 µ sec

The turn ratio of the primary side to secondary side of the flyback transformer (FBT) is about 40 times, and as a result, a pulse that is about 40 times (approximately 33 kV peak) Vp is output. The output pulse is rectified by the diode in the flyback transformer and capacitors inside the HVF (High Voltage Filter) and HVB (High Voltage Block) to produce 33 kV DC.
As the high voltage circuit operates asynchronized with the video signal, high voltage ripple components appear on the screen as noise. To prevent this, the high voltage is first passed through the HVF and then supplied to the HVB and CRT.

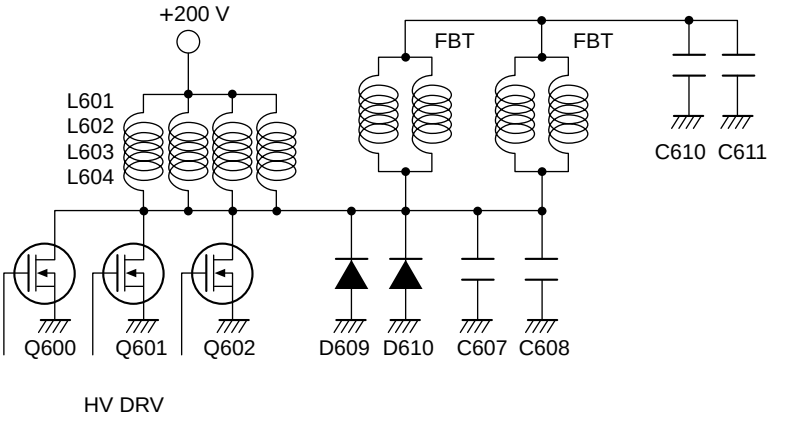


Fig. 15-1

15-3. HIGH VOLTAGE REGULATOR

In the high voltage circuit of this unit, fH in the 1) equation is varied and the resonance pulse (vcp) level is changed to control the high voltage regulation. fH is varied by the VCO (see “15.1 Internal Oscillation Circuit”.) Fig. 15-2 shows how the regulation is controlled. The all white signal, etc. is displayed to increase the high voltage load. When the high voltage drops, the oscillation frequency fH is decreased to increase the switching trace period to increase the Vcp. On the other hand, when the high voltage load decreases and the high voltage (HV) increases, the oscillation frequency fH is decreased to increase the switching trace period to increase Vcp.

The regulator has a feedback loop structure, and the high voltage fluctuation components are frequency divided and detected by the detection resistor inside the high voltage block (HVB). The detected output is input to the PA board as the HV. REG signal via CN87. The HV.REG signal is input to the error amplifier IC101 (2/2) via the filter IC101 (1/2), and compared with the reference voltage generated by IC100. The comparison output is then input to the internal oscillation circuit via the inverse amplifier. As a result, if the high voltage drops, the VCO oscillation frequency drops. If it increases, the VCO oscillation frequency increases and the high voltage is maintained at a constant.

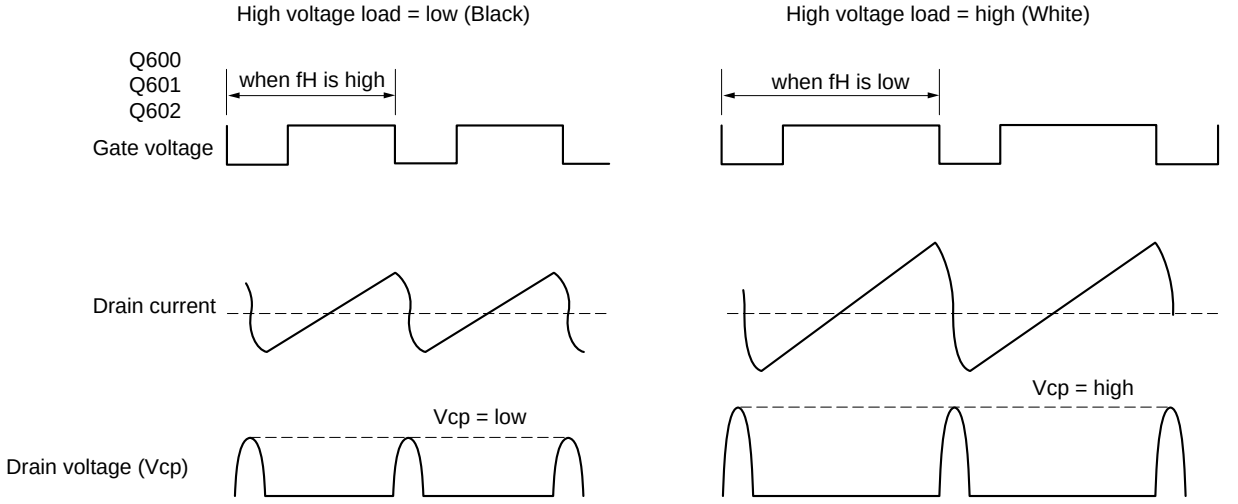


Fig. 15-2

15-4. VCO LIMITER

The VCO limiter circuit limits the VCO oscillation frequency when a problem occurs in the oscillation frequency of the VCO due to some reason to prevent damages of the high voltage circuit.
Q150 and Q151 compose the limiter circuit for the high frequency while IC102 (2/2) compose the limiter circuit for low frequency. In particular, as the high voltage increases when the VCO oscillation frequency becomes low, it can be set accurately by RV101 so that the input voltage to VCO does not drop below 1.70V.

15-5. HIGH VOLTAGE PROTECTOR CIRCUIT

This circuit turn OFF the power supply promptly when the high voltage rises abnormally as a result of the malfunction of the high voltage circuit due to some reason.
High voltage is voltage divided by the detection resistor inside the high voltage block and the detection results are input to the PA board as the HV.PROT.IN signal.
The HV.PROT.IN signal is input to the comparator IC251 (1/2) and compared with the reference signal generated by IC250 and RV250. When the HV.PROT.IN voltage is above the reference voltage, the comparator operates, Q153 turns ON via IC251 (2/2), and the high voltage oscillation stops. At the same time, Q252 is turned OFF via Q251 and the power of the unit is turned OFF.
At shipment, RV250 is adjusted so that the protector operates when the voltage becomes 34±0.3 kV.

15-6. ∑ IK PROTECTOR CIRCUIT

This circuit prevents flow of excessive beam to the CRT. This circuit detects the secondary current of four flyback transformers (FBT) (one pair for right and left respectively). The protector operates when an abnormal current (above 4.2 mA) is sent to either one.
When a current above 4.2 mA flows to the flyback transformer (FBT) connected to CN89, the Q200 base voltage becomes less than 0.6 V and Q200 goes OFF. As a result, the Q200 collector becomes High level, and the output of the comparator IC200 (1/2) becomes High level via the (OR) gate circuit by D200. Consequently, Q154 becomes ON and the high voltage oscillation stops. At the same time, the IC200 (2/2) output becomes High level and the power goes OFF.

15-7. ABL DETECTION CIRCUIT

In this unit, the current flowing to the four flyback transformer is detected by the two ABL detection circuits on the left and right sides each. Therefore to obtain all ABL signals, there is a need to add the two groups of currents in the PA board. The two groups of FBT currents are converted to the voltage signal in R612, R200, R201, and R202 and in R613, R205, R206, and R207. The converted signals are input to IC301 (1/2) via the buffer IC300, and added there. The added signal is then polarity-inverted by IC301 (2/2) and sent to the BA board from CN86.

SECTION 16
POWER SUPPLY SYSTEM

16-1. STRUCTURE OF POWER SUPPLY BOARD

This unit adopts a power supply circuit with full-wide input (AC 80 to 288 V) a maximum output of about 1000W, which is composed of the F board (AC filter), GA/GAA board (active filter), GB/GBA/GBB/GC boards (main converter).

F board :

This board is composed of a filter circuit for power disturbance measures and is incorporated with a 2-line filter circuit for inputs.

GA/GAA board :

These boards improve the power factor for AC inputs input via the AC filter and supply the approximately 370 DC voltage to the following four converters by the boosting chopper.
The GAA board is mounted with the following control circuits (control IC and peripheral circuits).

GB/GBA/GBB/GC boards :

When the DC voltage is supplied from the active filter, these boards drive the four converts as the secondary side output, and outputs various voltages.
They adopt a separate excited type current resonance converter.
The GBA and GBB board is mounted with the following control circuits (control IC and peripheral circuits).

16-2. ACTIVE FILTER

With the normal capacitor input, as current only flow near the peak commercial voltage, the power factor is poor, and the specified harmonic distortion cannot be met.
In this system, a boosting type active filter is therefore adopted to improve the power factor.

Basic Operations

In this system the power factor is improved and controlled by comparing the waveform made by multiplying the commercial voltage waveform with the error of the output voltage waveform with the current waveform detected by the current detection resistor, and stabilizing the voltage output from the boosting chopper and correcting the input current waveform at the same time. This unit mounts two active filters. As these two filters have the same basic operations, only one circuit will be described below.
The input voltage is converted to current by R105 and R106 of the GAA board, and input to I_{AC} of IC101. In order to enlarge the dynamic range, the voltage which is obtained by averaging DC by passing through the CR filter (R101, R102, R103, R104, C101, C102) is input to V_{RMS} of IC101.
The output voltage of IC101 is voltage-divided by the detection resistors (R125, R126, R127, R128, R129, RV101) of the GAA board. This voltage-divided voltage is then input to V_{SENSE} of IC101, compared with the reference voltage (Vref) inside the IC, and input to the multiplier. The three signals mentioned above (input current waveform : I_{AC}, input voltage average value : V_{RMS}, output voltage error : V_{SENSE}) are calculated and the calculation results and switching current value are calculated by the current error amplifier. The calculation results are then input to the PWM comparator, to generate the drive signal of the boosting chopper (MOS FET : Q1, Q2, Q3) of the GA board. The switching current value is detected by inputting the both ends voltage values of the detection resistance of the GA board (R154, R155, R156, R191) to “IM” and “IS” terminals.

16-3. MAIN CONVERTER

This unit mounts a four main converters. As the converters have the same basic operations, only the +15 V is described below.

Basic Operations

The DC output of the active filter is supplied to the switcher (MOS FET : Q5, Q6) of the GB board and the switcher (MOS FET : Q5, Q6) is turned ON and OFF according to the switching frequency determined by IC201 of the BGA board. At this time, the main current flowing to T2 becomes the sine resonance current generated by the resonance of the T2 leakage inductance and the capacitance of C26 and C32 , and the power is supplied to the load side. IC201 recharges the external timing capacitance (C215) at the constant current and generates the sawtooth wave. The oscillation frequency can be varied by changing the current of IC201 to R417. In this circuit, the +115 V output voltage is detected by IC203, and the current flowing to the photo diode PH202 is controlled to change the switching frequency.
The output voltage is controlled by changing the switching frequency against the changes in the input voltage and load as described above.

16-4. SUB POWER SUPPLY OPERATIONS

The flyback converter using a PWM control IC is adopted for the sub power supply.

Sub Power Supply Specifications

Rated input voltage : AC100/220 V
Output voltage : SUB6 V/load 1 to 4 A
Vcc1 (supplied from D1)/load 0 to 25 mA
Vcc2 (supplied from D4)/load 0 to 25 mA
Vcc3 (supplied from D6)/load 15 mA

Basic Operations

The AC voltage input to the F board is passed through the filter of the F board and the DC voltage is rectified by the GA board and output from the connector (CN20) of the GB board.
The DC voltage charges the capacitor of the GC board via R12 and R13 (start resistors). When the charged voltage reaches the start voltage of the Vcc (Pin 14) of the PWM control (IC5), IC5 starts operating.
The control IC (IC5) operates as follows.

- Pin 1 to Pin 3 : Drive totem pole output
- Pin 4 : Latch protection
- Pin 5 : F/B
- Pin 6 : Sets dead time (Not used)
- Pin 7 : REF
- Pin 8 : Sets soft start at start
- Pin 9 to Pin 11 : Sets the oscillation frequency (Approx. 70 kHz)
- Pin 13 : Current limit
- Pin 14 : Vcc

When Vcc is supplied to the control IC, the oscillator (sawtooth wave) operates. At the same time, the soft start circuit operates, Q4 (FET) is driven by the drive signal. The separate type transformer (T1) where the primary and secondary sides are insulated is adopted. Each winding is turned by the flyback method for the main winding of the primary side.
When Q4 (FET) is ON, the output of each winding goes off. When Q4 (FET) is OFF, signals are output from each winding. The output from the winding of Pins 10 to 12 and Pins 13 to 15 of T1 is rectified by D3, C8, and C9, smoothed by L1 and C12 next, and output as SUB 6 V. The SUB 6 V is input to the GC board, after which the reference voltage is generated by the shunt regulator (IC2). This reference voltage and output voltage are compared by the ope-amplifier (IC6) and the current of the light-emitting diode of the photocoupler (PH5) is controlled. The output of PH5 is input to Pin 5 (F/B terminal) of the PWM IC (IC5) and controlled so that the voltage stabilizes.
The other ope-amplifier in IC6 detects the output voltage state (detection of over-voltage). When over-voltage is detected, Pin 4 (latch protection terminal) of IC5 is triggered via the photocoupler (PH4) and is protected.

T1 Primary Winding

The voltage of Vcc1 winding (Pins 7 and 8), Vcc2 winding (Pins 4 and 6) and Vcc winding (Pins 4 and 5) is determined by the winding ratio for SUB 6 V. Vcc1 (Vcc2) is rectified by D1 (D4) and C3 (C7) and more than 22 V is output. This voltage (22 V) is input to the 3-pin regulator IC and IC2, and 20 V is output. This output voltage (20 V) is controlled by turning ON and OFF Q1 and Q2 by the P-Cont signal. The controlled output voltage is supplied to IC101 (PFC) of the GAA board (two) and IC for control of the main converters (IC201 and IC202 of the GBA board and IC401 and IC402 of the GBB board).

Vcc3 is rectified by D6 and C14 and approximately 14 V is output. This voltage is supplied to Vcc of IC5 (PWM) of the GC board. Furthermore, when the current flowing to FET by the detection resistor R20 is detected and the detected voltage goes above the voltage of Pin 13 (current limit terminal) of IC5, the ON period of the drive output signal becomes short, and the excessive current is limited.

ON/OFF Sequence

The ON and OFF sequence of this unit is controlled by the ON and OFF of the P-Cont signal as shown below. SUB 6 V is reduced to 5 V by R11 and D1 of the GC board and supplied to Pins 14 (Vcc), 2, and 9 of IC3 (AND gate) of the GC board. When P-Cont becomes High level, Pins 1, 10, and 12 becomes High level. As Pin 13 is Low level, Pin 11 is also Low level, Pin 8 becomes High level, and C5 of the GC board is charged.
When Pin 3 becomes High level, Q1 of the GC board operates and current is supplied to the diode of the photocoupler PH3. As a result, Q2 of the GB board operates, and voltage (Vcc) is supplied to the “LowB block “ control IC.
When the 15 V of “Low B block” is output, Pin 13 of IC3 of the GC board becomes High level. When Pin 11 becomes High level, Q4 of the GC board operates and current flows to the diode of the photocoupler PH1. As a result, Q1 of the GB board operates, and voltage (Vcc) is supplied to the control IC of the “Low B block”.
When P-Cont becomes Low level, Pin 11 (+B block) of the GC board becomes Low level, power supply (Vcc) of the +B block of the IC3 of the control IC is turned off, and the +B block output starts to drop. The voltage of Pin 1 of IC3 drops according to the discharge time constant of C5 and R14 of the GC board. After about 30 ms, Pin 3 of IC3 becomes Low level, and power supply of the control IC of the “Low B block” goes off.

Overvoltage Protection

Overvoltage protection is performed in this unit as follows. IC1 of the GC board generates the reference voltage. The reference voltage is supplied to IC4 and compared with the 15 V, 50 V, 115 V, and 200 V output voltage. When any one of these output voltages become overvoltage, Q3 operates, the P-Cont. signal is set to the Low level by the thyristor circuit composed of Q2 and Q3, and the power supply is latched. The latch is cleared when the power supply switch is turned off.
IC3 and IC4 of the GB board monitors the output voltage of the active filter. When the overvoltage is detected, Pin 4 of IC5 of the GC board becomes High level, and the power shuts down.

SECTION 17
YA BOARD

17-1. CPU SYSTEM

The CPU of this unit is a 32-bit RISC microprocessor. All control operations of the unit are performed by one chip. The circuits of the YA board can broadly be divided into four blocks.

- CPU
  - MAIN BLOCK
    - SIRCS processing
    - +5 V supply to commander
    - Set protector
    - 7 seg. LED control
  - COMM. BLOCK
    - RS-232C communication
    - RS-422A communication
    - RS-485 communication
  - REGI BLOCK
    - I^2C control
    - Regi DAC control
    - G2 control
    - Sync separate
    - Frequency detect
    - Data save/load
  - OSD BLOCK
    - OSD processing
    - Character and internal signal generation
    - V-shift control
    - Blanking control

17-1-1. Main Devices of YA Board

CPU	HD6437043AF28	
Address dec.	UPD65646GJ-252-8EU	Sub µcom・SIRCS control
Sub µcom	CXP846P48Q	SIRCS encoder/decoder
UV-EPROM	M27C4002-10F1	Uploader
Program Flash ROM	MBM29F800BA-70PFTN	Main program
S-RAM	IDT71024S15Y∗2	
I/O Port ④	UPD65646GJ-252-8EU	Set protector
7 seg. LED driver	EPM7128STC100-15-DRV	7 seg. LED control
Serial I/F with FIFO	PC16552DV	Serial communication
RS-232C driver	MAX202ECSE	RS-232C control
RS-485 driver	MAX3085CSA∗2	RS-485 control
RS-422A driver	MAX489ECSD	RS-422A control
I/O Port ②	UPD65646GJ-252-8EU	IFB control, I^2C control, various differentiation operations
Battery S-RAM	DS1245Y-120	User data save (Expandable to 512 kbytes)
Backup Flash ROM	MBM29F040C-90PD	Service/Factory data save
Regi DAC controller	CXD305-127R	DAC control for registration
G2 DAC controller	CXD2309Q	DAC control for G2
Freq. Det. G/A	UPD65654GC-327-3B6	Freq. Det.
Sync sep. G/A	CXD8773R	Sync control
ODS G/A	UPD65806GD-064	OSD control
S-RAM	IDT71016S15Y∗2	
I/O Port ③	UPD65646GJ-252-8EU	OSDC control, PLL control
Clock driver	MC10H640FN	2CLK driver
CMD Dualport RAM	IDT71321S55J	OSD command RAM
FONT Flash ROM	MBM29F400BC-70PFTN	OSD FONT DATA

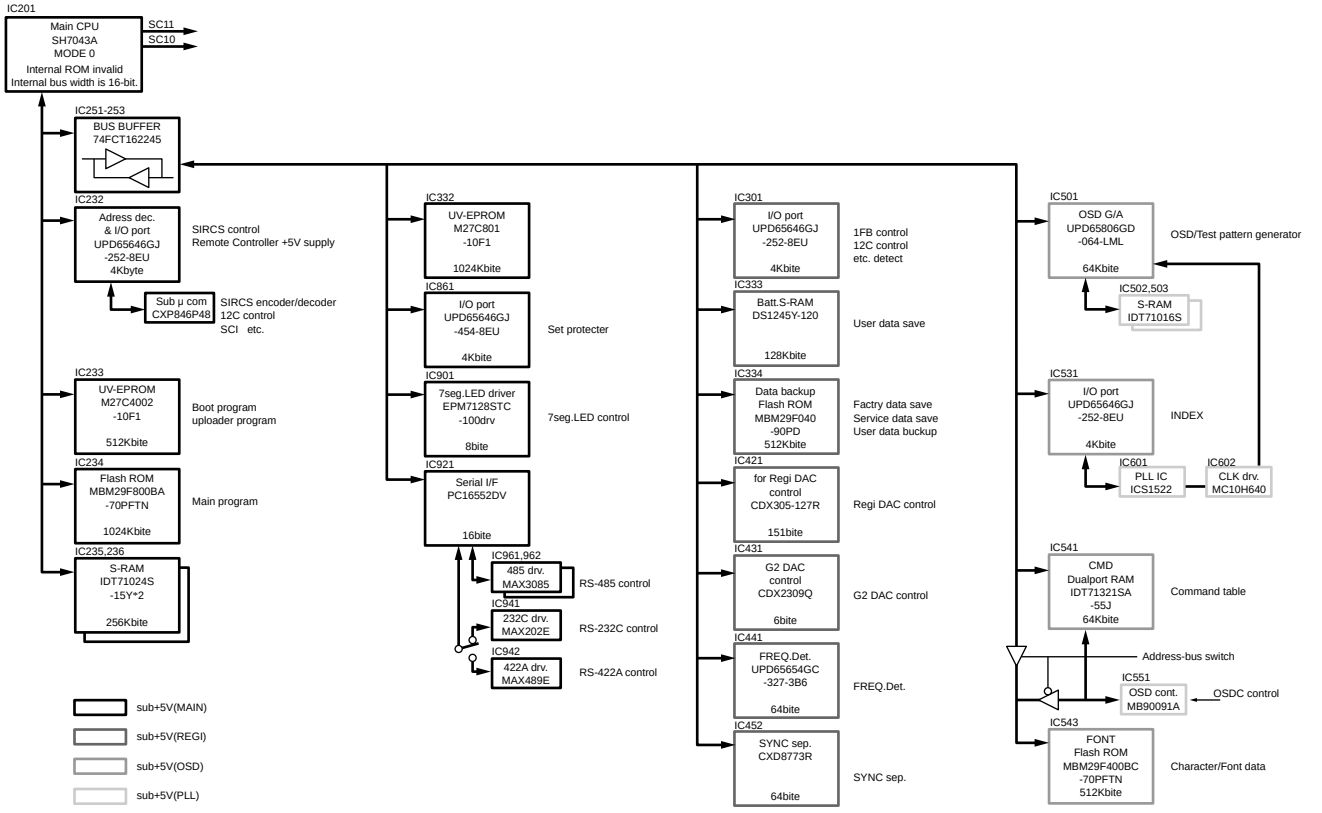


Fig. 17-1

17-1-2. Version Upgrading of Program

In this system, in order to rewrite a program data on the board, the main program data and font data are stored in the flash memory. As data is rewritten using a communication system, it eliminates the need to perform the following procedure required to upgrade program version which is quite inconvenient ; 1) removing the cabinet, 2) removing the board, 3) replacing the program ROM, and 4) returning the board to its original position. The upgrading procedure is now very simple ; just by connecting the cable to the D-sub connector for communication, only the instructions of the communication device need to be followed in order to upgrade the version of the built-in program.

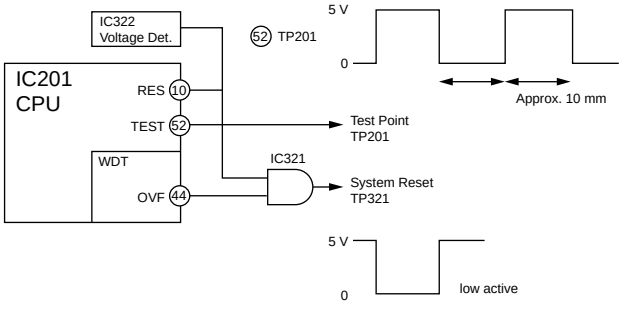


Fig. 17-2

17-1-3. Resetting the System

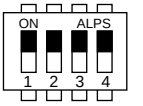
The system is reset by the output of the WDT (Watch Dog Timer) in the CPU and external voltage monitoring IC. Normally, the CPU sends a perioddical trigger to the built-in WDT to indicate that operations are normal. However when it stops sending the trigger due to some reason, the built-in WDT determines that the CPU is abnormal, and generates the Reset signal internally.
To reset the external devices of the CPU, the OVF output signal indicating that the built-in WDT has generated reset is used.
The unit is also mounted with an external voltage monitoring IC, so that the system can be reset normally in times of voltage instability when the main power is ON and in momentary power failures.

17-1-4. Various Setting Switches

There are eight switches on the YA board. These are described briefly below.

S201 : SW for setting CPU operations

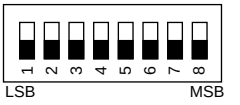
1. Factory Mode on/off : When ON, factory mode off
2. Refresh on/off : When ON, refresh mode off
3.
4. For reviewing design



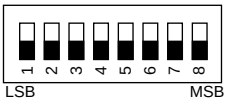
S202 : Used for formatting the user area
Request from software (ERROR CODE “30”)
Or used for forced formatting.

S203 : For future application

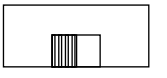
S204 : Software version differentiation
Set initial values of the VPH-G90 as shown on the left.



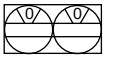
S205 : Software version differentiation
Set initial values of the VPH-G90 as shown on the left.



S961 : For switching between RS-232C and RS-422A
→ RS-232C communication
← RS-422A



S962, 963 : For setting device index
Used for setting device index to 00 to 99.
Setting to 00 disables control operations other than that using the control panel.



17-2. SIRCS PROCESSING CIRCUIT

17-2-1. SISCS MIX

Although the SIRCS signal can be directly received by the CPU, since various SIRCS signals are input to the YA board, to enable all SIRCS signal to be received when several SIRCS signals are input at the same time, the SIRCS signals are processed according to a priority order.

Priority Order of SIRCS

Communication → Control Panel → CCQ, WIRED → Light-receiving section

When the CPU receives a SIRCS signal through the highest priority order communication path, other SIRCS inputs are ignored, and the SIRCS CODE obtained in the communication is written in the SIRCS encoder. Taking this writing operation as the trigger, the SIRCS encoder sets the OUT terminal to LOW and outputs the SIRCS signal.

If the SIRCS signal (SIRCS RC) from the control panel is input to the YA board, the RC ON line becomes LOW at the same time, and SIRCS signals with lower priority order than the SIRCS RC are cut. All SIRCS RC signals are input to the CPU, selected, and only those required are written in the SIRCS encoder.

Normally, the SIRCS CCQ line is bi-directional, but becomes one-direction only when signals from the SIRCS encoder or SIRCS RC signals are output.

The SIRCS signals (SIRCS, NA, NB) from the light-receiving section have the same priority order, and so cannot be received properly when input at the same time. However, each line can be invalidated by software control.

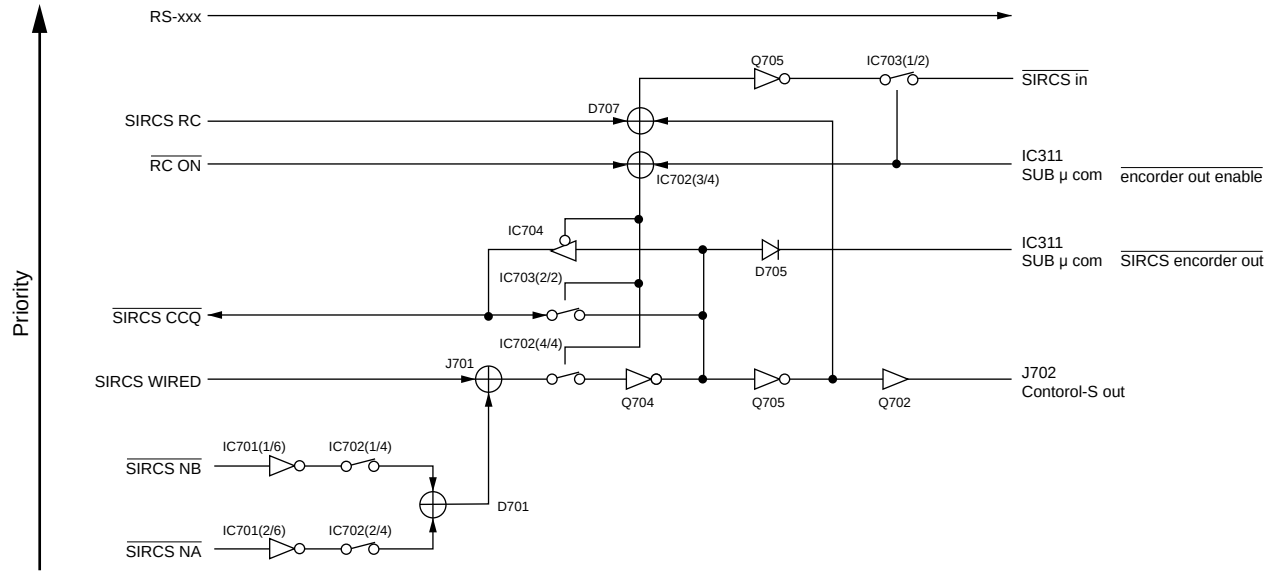


Fig. 17-3

17-2-2. Circuit Supplying +5 V To Commander

This circuit supplies power to the commander connected to the PJ unit by the STEREO SIRCS cable. It consists of two circuits-the normal state circuit, and commander LIGHT ON state circuit.

The normal state circuit can supply power when sub +6 V is started by the AC POWER ON of the unit.
When the commander button is pressed in this state, approximately 5 V, 4 mA is supplied to the commander from the CONTROL-S terminal. If the output is short-circuited (when the MONAURAL SIRCS cable is connected, etc.), the current supplied from the terminal becomes fixed at approximately 55 mA.

When the LIGHT ON button is pressed by the commander, the SIRCS signal sent from the command is received by the CPU via the SIRCS MIX circuit. At the same time, the CPU checks each differentiation line (WI ON, ON ENABLE), and when it has confirmed that it is the LIGHT ON SIRCS from the commander connected by the cable, it sets the supply circuit to ACTIVE. As a result, the current restriction mentioned earlier is cleared, and the current consumed by LIGHT UP is supplied to the commander.

The conditions at which supply of the LIGHT UP current is stopped are;

1. When the LIGHT button of the command is pressed again while the LIGHT is lit (when LIGHT OFF SIRCS is received)
2. After 30 ms from when LIGHT ON SIRCS is received (the counter is reset when SIRCS is received while counting the time)
3. Output voltage monitor (Detected by IC732 : Forced OFF when the output voltage is below 3.0 V)
4. When the STEREO SIRCS cable is disconnected (Detected by CONTROL-S terminal)

In any of the above conditions, the power supply for command LIGHT ON sets into the STANDBY state, and the normal state circuit is set back again.

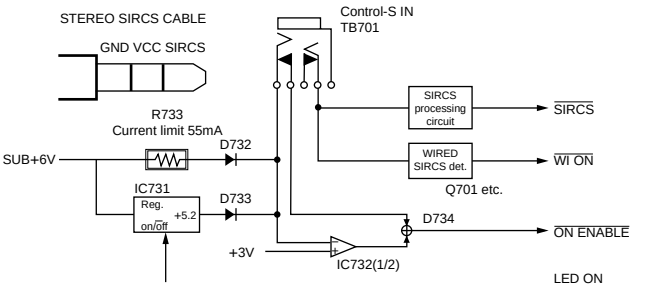


Fig. 17-4

17-3. SET PROTECTOR

17-3-1. Set Protector Circuit

The protector circuit can broadly be divided into two blocks. One is the protector by the software and the other is the protector by the hardware. Normally, the unit is protected by the software protector, and the hardware protector serves as a spare circuit for when the software protector cannot operate. The protector circuit is effective only when the power of the unit is ON, and does not function in the STANDBY state.
Information on protector signals from each board in the unit is gathered in the YA board, and constantly monitored by IC861. When a protector signal is detected, IC861 generates an interrupt signal to the CPU. On receiving this, the CPU takes in the information via IC861. Based on this information, the CPU displays error codes on the 7 segment LED on the YB board, and sets back the unit into the STANDBY state.

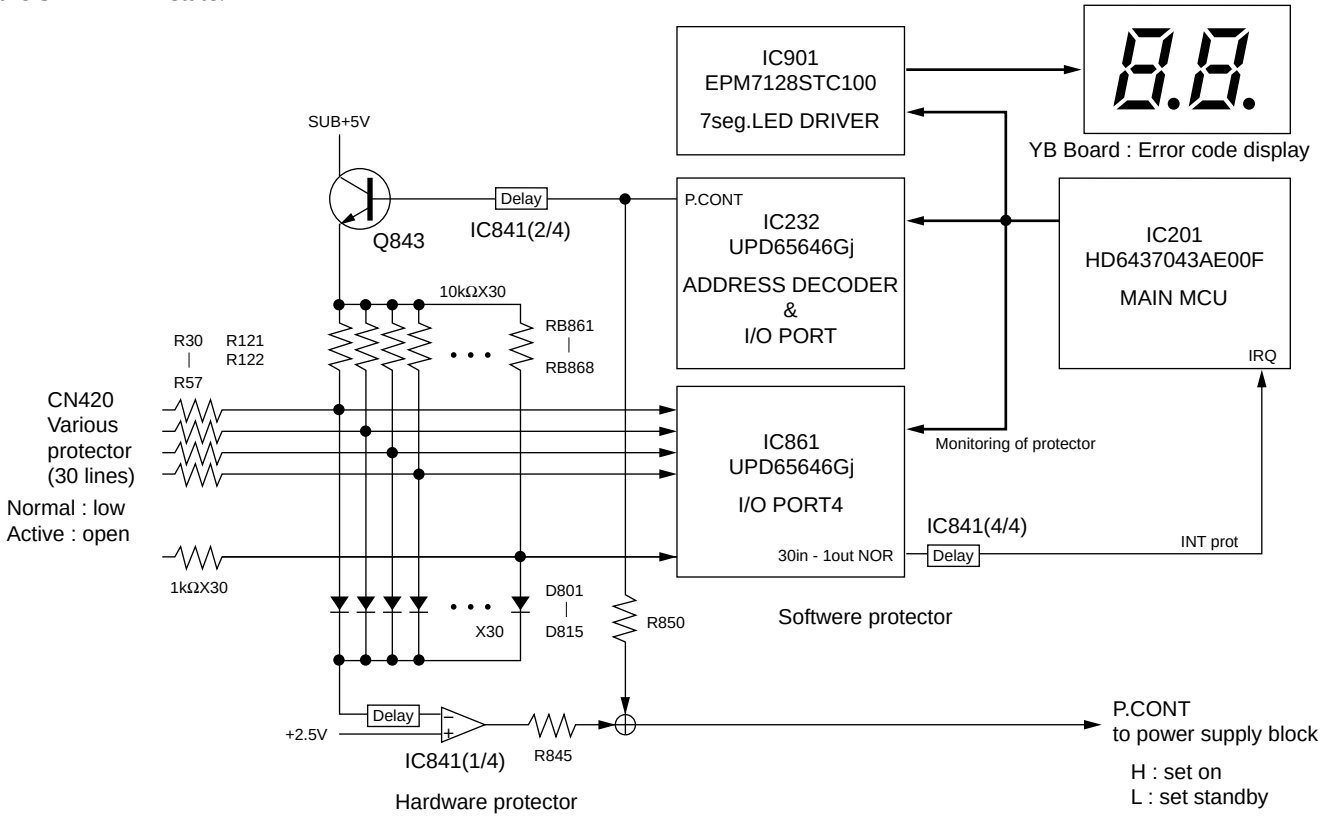


Fig. 17-5

17-3-2. 7-Segment LED Error Codes

The error messages displayed on the 7-segment LED consists of protector information and information on the operating state of the unit.
Error messages are displayed in three colors-green, orange, and red, and the significance is determined by the color. The displayed number and corresponding message are shown in the following table.

No.	No.	Class	Application	Identifier	Note
00	00			ERR_NORMAL	
01	01	Warning	BOOT	ERR_WARN_MAINNVM_SUMERR	MAIN NVM check sum incorrect !
02	02	Warning	BOOT	ERR_WARN_MAINNVM_INSTALLING	MAIN NVM installing (from ROM)...
03	03	Warning	BOOT	ERR_WARN_FONTNVM_SUMERR	FONT NVM check sum incorrect !
04	04	Warning	BOOT	ERR_WARN_FONTNVM_INSTALLING	FONT NVM installing (from ROM)...
05	05	Warning	BOOT		
06	06	Warning	BOOT		
07	07	Warning	BOOT		
08	08	Warning	BOOT		
09	09	Warning	BOOT		
10	0A	Warning	BOOT		
11	0B	Warning	BOOT		
12	0C	Warning	BOOT		
13	0D	Warning	BOOT		
14	0E	Warning	BOOT		
15	0F	Warning	BOOT		
16	10	Warning	DOWN LOADER		DownLoader starts! (2times flashing)
17	11	Warning	DOWN LOADER		NVM data down loading (from COMM)...
18	12	Warning	DOWN LOADER		NVM updating (from COMM)...
19	13	Warning	DOWN LOADER		
20	14	Warning	DOWN LOADER		
21	15	Warning	DOWN LOADER		
22	16	Warning	DOWN LOADER		
23	17	Warning	DOWN LOADER		
24	18	Warning	DOWN LOADER		Transport Error
25	19	Warning	DOWN LOADER		Transport Error Start Code Low Byte Error
26	1A	Warning	DOWN LOADER		Transport Error Packet Length Error
27	1B	Warning	DOWN LOADER		Transport Error Data Length Error
28	1C	Warning	DOWN LOADER		Transport Error Header Checksum Error
29	1D	Warning	DOWN LOADER		Transport Error Data Checksum Error
30	1E	Warning	DOWN LOADER		Transport Error Data End Low Byte Error
31	1F	Warning	DOWN LOADER		Transport Error Data End High Byte Error
32	20	Warning	DOWN LOADER		Transport Error Invalid Command
33	21	Warning	DOWN LOADER		Transport Error Retry occur
34	22	Warning	DOWN LOADER		
35	23	Warning	DOWN LOADER		
36	24	Warning	DOWN LOADER		Session Error
37	25	Warning	DOWN LOADER		
38	26	Warning	DOWN LOADER		
39	27	Warning	DOWN LOADER		
40	28	Warning	DOWN LOADER		
41	29	Warning	DOWN LOADER		
42	2A	Warning	DOWN LOADER		
43	2B	Warning	DOWN LOADER		
44	2C	Warning	DOWN LOADER		
45	2D	Warning	DOWN LOADER		
46	2E	Warning	DOWN LOADER		
47	2F	Warning	DOWN LOADER		Return to Normal Mode
48	30	Warning	MAIN	ERR_WARN_USRNVM_FORMATERR	User NVM format not available !
49	31	Warning	MAIN	ERR_WARN_USRNVM_FORMATTING	User NVM formatting...
50	32	Warning	MAIN	ERR_WARN_USRNVM_WRITING	User NVM writing...
51	33	Warning	MAIN	ERR_WARN_SVCNVM_FORMATERR	Service NVM format not available !
52	34	Warning	MAIN	ERR_WARN_SVCNVM_FORMATTING	Service NVM formatting...
53	35	Warning	MAIN	ERR_WARN_SVCNVM_WRITING	Service NVM writing...
54	36	Warning	MAIN	ERR_WARN_FTYNVM_FORMATERR	Factory NVM format not available !
55	37	Warning	MAIN	ERR_WARN_FTYNVM_FORMATTING	Factory NVM formatting...
56	38	Warning	MAIN	ERR_WARN_FTYNVM_WRITING	Factory NVM writing...
57	39	Warning	MAIN	ERR_WARN_USRNVM_FTYRESET	User NVM needs FTY reset (Simulation → Normal)
58	3A	Warning	MAIN	ERR_WARN_IMEM_CHANGING	Input memory changing...
59	3B	Warning	MAIN	ERR_WARN_ONDELAY_WAITING	Now Power on delay waiting...

No.	No.	Class	Application	Identifier	Note
60	3C	Warning	MAIN		
61	3D	Warning	MAIN		
62	3E	Warning	MAIN		
63	3F	Warning	MAIN		
64	40	Warning	MAIN	ERR_WARN_SYSTEM_CONFIGURING	Configuring the system
65	41	Warning	MAIN	ERR_WARN_PJ_INDEXERR	Same DEVICE INDEX for Projector detected
66	42	Warning	MAIN	ERR_WARN_SW_INDEXERR	Same DEVICE INDEX for Switcher detected
67	43	Warning	MAIN	ERR_WARN_SW_MASTERERR	Master Switcher not exist
68	44	Warning	MAIN		
69	45	Warning	MAIN		
70	46	Warning	MAIN		
71	47	Warning	MAIN		
72	48	Warning	MAIN		
73	49	Warning	MAIN		
74	4A	Warning	MAIN		
75	4B	Warning	MAIN		
76	4C	Warning	MAIN		
77	4D	Warning	MAIN		
78	4E	Warning	MAIN		
79	4F	Warning	MAIN		
80	50	Warning	MAIN		
81	51	Warning	MAIN		
82	52	Warning	MAIN		
83	53	Warning	MAIN		
84	54	Warning	MAIN		
85	55	Warning	MAIN		
86	56	Warning	MAIN		
87	57	Warning	MAIN		
88	58	Warning	MAIN		
89	59	Warning	MAIN		
90	5A	Warning	MAIN		
91	5B	Warning	MAIN		
92	5C	Warning	MAIN		
93	5D	Warning	MAIN		
94	5E	Warning	MAIN		
95	5F	Warning	MAIN		
96	60	Protector	MAIN	ERR_PROT_UNKNOWN	Unknown
97	61	Protector	MAIN	ERR_PROT_POW1	POW1
98	62	Protector	MAIN	ERR_PROT_POW2	POW2
99	63	Protector	MAIN	ERR_PROT_POW3	POW3
100	64	Protector	MAIN	ERR_PROT_POW4	POW4
101	65	Protector	MAIN	ERR_PROT_POL	POL
102	66	Protector	MAIN	ERR_PROT_HSTOP	H.STOP
103	67	Protector	MAIN	ERR_PROT_VSTOP	V.STOP
104	68	Protector	MAIN	ERR_PROT_SUB	SUB
105	69	Protector	MAIN	ERR_PROT_HV	HV
106	6A	Protector	MAIN	ERR_PROT_LOT	LOT
107	6B	Protector	MAIN	ERR_PROT_IK	Ik
108	6C	Protector	MAIN	ERR_PROT_SIK	∑Ik
109	6D	Protector	MAIN	ERR_PROT_FAN1	FAN1
110	6E	Protector	MAIN	ERR_PROT_FAN2	FAN2
111	6F	Protector	MAIN	ERR_PROT_LENS	LENS
112	70	Protector	MAIN	ERR_PROT_CRTR	CRTR
113	71	Protector	MAIN	ERR_PROT_CRTG	CRTG
114	72	Protector	MAIN	ERR_PROT_CRTB	CRTB
115	73	Protector	MAIN	ERR_PROT_IFBB	IFBB
116	74	Protector	MAIN	ERR_PROT_IFBC	IFBC
117	75	Protector	MAIN		
118	76	Protector	MAIN		
119	77	Protector	MAIN		
120	78	Protector	MAIN		
121	79	Protector	MAIN		
122	7A	Protector	MAIN		
123	7B	Protector	MAIN		
124	7C	Protector	MAIN		
125	7D	Protector	MAIN		
126	7E	Protector	MAIN		
127	7F	Protector	MAIN		
128	80	Protector	MAIN	ERR_PROT_BA	BA

No.	No.	Class	Application	Identifier	Note
129	81	Protector	MAIN	ERR_PROT_DA	DA
130	82	Protector	MAIN	ERR_PROT_DB	DB
131	83	Protector	MAIN	ERR_PROT_DD	DD
132	84	Protector	MAIN	ERR_PROT_DE	DE
133	85	Protector	MAIN	ERR_PROT_EBR	EBR
134	86	Protector	MAIN	ERR_PROT_EBG	EBG
135	87	Protector	MAIN	ERR_PROT_EBB	EBB
136	88	Protector	MAIN	ERR_WARN_DIAGNOSTIC	Initializing...
137	89	Protector	MAIN	ERR_PROT_EBH	EBH
138	8A	Protector	MAIN	ERR_PROT_EBQ	EBQ
139	8B	Protector	MAIN		
140	8C	Protector	MAIN		
141	8D	Protector	MAIN		
142	8E	Protector	MAIN		
143	8F	Protector	MAIN		
144	90	Protector	MAIN		
145	91	Protector	MAIN		
146	92	Protector	MAIN		
147	93	Protector	MAIN		
148	94	Protector	MAIN		
149	95	Protector	MAIN		
150	96	Protector	MAIN		
151	97	Protector	MAIN		
152	98	Protector	MAIN		
153	99	Protector	MAIN		
154	9A	Protector	MAIN		
155	9B	Protector	MAIN		
156	9C	Protector	MAIN		
157	9D	Protector	MAIN		
158	9E	Protector	MAIN		
159	9F	Protector	MAIN		
160	A0	Error	BOOT		
161	A1	Error	BOOT		
162	A2	Error	BOOT		
163	A3	Error	BOOT		
164	A4	Error	BOOT		
165	A5	Error	BOOT		
166	A6	Error	BOOT		
167	A7	Error	BOOT		
168	A8	Error	BOOT		
169	A9	Error	BOOT		
170	AA	Error	BOOT		
171	AB	Error	BOOT		
172	AC	Error	BOOT		
173	AD	Error	BOOT		
174	AE	Error	BOOT		
175	AF	Error	BOOT		
176	B0	Error	DOWN LOADER		
177	B1	Error	DOWN LOADER		
178	B2	Error	DOWN LOADER		
179	B3	Error	DOWN LOADER		
180	B4	Error	DOWN LOADER		
181	B5	Error	DOWN LOADER		
182	B6	Error	DOWN LOADER		
183	B7	Error	DOWN LOADER		
184	B8	Error	DOWN LOADER		
185	B9	Error	DOWN LOADER		
186	BA	Error	DOWN LOADER		
187	BB	Error	DOWN LOADER		
188	BC	Error	DOWN LOADER		
189	BD	Error	DOWN LOADER		
190	BE	Error	DOWN LOADER		
191	BF	Error	DOWN LOADER		
192	C0	Error	DOWN LOADER		
193	C1	Error	DOWN LOADER		
194	C2	Error	DOWN LOADER		
195	C3	Error	DOWN LOADER		
196	C4	Error	DOWN LOADER		
197	C5	Error	DOWN LOADER		

No.	No.	Class	Application	Identifier	Note
198	C6	Error	DOWN LOADER		
199	C7	Error	DOWN LOADER		
200	C8	Error	DOWN LOADER		
201	C9	Error	DOWN LOADER		
202	CA	Error	DOWN LOADER		
203	CB	Error	DOWN LOADER		
204	CC	Error	DOWN LOADER		
205	CD	Error	DOWN LOADER		
206	CE	Error	DOWN LOADER		
207	CF	Error	DOWN LOADER		
208	D0	Error	MAIN	ERR_FATAL_USRNVM_FORMATERR	User NVM format not available !
209	D1	Error	MAIN	ERR_FATAL_USRNVM_WRITEERR	User NVM write error !
210	D2	Error	MAIN	ERR_FATAL_SVCNVM_FORMATERR	Service NVM format not available !
211	D3	Error	MAIN	ERR_FATAL_SVCNVM_WRITEERR	Service NVM write error !
212	D4	Error	MAIN	ERR_FATAL_FTYNVM_FORMATERR	Factory NVM format not available !
213	D5	Error	MAIN	ERR_FATAL_FTYNVM_WRITEERR	Factory NVM write error !
214	D6	Error	MAIN	ERR_FATAL_STDCONSTNVM_FORMATERR	Standard Const NVM format not available !
215	D7	Error	MAIN		
216	D8	Error	MAIN		
217	D9	Error	MAIN		
218	DA	Error	MAIN		
219	DB	Error	MAIN		
220	DC	Error	MAIN		
221	DD	Error	MAIN		
222	DE	Error	MAIN		
223	DF	Error	MAIN		
224	E0	Error	MAIN		
225	E1	Error	MAIN		
226	E2	Error	MAIN		
227	E3	Error	MAIN		
228	E4	Error	MAIN		
229	E5	Error	MAIN		
230	E6	Error	MAIN		
231	E7	Error	MAIN		
232	E8	Error	MAIN		
233	E9	Error	MAIN		
234	EA	Error	MAIN		
235	EB	Error	MAIN		
236	EC	Error	MAIN		
237	ED	Error	MAIN		
238	EE	Error	MAIN		
239	EF	Error	MAIN		
240	F0	Error	MAIN		
241	F1	Error	MAIN		
242	F2	Error	MAIN		
243	F3	Error	MAIN		
244	F4	Error	MAIN		
245	F5	Error	MAIN		
246	F6	Error	MAIN		
247	F7	Error	MAIN		
248	F8	Error	MAIN		
249	F9	Error	MAIN		
250	FA	Error	MAIN		
251	FB	Error	MAIN		
252	FC	Error	MAIN		
253	FD	Error	MAIN		
254	FE	Error	MAIN		
255	FF	Error	MAIN		

17-4. I²C CONTROL

The I²C bus performs serial communication with the I²C device using two lines SCL and SDA.

As no control is performed during set standby, the line connected to this line is separated by incorporating a bus switch to prevent current leakage during standby.
The I²C bus mainly performs control of the small signal circuit on the BA board.

17-5. DAC CONTROL

17-5-1. Registration DAC Control

The DAC IC control for adjusting registration on the D board is performed by eight control lines-D-SCL, D-SDA0, D-SDA1, D-SDA2, D-LD0, D-LD1, D-LD2, and D-LD3.
To control one channel DAC, 12-bit DAC data (including the DAC address), CLK for data shift, and LD pulse for inputting the data are required. The actual IC incorporates a 8-ch DAC.

DAC control waveform (For one channel)

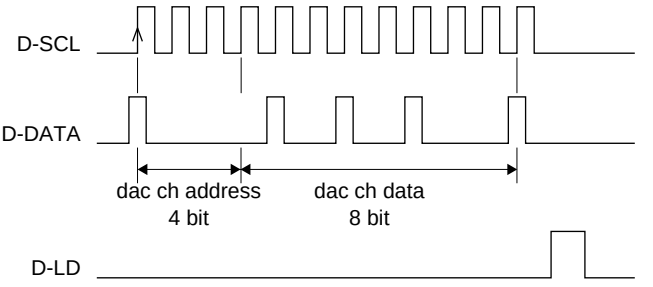


Fig. 17-6

This DAC IC also has a SDO terminal (Serial Data Out). As it can be cascade connected, a group of DAC ICs can be formed by cascade connection so that several DACs can be controlled at one time.
In the D board, six of these DAC ICs are cascade connected to form one group and there are altogether twelve groups.
In order to control all DACs, 12-bit × 6 × 8-channel 12-group data is required.

One group

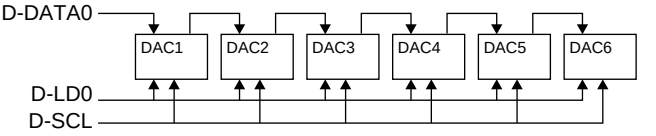


Fig. 17-7

DAC control waveform (1 group)

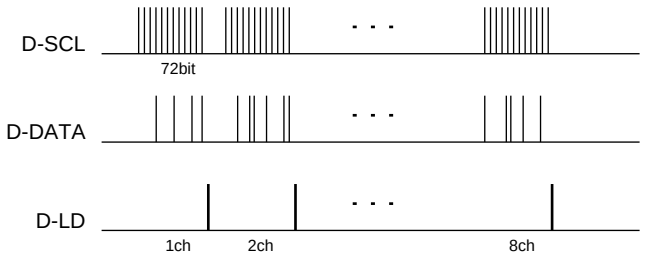


Fig. 17-8

Taking into consideration effects on the images, data is transferred to the DAC within about half (180 us) the VD period (flyback period) taking the deflection return VD as the trigger.
The transfer CLK is about 5 MHz.
In the YA board, data of three groups are temporarily stored in IC421 during the video period, and data transfer is started at the same time the VD period starts.
Consequently, 4VD is required to control the DAC of all twelve groups.

17-6. SYNC PROCESSING

17-6-1. Sync Sep. G/A (IC452)

A newly developed IC which performs input sync presence detection, input sync polarity detection, output sync polarity standardization, H/V separation, H-sync width standardization, clamp pulse generation, interlace differentiation, and frequency detection.

Input sync presence detection

H/C sync : For the RGB input, the signal connected to the H/C-sync input terminal on the BA board is input.
For the video input, the sync-separated composite-sync by the BA board is input.
- Determined as present when SYNC is input in the 16H continuous period.
- Determined as absent when SYNC is not input even one time for 6.2 msec. in the continuous period.

V sync : For the RGB input, the signal connected to the V-sync input terminal on the BA board is input.
For the video input, the sync-separated V-sync is input by the BA board.
- Determined as present when V SYNC is input even once in the 8192H period.
- Determined as absent when V SYNC is not input even once in the 8192H period.

SonG : Green is input for the RGB input and the signal sync-separated by the BA board is input for the video input.

Input sync polarity detection, standardization output

As the polarity of the H/V sync input to the YA board is not standardized by the type of input signal, the polarity is determined inside G/A, and at the same time, the negative polarity is standardized and output.

H/V Separation

When the sync source selected is C-sync, SonG, the signal is separated into H-sync and V-sync, and output to the deflection block. This is then performed without adjustments to 15 to 150 kHz by the digital H/V separator in the G/A block. If the equivalent pulse is present, it is extracted and output.

Interlace differentiation

When the H SYNC just before the V SYNC is detected, it is determined as INTERLACE if the distance of this period is above 1/4H and below 3/4H for every FIELD.

Frequency detection

fH counter : 11 bit (master clock = 20 MHz)
Can be measured from 10.24 kHz. Accuracy when fH = 200 kHz : Average 1 %. Worst 2 %.
As the value matching for 64H is output, it is not affected by the equivalent pulse, etc.

fV counter : 13 bit
Counts the number of horizontal lines. Can count to 8192 lines.
Outputs the number of lines of the V period counter.
(Not processed such as averaging, etc.)

Clamp pulse generation

The clamp pulse is generated by the following timing according to the type of clamp source in the table described later.
If no SonG, the clamp pulse is generated from the front edge of HS/CS-sync so that H-Back Porch can also be applied to short sources.

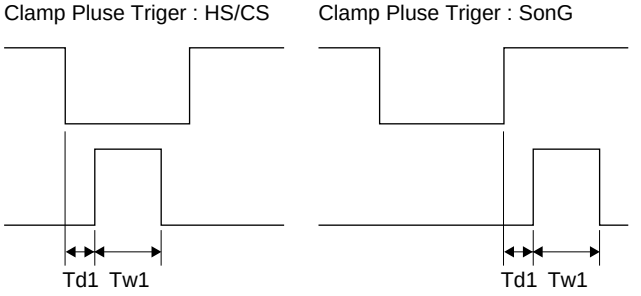
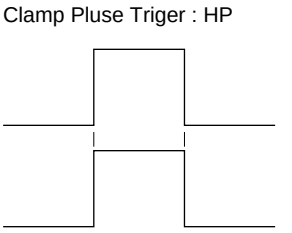


Fig. 17-9



HP width : ≒ 1050 ns (When fH < approx. 50 kHz)
≒ 560 ns (When fH ≧ approx. 50 kHz)

Fig. 17-10

When no interval in V-sync, and C-sync or H/V-sync is present, as SonG cannot be accurately detected, clamping may be incorrect. In this case, disconnect the external sync signal, or select trigger the CLAMP pulse generation at the setting menu of the CLAMP pulse.

The CLAMP pulse output from the YA board is selected by IC456.

Clamp : When AUTO/H/C/SonG
The Sync Sep. G/A output becomes the output of the YA board.

Clamp : When HP
The HD deflected to the YA board becomes the output of the YA board.

Input Signal Type	Td1 (ns)		Tw1 (ns)	
	Less than 39 kHz	More than 39 kHz	Less than 39 kHz	More than 39 kHz
VIDEO	400 + 50		1000 + 50	
S-VIDEO				
COMPONENT				
RGB	400 + 50	100 + 50	1000 + 50	500 + 50
15 kRGB				
HDTV YPBPR	700 + 50		1000 + 50	
HDTV GBR				
DRC	400 + 50		1000 + 50	
INT IDTV				
IDTV				
SDI-422	400 + 50		1000 + 50	

17-7. FREQUENCY DETECTION

As the registration and color temperature of the CRT projector become unstable due to the horizontal frequency fH and vertical frequency fV, accurate frequency detection is required because the CPU selects and calculates adjustment data, as well as calculates the positions and size of TEST PATTERN and OSD.
In order to perform these processes quickly and accurately, the accuracy and speed of the frequency detection system plays an important role. Inside the source, fH/fV jitters occur, frequency deviates minutely due to temperature, and fH/fV may become unstable during special playback (fast forward, etc.) of the video.
A frequency detection system which detects the frequency accurately and quickly is required.

Through the development of a new G/A, and review of current frequency detection systems from the hardware and software perspective, the signal switching time has been reduced and screen erasure quality has been improved in the VPH-G90.

Improvements of frequency detection system

- Addition of VD synchronizer
  A VD synchronizer (noise -prevention measure) is incorporated in the front stage of the fV counter. This enhances the noise-resistance of the fV counter, thus eliminating signal stable detection incorrect operations.

Addition of frequency detection of signal source

- Frequency is detected by the SYNC (SYNC SEP IC output) of the input signal so that it is not affected by V SHIFT and AFC.
  This as a result, eliminates V SHIFT circuit incorrect operations and deflection stable waiting time, and realizes compatibility with the frequency limiter.

Deflection frequency detection

- Frequency detection is also performed by the deflection SYNC.
  As a result, high quality screen erasure can be performed, and messages can be displayed on the OSD during NO INPUT, abnormal signal, and V HOLD adjustments.

17-8. COMMUNICATION

17-8-1. RS-232C Communication (IC941)

Communication with the controller can be performed using the RS-232C communication protocol.
The D-sub 9-pin connector for connecting the communication cable arranged on the rear panel of the unit is also used for RS-422A communication. It is switched by S961.
The data sent from the controller is input to the D-sub 9-pin connector on the rear panel of the unit and received by IC941.
The data received is converted to parallel data by IC921 and sent to the CPU for processing.

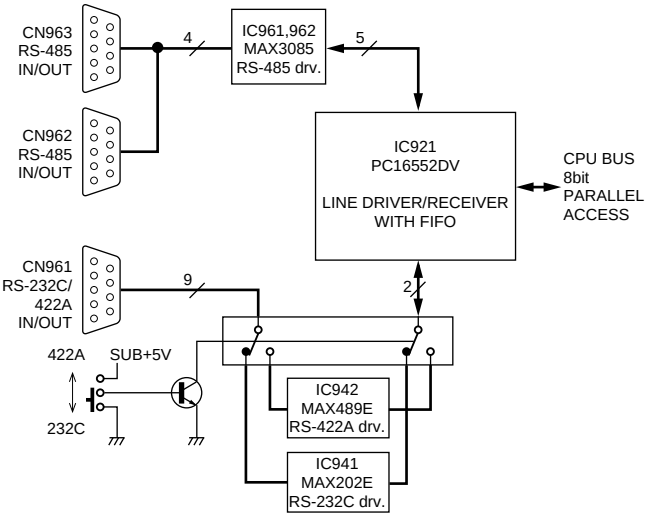


Fig. 17-11

17-8-2. RS-422A Communication (IC942)

Communication with the controller can be performed using the RS-422C communication protocol.
The D-sub 9-pin connector for connecting the communication cable arranged on the rear panel of the unit is also used for RS-232C communication. It is switched by S961.
The data sent from the controller is input to the D-sub 9-pin connector on the rear panel of the unit and differentiated by IC942.
The data differentiated is converted to parallel data by IC921 and sent to the CPU for processing.

17-8-3. RS-485 Communication (IC961, IC962)

Communication with the controller can be performed using the RS-485 communication protocol.
Two D-sub 9-pin connectors for connecting the communication cable are provided on the rear panel of the unit for RS-485 communication. As these are jumper-processed inside, there is no priority order.
The data sent from the controller is input to the D-sub 9-pin connector on the rear panel of the unit and differentiated by IC961 and IC962.
The data received is converted to parallel data by IC921 and sent to the CPU for processing.

17-8-4. INDEX Setting

The INDEX of the unit is set by the two rotary switches (S962, S963) on the rear of the unit.

17-9. CHARACTER & BUILT-IN TEST SIGNAL GENERATION BLOCK

The character & built-in test signal generation block is composed of the on-screen display controller (IC551, IC541, IC543, IC571 (part of PLD)), IC501 gate array, SRAM (IC502, IC503), TEST IRE signal generator (IC571 (part of PLD) and IC572), and PLL circuit (IC601 and IC602).

17-9-1. On-Screen Display Controller (OSDC ; IC551 MB90091AP)

The OSDC has a built-in memory for displaying (VRAM). It can configure an OSD screen of up to 24 characters × 12 lines at maximum and display images.
The dot structure of one character is 24 dots × 32 dots.
It can be equipped with an external character font memory and command table memory for storing display command data, thus reducing the burden on the control microprocessor sharply.
Normally, only 512 characters (64 Kbyte space) can be accessed from the external font memory as the data for writing in the VRAM.
But by using the external address expansion terminal (Pins 21, 22, 23 of IC551), 4096 characters (512 Kbyte space) can be fully accessed, this realizing display of 7 languages (English, French, German, Italian, Spanish, Japanese, and Chinese).
As the clock (dot clock) serving as the basis for displaying characters is 42 MHz at maximum, in order to realize multi-scanning, upper conversion and line conversion are required. These functions are realized by the IC501 gate array.

17-9-2. Character Font FLASH_ROM (IC543 MBM29F400BC-70 4M bit)

4096 types of character patterns (for 7 languages such as alphabets, numerals, Japanese characters, Chinese characters, title button of MENU screen, etc.) can be stored.
Although the control line of this IC is connected to the normal OSDC IC, when rewriting the internal data, connection is switched to the microprocessor (IC201) for control by the Bus SW (IC590 to 593, 595 to 597) so that new data can be down loaded by communication from outside the projector.

17-9-3. Command Table DUALPORT_RAM (IC541 IDT71321SA55J 16K bit)

The control microprocessor (IC201) writes the command data for composing the OSD screen in the DP_RAM (IC541) beforehand in the VD period.
After this, it sends a command to acquire this data to the OSDC to realize quick OSD display processing.

17-9-4. Gate Array (IC501 uPD65806GD-064)

Generates character and test signals synchronized to the frequency of the input signal from the clock (Pin 85 2 CLK) synchronized to the deflected horizontal signal HD and the vertical signal VD.
When no signals are input, its built-in signal generator for generating H-SYNC and V-SYNC from the external clock (20 MHz) generates character and test signals synchronized to this internal signal.
As 834 clock/1H is set as the dot clock for displaying the OSD character, when the maximum and maximum horizontal frequencies of the input signals are set to 15 kHz and 150 kHz (target value in design), the dot clock frequency becomes;
15 kHz × 834 clock = 12.5 MHz
150 kHz × 834 clock = 125.1 MHz

Consequently, an upper converter which can deal with 12 MHz to 130 MHz is required.
Upper conversion is realized by the IC601 and IC602 high band PLL and IC502 and IC503 SRAM.

17-9-5. SRAM (IC502, IC503 IDT71016S15Y)

To convert the OSD character signal from low frequency to high frequency, after writing the OSD character signal data in the SRAM at low frequency, it is read at high frequency.
The cycle time can be calculated as follows;
1 dot display time = (1/150 kHz)
834 clocks = 1/125.1 MHz = 7.99 nsec.
ROM capacity : 24 characters × 24 dots × 12 lines × 32 dots × 4 (R, G, B VOB1) = 884736 bits (approximately 1 Mbit)
Two SRAMs (Made by IDT : IDT71016S15Y) with the following specifications are used;
IDT71016S15Y : SRAM (64 k × 16 bit)
Cycle time : 15 nsec.
Memory capacity : 1048576 bit (1 Mbit)

As the data number is 4 (R,G,B,V), by performing serial-parallel conversion at 16 bits, the cycle time is as follows;
Cycle time = 7.99 nsec. × (16 bit/4) = 31.96 nsec.
Thus the SRAM specifications are satisfied.

Reading/Writing SRAM

The read/write SRAM is rewritten for every reading frame of IC551 (MB90091). Although read/write take-over occurs, OSD display is very slow compared to the vertical frequency, thus there are no problems as it can be taken to be the same as still images.

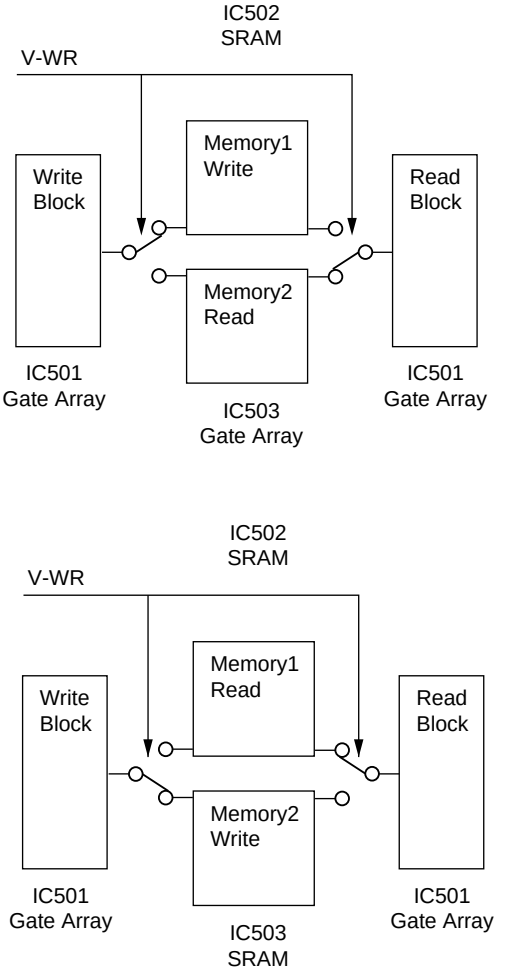


Fig. 17-12 Reading and Writing from/to SRAM

17-9-6. TEST IRE Signal Generator (IC571 (Part of PLD), IC572 MB86022PF)

The STAIR STEP signal data generated in the gate array (IC501) is throughed or converted to the PLUGE/0 IRE/10 IRE/100 IRE signal data by IC571, converted to analog signals by the D/A converter (IC572), and sent to the signal block board.

17-9-7. PLL Circuit (IC601 ; ICS1522M, IC602 : MC10H640FN)

The character and built-in test signals are generated by synchronizing with the HD and VD deflected by the PLL circuit.

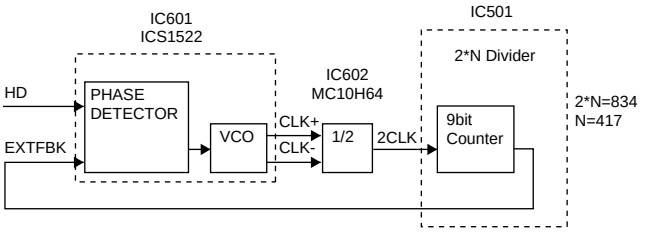


Fig.17-13 PLL Circuit Block

The HD from the deflection block is used instead of the input SYNC after the signal is passed through the AFC circuit because it helps eliminate jitters and noise components, stabilizes PLL operations, and prevents displayed characters from moving on the screen even after RGB-SHIFT adjustments.

17-9-8. 2 CLK Generator (IC602 MC10H640FN)

From the fact that the maximum dot clock frequency becomes approximately 130 MHz, there is a need to operate the circuit at 130 MHz at least.
The gate array (IC501) used in this unit can only operate at 65 MHz at maximum, therefore the internal operations of the gate array are parallel-processed at 2 CLK (1/2 of the PLL output clock frequency) and 2CLK is selected just before gate array output to realize superficial 130 MHz operations.

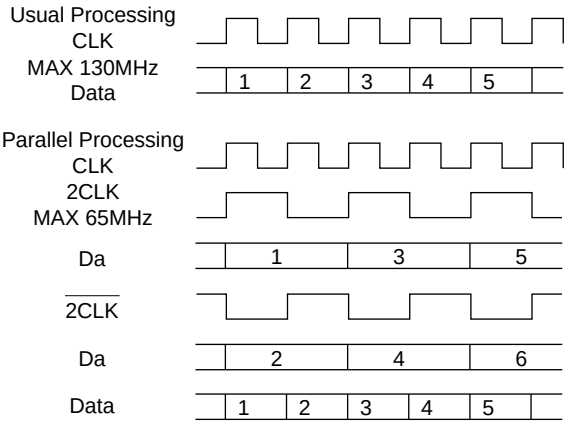


Fig. 17-14 Serial-Parallel Conversion

17-9-9. TTL-to-MECL TRANSLATOR (IC104, IC106)

The built-in test signal and character R/G/B signals are output from IC501. The maximum frequency is approximately 130 MHz.
For this reason, a driver IC (IC104, IC106) for sending these output signals to the signal block board is required. This helps realize display of clear built-in test signals and characters.

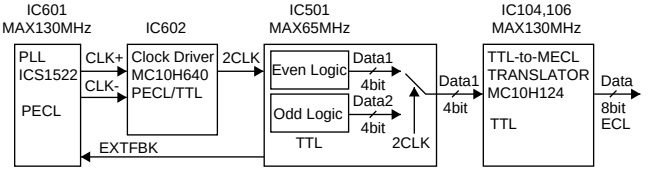


Fig. 17-15 Character & Built-in Test Signal Generation Block

17-9-10. VD Synchronizer (IC571 (Part of PLD), IC573)

The phase relation of HD and VD input to the YA board is random. Moreover, jitters occur in the range of 4.5 µsec. at maximum due to effects of the shift circuit.
As a result, V jitters may occur in the characters and built-in test patterns. The reason for this is because in the following phase relation, the scanning line counter (inside IC501) which clears jitters, as the HD determining the display position of the character hatch a clock, using VD increases/decreases by one count.

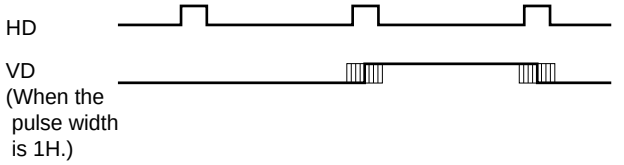


Fig. 17-16 HD, VD Timing

In the circuit provided, if VD drops when HD is high, the timing is determined to be as above, and the VD sent to IC501 is delayed by about 6 µsec. from the VD input. In the delayed state, when the timing is determined to be as above again, delay is stopped.

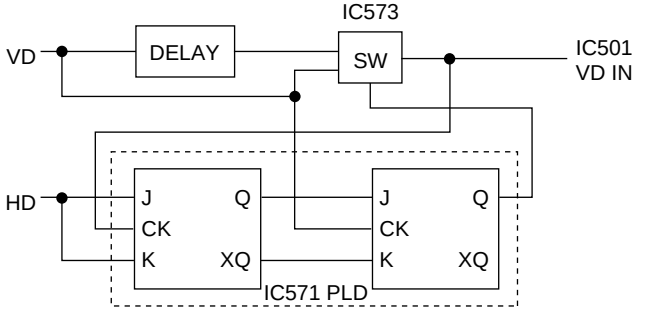


Fig. 17-17 VD Synchronizer Block

Jitters of characters, etc. have been resolved by synchronizing the VD to the HD by this circuit. The 6 µsec. value is determined from the minimum 1 H time (about 6.7 µsec at 150 kHz) and maximum jitter width (4.5 µsec.).

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