

CIRCUIT DESCRIPTION

DAUGHTER (PWC-4071)

1. Functions and specification

- Y/C separation of composite video signals
- VIDEO/S-VIDEO changeover
- RGB decoding
- Closed caption applicable
- Slots for optional input boards

Specification

- Video mode : NTSC, PAL, SECAM, NTSC4.43
- Y/C separation : Adaptive 3-line digital comb filter (NTSC, PAL)
Trap and band-pass filter (SECAM, NTSC4.43)
- Decoder block : Base-band signal processing system
(No adjustments required for the PAL and SECAM decoder circuits)

2. Circuit descriptions

The DAUGHTER board is composed of the Y/C separation block, the signal changeover block, the closed caption block, the signal processing decoder block, and the slot block.

The composite signal input entered in the Y/C separation block is identified as any one of the NTSC, PAL, SECAM, and NTSC4.43 signals through the discrimination for the vertical frequency of 50/60Hz and the color subcarrier of 3.58/4.43MHz. The resultant signal is processed at the Y/C separation block by the adaptive 3-line digital comb filter when it is an NTSC or PAL signal, or by the trap and band-pass filter when it is a SECAM or NTSC 4.43 signal. The adaptive 3-line digital comb filter is composed mainly of the digital comb filter IC (IC802), the 4fsc clock and clamp pulse generator (IC801), and the I/O low-pass filter (FL801 - FL803).

The signal changeover block is used to select a signal suitable for the discriminated video mode, from the signals obtained through the Y/C separation by the two systems of the adaptive 3-line digital comb filter and the trap and band-pass filter. Changeover between this selected signal and a signal from the S-VIDEO input terminal is carried out under the control from the SYSTEM board (selection by remote control). In this block, delay time compensation is also effected for the Y and C signals (DL701 - DL703, IC707).

In the closed caption block (IC301), when a video signal contains a closed caption signal, such a signal is decoded and then output as the R, G, B blanking signal so that the obtained text can be put into on-screen display. The output signal is superposed on the video signal at IC701 of the signal processing decoder block. The signal processing decoder block is used to convert the Y/C signal to the R, G, B, H, and V signals. It is composed of the I²C bus-controlled video-chroma-sync deflection processing IC (IC701), CCD delay line (IC702), and the pseudo flyback pulse generator block (IC703). Since this decoder circuit employs a baseband signal processing system, no adjustments of coils, etc., are required though such adjustments have been conventionally indispensable for the decoding of PAL and SECAM. The pseudo flyback pulse generator block is indispensable since IC701 (an IC used for television) is employed in the multi-sink PJ. A one-shot multi-vibrator is used to produce pseudo flyback pulses output from IC701.

The slot block is provided with two slots (DIN connectors) to be used when optional input boards are connected.

GAIN CTL PWB (PWC-4196)**1. Functions**

- Video/sync signal changeover
..... RGB/VIDEO/TEST
- Contrast control
- On-screen signal injection
- R.G.B ON/OFF
- Video blanking
- BRIGHT/WHITE uniformity
- Sync signal processing
..... Waveform shaping, G-SYNC/MIX-SYNC separation
- AKB reference signal generation/injection

2. Circuit descriptions

The GAIN CTL PWB can be outlined that it is in charge of video signal processing and sync signal processing.

① Video signal processing block (descriptions based on the circuit symbols of G-ch)

The RGB signal from the VIDEO MOTHER PWB, the VIDEO signal from the DAUGHTER PWB separated into RGB, and the built-in TEST signal from the SYSTEM PWB are respectively entered in the GAIN CTL PWB at 0.7Vp-p through the DIN "YM" connectors.

After these video signals have been terminated at 75Ω, they are selected by any one of Q7006 and others, and then entered in IC7009 through Pin 5. At this IC7009, various processings are carried out, such as contrast control, video blanking, and bright/white uniformity.

For contrast control, the lowest voltage is chosen from the following at the diode-OR circuit and entered in IC7009 through Pin 12:

Control voltage by remote control (D7028)

ABL voltage by total high voltage/current detection at HV PWB (D7026)

ABL voltage by high voltage/current detection for each CRT at VIDEO OUT PWB (D7027)

ABL voltage from another set when multiple PJs are connected through ABL links

For video blanking, pulses from the OSC PWB generated for the retrace time of vertical deflection, pulses from the SYSTEM PWB generated for the ON-screen time, and blanking control pulses from the WAVE PWB by remote control are synthesized at IC7006. Since then, the resultant signal input is entered in IC7009 through Pin 16.

At Pin 5 of the input block in IC7009, video signals of Q7087 and others are cut off by remote control, or turned ON/OFF by PICTURE MUTE.

After the above-mentioned processing in IC7009, video signals are output from Pin 24, and the on-screen and AKB signals are entered by Q7076 and others. Since then, the resultant signal is output from Pin 3 of the connector "GG" to the CRTOUT PWB at 0.7Vp-p/75Ω.

② Sync signal processing block

The sync signal of the RGB signal from the VIDEO MOTHER PWB and the sync signal of the VIDEO signal from the DAUGHTER PWB are entered in the GAIN CTL PWB through the DIN "YM" connectors. These signals are amplified at H:Q7051, V:Q7054, and others, and then applied respectively to Pin 6 (H) and Pin 8 (V) of IC7012. To separate the G-SYNC signal, the video signal of G-ch is amplified at Q7048 and others, and applied to Pin 4 of IC7012.

In IC7012, polarity discrimination of input sync signals is effected, in addition to waveform shaping of sync signals (TTL arrangement) and sync separation of MIX-SYNC/G-SYNC. The result of polarity discrimination is used as data for signal discrimination at the SYSTEM PWB.

The sync signal outputs from Pin 15 (H) and Pin 14 (V) of IC7012 are sent to the OSC PWB in the Negative/TTL mode.

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VIDEO OUT PWB (PWC-4191)

1. Functions

- AKB control
- Brightness control
- White balance adjustment
 - ... Drive-cathode G1 voltage amplitude, bias-G2 voltage

2. Circuit descriptions

The VIDEO OUT PWB has a control circuit for white balance adjustment including AKB/BRIGHT.

The waveform of cathode current detected by the CRTOUT PWB is taken from the DIN connector "YV" and entered in the VIDEO OUT PWB.

This cathode current waveform is buffer-processed by Q7423 and others, and the ABL voltage output is sent to the GAIN CTL PWB by IC7506 and others so that the mean value of each CRT cathode current is maintained below 1.4mA.

To perform AKB control, the buffer-processed cathode-current waveform is input in the sample hold circuit consisting of Q7424 and others. This process is needed to take out a constant amount of reference current from the cathode in the form of a DC voltage, by performing sample hold at a timing when a reference signal is injected during the 1H period shortly after the completion of V-blanking in the GAIN CTL PWB. The sample-hold voltage is compared with the reference voltage by IC7506 and others, in order to control the G2 AMP circuit on the HV PWB. As a result, the G2 voltage changes and a feedback loop functions to maintain a constant cathode current.

The G2 voltage is also affected by brightness control and cut-off control during white balance adjustment. At that time, the amplitude of reference voltage applied to the GAIN CTL PWB is changed.

The D/A converter of IC7702/03 is available on the VIDEO OUT PWB, so that G2 voltage control (BRIGHT BIAS/BRIGHT GAIN, etc.) for white balance adjustment and cathode•G1 voltage amplitudes (VR7505 only for G-ch) can be adjusted with the remote control.

CRTOUT PWB (PWC-4192) / AMP PWB (PWC-4198)

1. Functions

- Video AMP
 - ... Amplifying the 0.7Vp-p video signal input from the GAIN CTL PWB to the following voltages:
 - Cathode electrode : Approx. 70Vp-p Negative
 - G1 electrode : Approx. 70Vp-p Positive ($A_v=100 \times 2$)
- In addition to the above cathode and G1 voltages, heater voltage (6.3V) from the power unit and G2 voltage (300 - 1000V) from HV PWB are fed to the CRT.

2. Circuit descriptions

For the CRTOUT PWB, three boards are respectively mounted on the neck of each R/G/B CRT. The circuit configuration of each CRTOUT PWB for R/G/B is almost identical with each other. However, since the circuit constants of parts are different, a relevant CRTOUT PWB for each color should be used in the case of board replacement.

Descriptions will be given below, using the circuit symbols of the G CRTOUT PWB.

The video signal of 0.7Vp-p output from the GAIN CTL PWB at 75Ω is entered in the CRTOUT PWB through the coaxial cable connector "GG" and terminated at 75Ω.

This video signal is divided into the Posi signal and the Nega signal. The Posi signal is for the cathode, obtained from transistor Q7909G casode-connected to Pin ⑮ of IC7923. The Nega signal is for the G1 gained through Q7911G from Pin ⑭. Each signal is amplified to approximately 2.2Vp-p and then output. Voltage at Pin ⑧ of IC7921, which is a cathode output signal, is resistance-divided and returned to Pin ③ of IC7923. By comparing

this voltage with the voltage at Pin ④, with a timing of clamp pulses (TTL/positive) entered in Pin ②, a feedback loop becomes effective so that the DC reproduction of the cathode voltage waveform is kept constant.

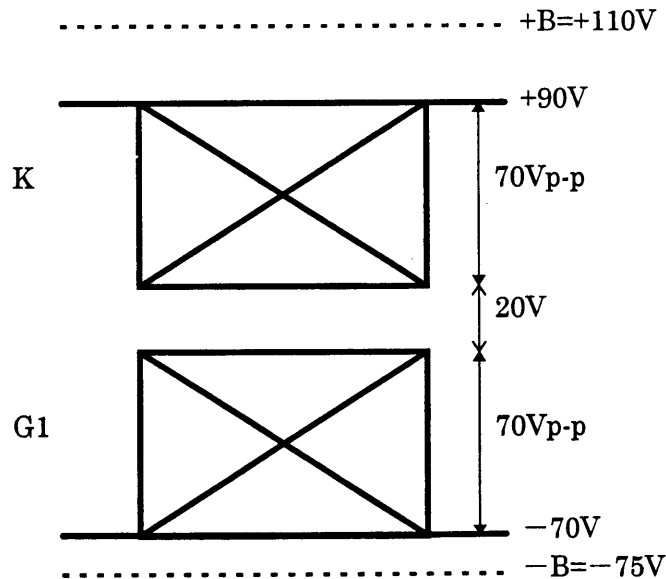
These two signals are respectively amplified to about 5Vp-p, by the sub-boards K AMP PWB and G1 AMP PWB, standing right and left. For the G-ch, gamma compensation processing is effected at each sub-board to crush the signal's peak, in order to improve the white balance contrast tracking characteristics.

The output from each sub-board is polarity-reversed and amplified up to about 70Vp-p by the video pack IC7921 for the cathode and the video pack IC7922 for the G1. The cathode generates a negative waveform, while G1 generates a positive waveform.

After being output from IC7921, the cathode voltage passes through the cathode current detector circuit of Q7903G and is then fed to the cathode electrode of the CRT. According to the amount of cathode current detected here, AKB and single-tube ABL are controlled on the VIDEO OUT PWB. The voltage waveform appearing at the cathode electrode is maintained at +90V_{DC} for the black level, and its amplitude is about 70Vp-p.

The G1 voltage output from IC7922 is processed for DC cut at C7912G. Since then, it is minus-biased by the pedestal clamp circuit consisting mainly of Q7907G, and fed to the G1 electrode of the CRT. The voltage waveform appearing at the G1 electrode is about -70V_{DC} for the black level, and its amplitude is about 70Vp-p.

- Voltage waveforms at the cathode and G1 electrodes are as follows:



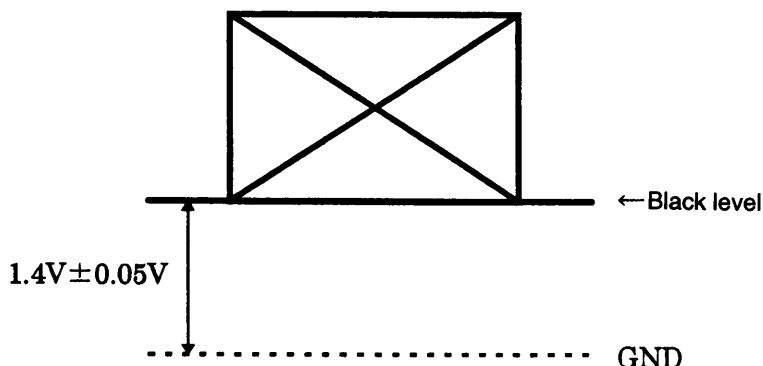
As a phenomenon to be seen when the CRTOUT PWB is out of order, the CRT back raster of that color may look as if it were floating. In some cases, a high-voltage beam protector may function to trip the power supply. In such a case, the CRTOUT PWB of that color is out of order if either of each black level cathode (+90V) or G1 (-70V) has been lowered.

When the back raster is normal but the CRT of that color is dark, or when the amplitude of input signal is normal (GAIN CTL PWB - R: TP7013, G: TP7012, B: TP7011 - Each 0.7Vp-p) but the voltage amplitude of either cathode or G1 electrode is small, the CRTOUT PWB of that color can also be abnormal. Since this circuit is designed so that the cathode and the G1 can have almost the same voltage amplitudes, a great difference between these amplitudes can be a standard for fault diagnosis. The voltage amplitude is 70Vp-p in the standard state where the contrast is 100% and the signal is without ABL effects (cross-hatch, etc.). The possible deviation is 50 ~ 70Vp-p according to white balance adjustments.

When checking these voltage waveforms, the G1 electrode is located atop the PWB and it is therefore possible to apply an oscilloscope probe to the terminal of the CRT socket. Check the silk printing of the PWB. When examining the cathode electrode, the C7920G lead is located where application of the probe is easy to carry out.

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When the CRTOUT PWB has been replaced, check the waveform at TP7921 at with oscilloscope and adjust VR7921 until the black level attains $1.4V \pm 0.05V$.



WAVE PWB (PWC-4193)

1. Functions

- Establishment and control of FOCUS compensation waveform
- Establishment and control of ASTIG compensation waveform
- Establishment and control of Analog ALIGNMENT compensation waveform
- Establishment and control of BLANKING adjustment pulses
- Establishment and control of CENTERING adjustment DC voltage

2. Circuit descriptions

① Basic waveform generating block

A waveform generator IC (CXA1470) of IC9001 is used.

Four types of basic waveforms are produced; horizontal saw-teeth, horizontal parabolic, vertical saw-teeth, and vertical parabolic, synchronized with horizontal and vertical pulses entered in the IC.

② FOCUS compensation waveform generator and control block

A waveform necessary for compensation is established by the use of the standard waveform and the multiplication IC (CXA1726). The signal level is controlled by the ANALOG D/A converter (MP7670). The compensation data are entered in D/A from the SYSTEM board. The D/A has independent waveforms for red, green, and blue, and the level-controlled compensation waveform is added with these waveforms and then fed to the F-DRIVE.

The compensation waveforms output from the connector POWA are as follows:

- 16B Red dynamic FOCUS compensation waveform
- 16A Green dynamic FOCUS compensation waveform
- 15B Blue dynamic FOCUS compensation waveform
- 15A Red center FOCUS compensation waveform
- 14B Green center FOCUS compensation waveform
- 14A Blue center FOCUS compensation waveform

③ ASTIG compensation waveform generator and control block

A waveform necessary for compensation is established by the use of the standard waveform and the multiplication IC (CXA1726). The signal level is controlled by the ANALOG D/A converter (MP7670). The compensation data are entered in D/A from the SYSTEM board. The D/A has independent waveforms for red, green, and blue, and the level-controlled compensation waveform is added with these waveforms and then fed to the A-DRIVE.

The compensation waveforms output from the connector POWA are as follows:

- 4A Vertical (HV) red ASTIG compensation waveform
- 4B Vertical (HV) green ASTIG compensation waveform
- 5A Vertical (HV) blue ASTIG compensation waveform
- 5B Skew (SK) red ASTIG compensation waveform
- 6A Skew (SK) green ASTIG compensation waveform
- 6B Skew (SK) blue ASTIG compensation waveform

④ ALIGNMENT compensation waveform generator

A multiplication IC (CXA1726) is used to produce an analog-controlled ALIGNMENT compensation waveform from the basic waveform in the D-CONV board.

Level control is effected in the D-CONV board, while generation of waveforms only is effected in the WAVE.

The compensation waveforms output from the connector POWA are as follows:

- 9A Horizontal parabolic waveform
- 9B Horizontal parabolic x vertical saw-tooth waveform
- 23B Horizontal saw-tooth waveform
- 23C Vertical saw-tooth waveform
- 24B Horizontal saw-tooth x vertical saw-tooth waveform
- 24C Vertical parabolic waveform
- 25C Horizontal saw-tooth x vertical parabolic waveform

⑤ DC voltage control block

Using a D/A converter (M62352) for DC voltage control, ALIGNMENT AMPLITUDE adjusting voltage, CENTERING adjusting voltage, BLANKING adjusting pulses, etc., are generated. The compensation data are sent from the SYSTEM board to D/A.

The control waveforms output from the connector POWA are as follows:

- 19C Horizontal AMPLITUDE control voltage
- 13B Horizontal red CENTERING control voltage
- 13A Horizontal green CENTERING control voltage
- 12B Horizontal blue CENTERING control voltage
- 12A Vertical red CENTERING control voltage
- 11B Vertical green CENTERING control voltage
- 11A Vertical blue CENTERING control voltage
- 29C BLANKING adjusting pulses

CIRCUIT DESCRIPTION

D-CONV PWB (PWC-4190)

1. Functions

- Generation and control of digital CONVERGENCE compensation waveforms
- Generation and control of digital ALIGNMENT compensation waveforms
- Control of analog ALIGNMENT compensation waveforms

2. Circuit descriptions

① CPU block

This is the central part of all functions available in D-CONV.

The IC to be used is μ PD71055 (IC8301) of PLCC84pin.

This block is maintaining communication with the CPU of the SYSTEM board. When the compensation values of ALIGNMENT and CONVERGENCE are sent from the SYSTEM, the compensation waveforms for them are generated and controlled, and the resultant output is sent to the C-DRIVE board.

② Memory block

This block has the work area, calculation area, program area, and store area, where various digital compensation waveforms are generated and controlled.

The software program used to actuate the D-CONV functions is accommodated in the 4M flash ROM (IC8308).

The point compensation waveform data of ALIGNMENT and CONVERGENCE are stored in the memory of D-CONV. However, other compensation waveform data of ALIGNMENT and CONVERGENCE are stored in the memory of the SYSTEM board.

③ Waveform generator and control block (Digital compensation waveform)

This block is composed of the OUTRAM used to store the compensation waveform controlling data, the G/A (gate array) intended to produce digital data of compensation waveforms based on the stored data, and the D/A converter used to convert digital data into compensation waveforms.

It is divided into two systems of horizontal and vertical, each performing the same circuit operation. The G/A generates three types of data outputs, red CONVERGENCE, blue CONVERGENCE, and ALIGNMENT. These data are converted into compensation waveforms at the D/A.

The horizontal and vertical ICs are as follows:

• Horizontal direction:

OUTRAM IC8331, IC8332

G/A IC8333

D/A IC8351

• Vertical direction:

OUTRAM IC8341, IC8342

G/A IC8343

D/A IC8361

The periodic clock is 256 times the horizontal frequency entered from the SYSTEM board to the OUTRAM. If this clock is incorrect, these digital compensation waveforms are not output normally.

④ Waveform control block (Analog compensation waveform)

Using the waveforms established in the WAVE board, part of ALIGNMENT adjusting waveforms are controlled by the analog D/A (IC8371).

⑤ Waveform adder block

The digital compensation waveforms established and controlled at the block of (3) above are added to the analog compensation waveforms controlled at the block of (4) above, and the resultant signal is output to the C-DRIVE board.

The compensation waveforms output from the connector POWA are as follows:

- 1A Horizontal red CONVERGENCE compensation waveform
- 1B Horizontal ALIGNMENT compensation waveform
- 2A Horizontal blue CONVERGENCE compensation waveform
- 2B Vertical red CONVERGENCE compensation waveform
- 3A Vertical ALIGNMENT compensation waveform
- 3B Vertical blue CONVERGENCE compensation waveform

3. Complement

Digital/Analog Distinction Table for ALIGNMENT Compensation Waveforms

Horizontal direction	Compensation waveforms	Vertical direction	Compensation waveforms
SKEW	Analog	TILT	Analog
BOW	Analog	BOW	Analog
LINEAR	Analog	LINEAR	(*)
KEYSTONE	(*)	KEYSTONE	Analog
PINCUSHION	(*)	PINCUSHION	Analog
LINEAR-BAL	Digital	LINEAR-BAL	(*)
KEY-BALANCE	Digital	KEY-BALANVE	Analog
PIN-BALANCE	Digital	PIN-BALANCE	Digital
LINE. DIST (EDGE)	(*)	LINE. DIST (EDGE)	Digital
		LINE. DIST (CENTER)	Digital

(*) Adjusting items established and controlled in the WAVE board

CIRCUIT DESCRIPTION

OSC PWB (PWC-4189)

1. Functions and performance

- Horizontal sync processing and various timing generation
- Vertical sync processing and various timing generation
- Video blanking waveform generation
- Horizontal deflection control
- Horizontal/vertical frequency count
- FOCUS PHASE adjustment
- POSITION adjustment

2. Outline circuit operation

① Horizontal oscillator block

Horizontal sync oscillation is effected with IC5728 (μ PC1883).

Horizontal sync input (HSIN) from the GAIN CTL PWB is converted by the F/V converter (IC5713), from frequency to voltage. The obtained voltage signal is sent to the CPU (IC5701) through the A/D converter (IC5714) and the output voltage from the D/A converter (IC5772) is applied to Pin 19 of IC5728. Thus, oscillation takes place at a frequency that is almost identical with the input frequency.

The oscillation sync signal is output toward the H-DEF PWB (HDRIVE) and further looped to the CPU through IC5707.

While data are taken in the CPU, horizontal deflection control (DY/FET changeover, voltage amplitude control, etc.) is conducted by software according to the input frequency.

② Vertical oscillator block

Vertical sync oscillation is effected with IC5723 (μ PC324).

Vertical sync input (VSIN) from the GAIN CTL PWB is entered via the V-POSITION adjusting circuit. The oscillation sync output is sent to the V-DRIVE PWB (VPP) and WAVE PWB (VPULSE). During free run, oscillation is maintained at about 40Hz.

③ Blanking waveform generator block

The horizontal block generates a blanking waveform based on the flyback pulse (FBP1) from the H-DEF PWB, and the vertical block generates a blanking waveform based on the blanking pulse (DEFVBLK) from the V-DRIVE PWB. These waveforms are output to the GAIN CTL PWB.

④ Focus phase and position adjustment

Based on the compensation data controlled by the SYSTEM PWB, the respective adjusting values of FOCUS PHASE and POSITION are output via the D/A converter (IC5711).

Under the control from the SYSTEM PWB, the V-POSITION is changed over to the WIDE mode or the NARROW mode.

The NARROW mode is used when entering an interlace signal or in the case of picture error.

3. Miscellaneous

① Volume control (VR5711)

This device is used for oscillation bias adjustment of μ PC1883 (IC5728), which is an IC for horizontal sync oscillation. It has already been adjusted at the time of shipment from the factory. The oscillation characteristics of horizontal frequency can be changed by adjusting this VR. No readjustment is needed in the field.

② Switch (S5701)

A reset switch for the CPU (IC5701).

③ Switch (S5702)

An ON/OFF switch for the WATCHDOG TIMER circuit of the CPU (IC5701). This switch is always set at OFF. If it is set at ON at the time of power ON, the CPU does not function.

④ Switch (S5703)

A switch for board adjustment. When it is depressed during picture projection, the horizontal sync signal flows. It can be reset when depressed again.

⑤ Switch (S5704)

A switch for board adjustment. This switch is always set at OFF. If it is set at ON at the time of power ON, LED (D5702) flashes and the sync signal flows.

A-DRIVE

1. Principle of basic operation

Various compensation waveforms of ASTIG for Center, Edge, and Corner, input from the WAVE PWB, are converted into voltages and currents. The ASTIG Mg coil in the FOCUS Mg is driven to trim the shape of beams on the CRT screen.

2. Protector

① $\pm 35\text{V}$ line voltage detection protector

Operation

When either of $\pm 35\text{V}$ line voltages is unusually lowered, an FA indication is given to the 7-seg and the power supply is shut down.

② $\pm 35\text{V}$ line current detection protector

Operation

When either of $\pm 35\text{V}$ line currents exceeds DC 2A, an FA indication is given to the 7-seg and the power supply is shut down.

F-DRIVE

1. Principle of basic operation

The F-DRIVE is composed of an AMP intended to drive the STAIC Mg coil in the FOCUS Mg through conversion of various compensation waveforms for Center, Upper/Lower Edge, and Focus, input from the WAVE PWB, into voltages and currents, and also another AMP intended to perform focus arrangement on the CRT screen by driving the DYNAMIC Mg coil in the FOCUS Mg through conversion of various compensation waveforms for FOCUS of Right/Left Edge and Corner into voltages and currents.

A tracking circuit is provided between the STAIC circuit and the DYNAMIC circuit, in order to establish a configuration so that the Center focus is not damaged by DYNAMIC compensation.

2. Protector

① $\pm 35\text{V}$ line voltage detection protector

Operation

When either of $\pm 35\text{V}$ line voltages is unusually lowered, an F9 indication is given to the 7-seg and the power supply is shut down.

② $\pm 35\text{V}$ line current detection protector

Operation

When either of $\pm 49\text{V}$ line currents exceeds DC 2A, an F9 indication is given to the 7-seg and the power supply is shut down.

CIRCUIT DESCRIPTION

C-DRIVE

1. Principle of basic operation

Various compensation waveforms for R, G, B, input from the D,CON PWB, are converted into voltages and currents. The CONV yoke (CY) in the deflection yoke is driven to arrange convergence on the CRT screen.

2. Protector

① $\pm 35\text{V}$ line voltage detection protector

Operation

When either of $\pm 35\text{V}$ line voltages is unusually lowered, an F8 indication is given to the 7-seg and the power supply is shut down.

② $\pm 35\text{V}$ line current detection protector

Operation

When either of $\pm 35\text{V}$ line currents exceeds DC 2A, an F8 indication is given to the 7-seg and the power supply is shut down.

V-DRIVE

The V-DRIVE PWB consists of the vertical deflection circuit block and the horizontal-centering circuit block.

1. Principle of basic operation

① Vertical deflection circuit block (V-DEF)

Vertical deflection waveforms (V.SAW + V.LIN + V.LINE BALANCE) entered from the WAVE PWB and the R,G,B vertical-centering compensation waveforms are added at the pre-AMP, and then converted into voltages and currents at the vertical output-stage AMP. By independently driving the R,G,B vertical yokes (V-DY) in the deflection yoke, it is possible to perform both vertical deflection and vertical raster shift. The circuit configuration is made so that the ceiling type and the floor type can be switched over to each other by remote control through changeover between the pump-up circuit for minus power supply in the output-stage AMP and the pump-up circuit for plus power supply.

The trigger pulses for vertical blanking are output toward the OSC PWB.

② Horizontal-centering circuit block (H-Centering)

Horizontal raster shift can be performed through voltage/current conversion of the RGB horizontal-centering compensation waveforms entered from the WAVE PWB, and by driving the centering yoke (CY2) in the deflection yoke.

2. Protector

③ Vertical deflection circuit block (V-DEF)

Vertical yoke connector detection protector

Operation

If the vertical yoke connector is not connected to the P-board terminals, a b0 indication is given to the 7-seg and the set is not turned on (for CRT protection).

Vertical swing protector

Operation

When the vertical swing is $0.5A_{p-p}$ or below, and if an abnormal DC is superposed on the vertical deflection waveform (V.SAW + V.LIN + V.LINE BALANCE) entered from the WAVE PWB, a b2 indication is given to the 7-seg and the power supply is shut down (for CRT protection).

④ Horizontal-centering circuit block (H-Centering) protector

Operation

If any abnormality arises in the Horizontal-centering circuit block (H-Centering), an F8 indication is given to the 7-seg and the power supply is shut down.

H-DEF (PWC-4069)

1. Functions and specifications

Functions:

- Horizontal deflection output
- Horizontal retrace time changeover (AUTO)
- Side-pin cushion, keystone compensation
- Horizontal deflection stop detection
- Horizontal deflection polarity reversal by connector exchange

Specifications:

- Horizontal frequency: 15 ~ 135kHz (for XG-1351)
- Horizontal retrace time: 6.0 μ S (15 ~ 30kHz)
2.6 μ S (30 ~ 77kHz)
2.0 μ S (77 ~ 120kHz)
1.4 μ S (120 ~ 135kHz)
- Source voltage for horizontal deflection output stage: Approx. 20 - 180V (changed by frequency and amplitude)

2. Circuit descriptions

The H-DEF board is composed of the horizontal deflection block that is controlled by the OSC board (PWC-4189), the source block where the side-pincushion/keystone compensation waveforms generated by the WAVE board (PWC-4193) are amplified and superposed on the source voltage of the horizontal deflection output block, and the horizontal deflection stop detection block where conditions of horizontal deflection stop and horizontal-deflection yoke connector draw-out are detected and a MUTE request is made.

The horizontal deflection block is composed of the following blocks: the pulse conversion block (IC5181) that converts the horizontal drive pulses (duty 50%) output from the OSC board into pulses with an optimal pulse width (almost identical with the retrace time) suitable to drive the horizontal output FET, the horizontal output FET drive block consisting of the photo-coupler (IC5101, IC5102) that changes the output pulses of the pulse conversion block from GND standard to floating-voltage standard and the horizontal output FET driving ICs (IC5103, IC5104), the switching source block (T5101, Q5111) used to generate and feed power to the horizontal output FET drive block utilizing the horizontal drive pulses, and the deflection output block consisting of the output FET (Q5101 ~ Q5110), the resonance capacitors (Q5101, Q5101B, Q5102, Q5102B, Q5103, Q5103B), the horizontal output choke coil (L5101), the linearity compensation coils (L5102, L5103), and the series/parallel connection changeover relays (RL5101 ~ RL5105). Horizontal retrace time changeover is effected by series/parallel connection changeover relays to exchange the connections of resonance capacitors and the horizontal deflection yoke coils. Such changeover is also controlled by the OSC board.

The source block is composed of the waveform amplifier block (IC5204, IC5205) that amplifies the output compensation waveform of the WAVE board to a required level according to the horizontal frequency and amplitude, the clamp block (Q5156, Q5157, etc.) that clamps the peak part of the amplified compensation waveform at the horizontal deflection source voltage supplied from the PS-UNIT, and the output block (IC5151, Q5151 ~ Q5154) that supplies to the horizontal deflection block a horizontal-deflection source voltage on which a compensation waveform is superposed.

The horizontal deflection stop detection block is composed of the current detection transformer (T5102 ~ T5104) that detects the horizontal deflection current, the reversal AMP (IC5301) used as a buffer for the secondary output circuit of the above-mentioned transformer, the double voltage rectifier circuit (peripheral circuit of D5242 ~ D5247) for the peak rectification of saw-tooth currents output from the reversal AMP, the comparator circuit (IC5209) that judges the proper flow of a horizontal deflection current through comparison between double-voltage-rectified voltage and the reference voltage, and the red LED (D5251) that is used to indicate deflection stop.

POWER SUPPLY UNIT

1. Functions and performance

- PFC (harmonic-related measures) circuit
 - T6601 (110V, 15.5V, -16V, 75V)
 - T6602 (150V, $\pm 5V$, +5V(D), 6.3V)
 - T6603 (5V(S))
 - T6604 (20 - 200V)
 - T6605 (± 35 , $\pm 49V$)
 - Overvoltage, overcurrent protection circuit
- 5-transformer, 15DC output

2. Outline circuit operation

① PFC (harmonic-related measures) circuit

This is a step-up converter circuit composed of a choke coil (L6504), switching transistors (Q6501, Q6502), a rectifier diode (D6503), and rectifier capacitors (C6511, C6512). This circuit is used to detect AC input currents and voltages at both electrodes of rectifier capacitors and control the switching transistor duties to decrease the harmonic component of the input current. Voltages of the rectifier capacitors are DC240V ~ 320V (Models XG-1351, XG-1101, XG-751) and DC300V ~ 400V (Models XG-1351G, XG-1101G, XG-751G).

② 110V, 15.5V, -16V, and 75V circuits

This is a DC/DC flyback converter circuit consisting of a control IC (IC6701), a switching transistor (Q6601), a flyback transformer (T6601), rectifier diodes (D6609 ~ D6612), rectifier capacitors (C6608, C6612 ~ C6614, C6616, C6617, C6620), and a pseudo-resonance capacitor (C6604). IC6701 for control is a controller for primary pseudo-resonance control. For output voltage control, 110V and 15.5V are detected by resistors R6617 and R6618, the voltage divided by the resistor R6717 and the volume control VR6703 is applied to the reference terminal of the shunt regulator IC6703, the signal compared by the comparator in this IC is transmitted to Pin ⑨ of the primary IC6701 through the photo-coupler (PC6701), and the voltage at the reference terminal of IC6703 is controlled to 2.5V by controlling the ON/OFF duty of the switching transistor by this signal.

③ 150V, $\pm 5V$ +5V (D), 6.3V circuits

This is a DC/DC flyback converter circuit composed of a control IC (IC6702), a switching transistor (Q6602), a flyback transformer (T6602), rectifier diodes (D6615 ~ D6618), and rectifier capacitors (C6626, C5528, C6629, C6633 ~ C6635, C6638 ~ C6640). The control IC6702 is a PWM controller for primary control. For output voltage control, 150V is detected by the resistor R6635, the voltage divided by the resistor R6725 and the volume control VR6702 is applied to the reference terminal of the shunt regulator IC6704, the signal compared by the comparator in this IC is transmitted to Pin ⑧ of the primary IC6702 through the photo-coupler (PC6703), and the voltage at the reference terminal of IC6704 is controlled to 2.5V by controlling the ON/OFF duty of the switching transistor by this signal.

④ 5V (S) standby source circuit

This is an RCC power source composed of a switching transistor (Q6606), a flyback transformer (T6603), a rectifier diode (D6630), and a rectifier capacitor (C6649).

For output voltage control, 5V (S) is detected by the resistor R6766, the voltage divided by the resistor R6765 and the volume control VR6751 is applied to the reference terminal of the shunt regulator IC6752, the signal compared by the comparator in this IC is transmitted to the base of the primary transistor Q6751 through the photo-coupler (PC6751), and the voltage at the reference terminal of IC6751 is controlled to 2.5V by controlling the oscillation frequency of the switching transistor by this signal.

⑤ 20 ~ 200V variable (F/V) circuit

From this circuit, a voltage about 20 times the input voltage of CTL (connector: Pin ③ of PS) is output to +B HDEF (connector: Pin ① of PS). This circuit is a DC/DC flyback converter circuit composed of a control IC (IC6751), a switching transistor (Q6607), a flyback transformer (T6604), rectifier diodes (D6633, D6634), and rectifier capacitors (C6656, C6658, C6659). The control IC6751 is a PWM controller used for primary control. For the control of output voltage +B HDEF, this voltage is detected and compared with the CTL voltage, the compared signal is transmitted to Pin ⑧ of the primary IC6751 through the photo-coupler (PC6751), and the output voltage is regulated by controlling the ON/OFF duty of the switching transistor by this signal.

⑥ $\pm 35V$, $\pm 49V$ circuit

This is a DC/DC flyback converter circuit composed of a control IC (SUB6601), a switching transistor (Q6609), a flyback transformer (T6605), rectifier diodes (D6639 ~ D6642), and rectifier capacitors (C6667, C6668, C6670 ~ C6672, C6674 ~ C6676, C6678, C6679). The control SUB6601 is a PWM controller for primary control. For output voltage control, 35V is detected by the resistor R6684, the voltage divided by the resistors R6666 and R6667 is applied to the reference terminal of the shunt regulator IC6703, the signal compared by the comparator in this IC is transmitted to Pin ② of the primary SUB6601 through the photo-coupler (PC6601), and the voltage at the reference terminal of IC6704 is controlled to 2.5V by controlling the ON/OFF duty of the switching transistor by this signal.

⑦ Overvoltage, overcurrent protection circuits

⑦-1. Overvoltage protection

The flyback transformers T6601, T6602, T6603, and T6605 are provided with overvoltage protection circuits. When output voltage is detected on the secondary side and any abnormality is found, all secondary output voltages are lowered except the standby source of 5V (S) and this leads to oscillation stop and the condition is latched. To reset this latching condition, Hi (5V) ∇ Lo (0V) is applied to PWBIT (Connector: Pin ② of MS).

⑦-2. Overcurrent protection

Source and emitter currents of the switching transistor in the primary circuit are detected for each flyback transformer (T6601 ~ T6605). When an overcurrent is sensed, the protection circuit operates to lower the output voltage.

When a state of output-voltage lowering continues for few seconds in the transformer output circuit of T6601, T6602, T6604, or T6605, all secondary output voltages are lowered except the standby source of 5V (S) and this leads to oscillation stop and the condition is latched.

This operation of latching is effected in the same circuit as for the protective operation against overvoltages. Resetting is effected in the same procedure to cancel the latching condition.

For overcurrent protection of +5V (D) and +6.3V outputs, operation is contained in Character V domain of the 4-terminal regulator. Therefore, lowering is effected to a degree of that line.

CIRCUIT DESCRIPTION

HVFBT PWB (PWC-4077)

1. Functions and performance

- Anode power supply
(32kV / 3.2mA in High brightness mode, 2.1mA in Normal mode, and 1.4mA in Long life mode)
- Voltage supply to Grid 2 of CRT (300 - 1000V, adjusted by remote control)
- High-voltage protection circuit
- Fan driving circuit
- Operating status output (presence of anode power supply, anode current value, fan stop detection)

2. Outline circuit description

① High-voltage generator block

This block is of two flyback type HV generator circuits, composed of flyback transformers (T5503, T5504), resonance capacitors (C5534, C5544), switching transistors (Q5516, Q5518), S-capacitors (C5535, C5545), and choke coils (L5503, L5504). To secure high output and high stability, this circuit is set at an oscillation frequency (about 40kHz) where flyback transformers can efficiently function. It is not synchronized with the horizontal deflection circuit. To achieve HV stabilization, an FM (frequency modulation) system is adopted, by which the voltage feed back from the HV-BLOCK (KS, KR connectors) is compared with the reference voltage (IC5503) by the comparator (IC5502), in order to change the oscillation frequency of the oscillator (IC5501). The source used is 150V supplied from Pin 1 of the HP connector.

The anode current is converted into a voltage by the use of a resistor (R5543) taking a current from a high-voltage inflow of the flyback transformer, and is then output to TP5507. Therefore, the anode current can be easily obtained by dividing the voltage value at this test pin by a resistance value of 470. The obtained voltage is applied to the GAIN-CTL board through Pin 6 of the YH connector to form a closed loop of ABL (Auto Brightness Limiter). By controlling the contrast, the mean value of anode current is limited to a constant level. For this ABL value, the average current is controlled by a combination of two switches (S5501, S5502). There are three modes of high brightness (high bright mode), ordinary (normal mode), and long life (long life mode). At the time of shipment from the factory, the setting is made in the normal mode. The high bright mode can be chosen, as required. However, this setting shortens the CRT life and burning of the glowing plane can occur. This should be borne in mind during practical use. Since average current is suppressed, the average brightness is lowered, but the CRT life can be prolonged in the case of a long time of continuous use for supervision, etc. Use in the normal mode is recommendable. It must be noted regarding the above-mentioned switches that operation cannot be confirmed if signals are generally bright as in the case of all-white signals and the contrast does not stay around the maximum position.

② Grid2 voltage supply block

Flyback pulses of about 1250Vp-p are extracted from the secondary coil of the above-mentioned choke coils (L5503, L5504), rectified by diodes (D5550, D5551, D5552, D5553) and a capacitor (C5562). The control voltages (Pins 3, 4, 5) entered from the GAIN-CTL board via the YH connector are amplified by the AMP (IC5504, Q5501R, Q5501G, Q5501B), working with the above-mentioned source voltage of 1250V. The amplified voltage is fed to Grid2 of the CRT.

Control voltage is generally 6V and output voltage is about 510V.

③ High-voltage protection circuit

This circuit is provided with the following 4 protectors related to high voltages:

- 1)..... PROTECT (1) HV overvoltage protector
- 2)..... PROTECT (2) Flyback overvoltage protector
- 3)..... Overcurrent protector 1 Anode overcurrent protector
- 4)..... Overcurrent protector 2 Primary overcurrent protector

PROTECT (1) is arranged to stop oscillation of the oscillator (IC5501) when the reference voltage is exceeded, by comparing the reference voltage (IC5501) with the high voltage potential-divided by HV-BLOCK and resistors (VR5501, R5531) by the comparator (IC5501).

PROTECT (2) is arranged to stop oscillation of the oscillator when the reference voltage is exceeded, by rectifying the tertiary coil voltage of the flyback transformer with diodes (D5517, D5519) and a capacitor (C5516), and by making comparison with the reference voltage in the same manner as for PROTECT (1). Overcurrent protector 1 is arranged to stop oscillation of the oscillator (IC5501) based on the result of judgment by the comparator (Q5512, Q5513), when the detected anode current is found to exceed the level set by ABL.

Lastly, overcurrent protector 2 is arranged to stop oscillation of the oscillator (IC5501) when an overcurrent flows from the choke coil, based on the result of judgment by the comparator (Q5502) that examines the voltage at the resistors (R5566, R5567) obtained through conversion of the current from the choke coil.

Once any protector operates, this information is transmitted to the SYSTEM board and shut down the set. At that time, the 7 segment LED indicates "FD" as an error code.

④ FAN driving circuit

FAN is connected to the connectors F1 ~ F9. Pin 1 of the connectors F1 ~ F9 is for the FAN source. This source is gained from Pin 3 of the HP connector at 15V through series resistors (R5509F, R5511F, R5513F, etc.). Since each fan has a different capacity of wind, the value of each resistance is changed according to the fan capacity. Each fan-stop is detected at Pin 2 of the connectors F1 ~ F9 and Pin 5 of the HP connector (FAN in the power unit). If a fan stops, Pin 3 of the HD connector is maintained at the "L" level. This information is transmitted to the SYSTEM board, and an indication of "WARNING" is displayed on the screen and the power supply of the set is tripped. At that time, the LED indicates "F0" as an error code.

SYSTEM PWB (PWC-4188)

1. Functions

- System control for the projector and its peripheral units (ISS-6020, controlling personal computer)
- Decoding of control switches in the rear part of the main body and remote control
- Fault detection and 7-seg display control
- Generation of on-screen display signal
- Generation of adjusting test signals
- Input terminal selection
- Input signal discrimination
- Control of VIDEO system circuit/DAUGHTER/OSC/WAVE PWB, D-CONV PWB
- Storage of various adjusting data

2. Hardware configuration

- CPU : μ PD70325-10 (V25+)
- SRAM : 32kBytes stack area
- PSRAM : 128kBytes work area
- EEPROM : 32kBytes program area
- Flash ROM : 640kBytes program area
- Parallel port: Projector's internal status detection and various controls
- Serial port : Communication with peripheral units

3. Description of switches and volume controls

① L8081, L8082, VR8081

No adjustments are required in the field, since all adjustments have been finished at the factory before shipment.

L8081 : VCO source oscillation adjusting coil for PLL

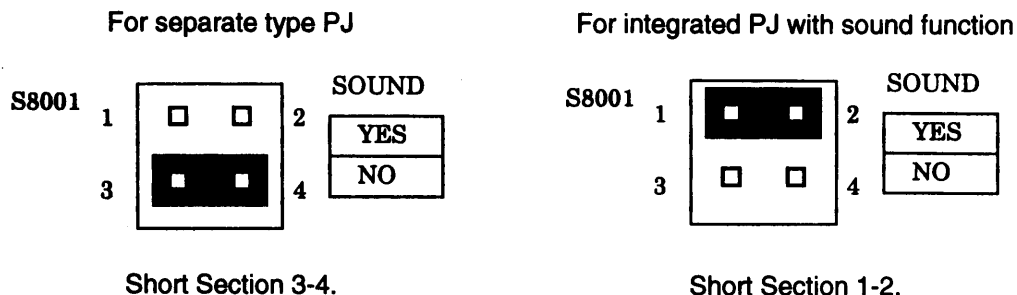
L8082 : VCO source oscillation adjusting coil for PLL

VR8081 : On-screen display position adjusting volume control

CIRCUIT DESCRIPTION

② S8001

This is a jumper switch used to enable software control of sound functions when this SYSTEM PWB is used for a model (screen integrated model) with the sound function.

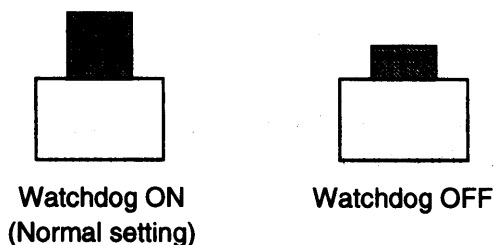


③ S8061, S8062

These are the switches to set up a condition of the reset circuit in the main CPU.

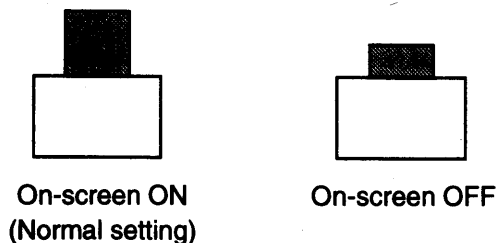
S8061 : This is a reset switch (non-lock switch) of the main CPU. While it is pushed, the CPU assumes the reset state.

S8062 : This is a watchdog timer ON/OFF switch (lock switch) of the main CPU. It is set at ON in normal usage. (The watchdog timer provides a reset function when the CPU should run away.)



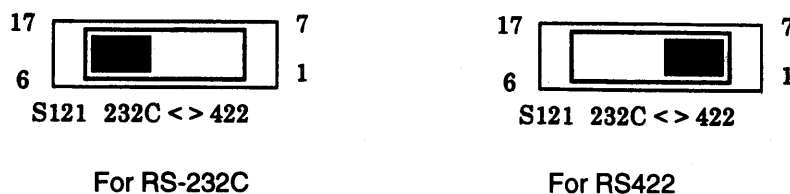
④ S8101

This is an on-screen display ON/OFF hard switch (lock switch), usually set at ON.



⑤ S8121

This is a communication system changeover switch for the OPTION terminal located in the rear part of the PJ main body. RS-232C and RS422 are available for the selection of two communication systems.



4. Circuit operation**① System control for the projector and its peripheral units (ISS-6020, controlling personal computer)**

When connected with its peripheral unit (ISS-6020) and external control equipment, this projector enables system structuring, employing a serial communication port.

1) Connection with ISS-6020

For connection with ISS-6020, Terminal REMOTE1 of the projector is used. The communication system is RS-422 and the communication speed is 9600bps fixed.

For data reception by communication with ISS-6020, a differential signal of RS-422 is sent from the REMOTE1 terminal via the S-MOTHER PWB and entered in IC8121 (driver/receiver of RS-422) on the SYSTEM PWB. Level conversion of the different signal/TTL signal is effected by IC8121. The signal converted to the TTL level is entered in the serial communication port of the main CPU (IC8001). Communication output of the projector is sent by the reverse routing through the same circuit systems.

2) Connection with external control equipment

Connection with external control equipment (personal computer, etc.) employs an OPTION terminal. The communication system for this terminal is RS-232C or RS-422, selective. Refer to the previous description (3-⑤) regarding the method of selection. The communication rate can be chosen between 4800bps and 38400bps according to the "setting of option terminal baud rate" for the projector.

- For RS-232C setting

For data reception from external equipment, a signal ($\pm 12V$) of RS-232C is sent from the OPTION terminal via the S-MOTHER PWB and entered in IC8122 (driver/receiver of RS-232C) on the SYSTEM PWB. This signal is converted by IC8122 to the level of $\pm 12V$ /TTL signal. The signal converted to the TTL level is entered in the serial interface circuit of IC8041 that is one of the external ports for the main CPU (IC8001). When receiving a data input, IC8041 makes a reception interrupt request to the main CPU. Upon reception of this request, the main CPU begins to get reception data through the data bus. Communication output of the projector is sent by the reverse routing through the same circuit systems.

- For RS-422 setting

For data reception from external equipment, a differential signal of RS-422 is sent from the OPTION terminal via the S-MOTHER PWB and entered in IC8121 (driver/receiver of RS-422) on the SYSTEM PWB. This signal is converted by IC8121 to the level of differential signal/TTL signal. The signal converted to the TTL level is entered in the serial interface circuit of IC8041 that is one of the external ports for the main CPU (IC8001). When receiving a data input, IC8041 makes a reception interrupt request to the main CPU. Upon reception of this request, the main CPU begins to get reception data through the data bus. Communication output of the projector is sent by the reverse routing through the same circuit systems.

② Decoding for remote control, control switches in the rear part of the main body, and parallel external control
Decoding for remote control, control switches in the rear part of the main body, and parallel external control is effected by IC8063 (SUB-CPU). Data are sent to the main CPU after conversion to internal commands.**1) Remote control**

Signals of wireless and wired remote controls are gathered together at the S-MOTHER PWB. Since then, data are entered in Pin 1 of SUB-CPU of IC8063, via IC8062 (comparator) of the SYSTEM PWB.

At the SUB-CPU, the received serial remote-control data are converted into 8-bit parallel internal commands that are then transferred to the main CPU via IC8023 that is an external port of the main CPU.

The main CPU decodes the received commands and executes the respective functions.

2) Control switches in the rear part of the main body

The control switches in the rear part of the main body is used to turn on and off the matrix consisting of I/O ports for the SUB-CPU of IC8063. The SUB-CPU identifies the pressed switch through the connector "SC" on the SYSTEM PWB, and sends out the converted internal command to the main CPU through IC8023 that is an external port of the main CPU. The main CPU decodes the received command and executes the respective functions.

CIRCUIT DESCRIPTION

3) Parallel external control

The 7-seg signal of parallel external control from the REMOTE1 terminal is entered in the SUB-CPU via the S-MOTHER PWB, and converted into an internal command. Since then, the command is sent to the main CPU through IC8023 that is an external port of the main CPU. The main CPU decodes the received command and executes the respective functions.

③ Fault detection and 7-seg display control

Conditions of the parallel input port (PTO-7) incorporated in the main CPU and several external input ports are searched by the main CPU of IC8001. If any abnormality is found, an error code corresponding to the contents of the error is given at the 7-segment display.

The 7-seg display data are set in the external port IC8042 of the main CPU, and then entered in the 7-seg LED through IC8043, IC8044, and the connector "SC."

The lower digit and the higher digit of the 7-seg LED are driven by IC8043 and IC8044, respectively.

④ Generation of on-screen display signal and adjusting test signal

Regarding the on-screen display signal and adjusting test signal, screen-display image data are written by the main CPU in the field memory consisting of IC8101 and IC8102 (VRAM). These data are read out in synchronization with the vertical and horizontal sync signals.

Since the data read from IC8101 and IC8102 (VRAM) are parallel, they are converted into serial signals by IC8103, and sent to the GAIN-CTL PWB and VIDEO OUT PWB via the output circuit.

⑤ Selection of input terminals

Input terminals are selected based on the H/L combination of Pin 20 and Pin 21 at IC8025 that is an external port of the main CPU. These signals are sent for input terminal changeover to the DAUGHTER PWB through the S-MOTHER PWB.

⑥ Input signal discrimination

Signal mode, horizontal frequency, No. of lines, sync polarity, input terminal, and other conditions are detected and identified for the input signal. At the time of signal registration, these conditions are internally acquired and stored together with the adjustment data for each registration signal. The registration data closest to the input signal are retrieved and output.

⑦ Control of VIDEO system circuit/DAUGHTER/OSC/WAVE/D-CONV PWB

The external-port IC8024 of the main CPU and the decoder circuit of IC8026 are used to determine which board of DAUGHTER/ OSC/ WAVE should be controlled. By the use of Pin 8 and Pin 9 of IC8024, serial data are sent to each board to control each gain.

For the D-CONV PWB, address/data buses of the main CPU are connected through the buffer of IC8181, IC8182, IC8183, IC8184, and IC8185. Using these buses, command exchange is controlled.

⑧ Storage of various adjusting data

Various adjusting data, except for those of alignment point and convergence point, are stored in IC8006 EEPROM. Backup protection of these data in the memory can be assured by a personal computer.

5. EEPROM initialize

IC8006 EEPROM stores various adjusting data, and also necessary information data needed to actuate the main CPU.

To control the data in the EEPROM, these data are attached with version numbers. Each time the AC source is turned on, inspection is carried out to examine if the data are available for normal operation of the main CPU. If the data in the EEPROM are found not to guarantee normal operation of the CPU, then it is necessary to initialize the memory.

When initialize is needed, "EF" flashes at the 7-seg LED after the AC source has been turned on. To execute initialize, press the "SELECT" button for 7 to 10 seconds at the control panel that is located in the rear part of the projector, while "EF" is kept flashing. During initialize, the 7-seg display turns to be continuous lighting of "EE" and it turns to be "00" upon completion of initialize.

(The initialize function is not started while "EF" keeps flashing.)