TOSHIBA

FILE NO. 336-9602

TECHNCAL TRAINING MANUAL

DATA & GRAPHICS PROJECTOR

P7300U

Return to Index

PRINTED IN JAPAN, May, 1996 S

CONTENTS

SECTION I
OPTICAL SYSTEM 1-1
1. NECK COMPONENTS 1-2
2. FUNCTIONS OF MAJOR COMPONENTS 1-2

SECTION II
POWER SUPPLY CIRCUIT 2-1
1. OUTLINE 2-2
2. P-RECT/HV PC BOARD 2-2
3. POWER-1 PC BOARD 2-6
4. POWER-2 PC BOARD 2-6
5. PROTECTION CIRCUIT 2-7
6. TROUBLESHOOTING 2-8

SECTION III
MICROPROCESSOR (CONTROL) 3-1
1. OUTLINE OF SYSTEM 3-2
2. SYSTEM MICROPROCESSOR BLOCK 3-4
3. MICROPROCESSOR RESETTING BLOCK 3-6
4. REMOTE CONTROL RECEPTION BLOCK 3-7
5. RS-232C TRANSMITTER/ RECEIVER BLOCK 3-8
6. CONTROL MODE READING BLOCK 3-9
7. NON-VOLATILE MEMORY BLOCK 3-10
8. ON-SCREEN DISPLAY BLOCK 3-10
9. CONVERGENCE/DEFLECTION SYSTEM CONTROL BLOCK 3-11
10. VIDEO SYSTEM CONTROL BLOCK 3-12
11. VARIOUS CONTROL MODES 3-12
12. RS-232C/RS-422 CONTROL METHOD 3-14
13. TABLE OF CONTROL ITEM BY EACH CONTROL MODE 3-15

SECTION IV
CONTROL CIRCUIT 4-1
1. OUTLINE 4-2
2. INTERNAL SYNC SIGNAL GENERATION CIRCUIT 4-2
3. TEST PATTERN GENERATION CIRCUIT 4-2
4. VARIOUS DATA 4-8

SECTION V
VIDEO CIRCUIT 5-1
1. OUTLINE 5-2
2. FLOW OF SIGNAL 5-2
3. INPUT SWITCHING CIRCUIT 5-3
4. DIGITAL COMB FILTER 5-3
5. PAL/SECAM PROCESSING CIRCUIT 5-6
6. UP-CONVERTER CIRCUIT 5-14
7. NTSC/HDTV PROCESSING CIRCUIT 5-19
8. CONTROL SYSTEM 5-24

SECTION VI
RGB CIRCUIT 6-1
1. OUTLINE 6-2
2. INPUT SIGNAL SWITCHING CIRCUIT 6-2
3. VIDEO SIGNAL AMPLIFIER CIRCUIT 6-2
4. VIDEO BLANKING CIRCUIT 6-3
5. ON-SCREEN SIGNAL/TEST SIGNAL PROCESS CIRCUIT 6-3
6. BRIGHTNESS CONTROL CIRCUIT 6-3
7. CONTROL CIRCUIT 6-4
8. SYNC SIGNAL PROCESS CIRCUIT 6-6
9. TRIMMING CIRCUIT 6-8

SECTION VII
CRT-D CIRCUIT 7-1
1. OUTLINE 7-2

SECTION VIII
DEF CIRCUIT 8-1
1. OUTLINE 8-2
2. VERTICAL F/V CONVERSION CIRCUIT 8-2
3. VERTICAL PHASE CIRCUIT 8-3
4. VERTICAL OSCILLATION CIRCUIT 8-5
5. VERTICAL SAW-TOOTH WAVE-FORM GENERATION CIRCUIT 8-6
6. VERTICAL REFERENCE WAVE-FORM GENERATION CIRCUIT 8-7
7. VERTICAL OUTPUT CIRCUIT 8-9
8. VERTICAL DEFLECTION STOP PROTECTION CIRCUIT 8-10
9. VERTICAL BLANKING CIRCUIT 8-11
10. OUTLINE OF HORIZONTAL CIRCUIT 8-11
11. HORIZONTAL OSCILLATION SYNC CIRCUIT 8-12
12. CONSTANT SWITCHING OF LOW FREQUENCY BAND AND HIGH FREQUENCY BAND 8-12
13. H. STOP CIRCUIT 8-13
14. CONTROL VOLTAGE OF HORIZONTAL OSCILLATION FREQUENCY 8-13
15. HORIZONTAL DRIVE PULSE DUTY CONTROL VOLTAGE 8-13
16. HORIZONTAL PHASE ADJUSTMENT CIRCUIT 8-15
17. HORIZONTAL F/V CONVERSION CIRCUIT 8-15

SECTION IX
HORIZONTAL FOCUS OUTPUT CIRCUIT 9-1
1. OUTLINE 9-2
2. DESCRIPTION OF OPERATION 9-2

SECTION X
CONVERGENCE CIRCUIT (CONV/FOCUS PC BOARD) 10-1
1. OUTLINE 10-2
2. DESCRIPTION OF CIRCUIT OPERATION 10-2

SECTION XI
CONVERGENCE OUTPUT CIRCUIT (FOCUS/ CONV-OUT PC BOARD) 11-1
1. OUTLINE 11-2
2. DESCRIPTION OF OPERATION 11-2

SECTION XII
HIGH VOLTAGE CIRCUIT 12-1
1. HIGH VOLTAGE OSCILLATION CIRCUIT 12-2
2. OUTPUT CIRCUIT 12-2
3. HIGH VOLTAGE CONTROL CIRCUIT 12-2
4. X-RAY PROTECTION CIRCUIT 12-2
5. HV STOP CIRCUIT 12-3
6. SCREEN VOLTAGE GENERATION CIRCUIT 12-3
7. ABL VOLTAGE GENERATION CIRCUIT 12-3
8. HIGH VOLTAGE LIMITATION CIRCUIT 12-4

SECTION XIII
H-OUT CIRCUIT 13-1
1. HORIZONTAL SIZE CIRCUIT 13-2
2. KEYSTONE AND PINCUSHION DISTORTION CORRECTION CIRCUIT 13-3
3. H. STOP CIRCUIT 13-3
4. DRIVE CIRCUIT 13-4
5. CENTERING ADJUSTMENT CIRCUIT 13-4
6. LINEARITY ADJUSTMENT CIRCUIT 13-4
7. R, G AND B AMPLITUDE VARIATION ADJUSTMENT 13-4
8. BLANKING PULSE GENERATION CIRCUIT 13-5
9. PROTECTION CIRCUIT 13-5

SECTION I
OPTICAL SYSTEM

1. NECK COMPONENTS

1-1. Parts Components Around the Neck of Projection Cathode Ray Tube

Fig. 1-1 shows the parts components around the neck of projection cathode ray tube.

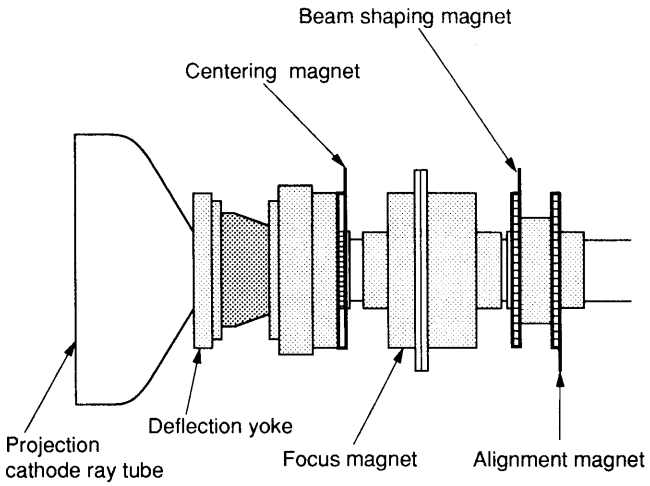


Fig. 1-1 Parts components around the neck of projection cathode ray tube

1-2. Description of Operation

As the components around the neck, there are provided the deflection yoke (which consisted of the main yoke, sub-yoke and centering magnet), focus magnet, beam shaping magnet and alignment magnet (the beam shaping magnet and the alignment magnet are united).

The main yoke of deflection yoke is composed of horizontal and vertical deflection coils, and bends the light beam to the horizontal and vertical directions. The sub-yoke is also called a convergence yoke, which is composed of horizontal and vertical coils, and functions to adjust the distortion by the adjustment current supplied from the convergence output circuit and to overlap the red, green and blue colors on the screen. The centering magnet is composed of bipolar magnet, located at the rear of deflection yoke and is for adjusting the picture position.

The focus magnet is composed of the permanent magnet and the coil, and makes the center and periphery of screen to be the uniform focus image by flowing to the coil the current of parabolic waveshape supplied from the focus circuit.

The beam shaping magnet and the alignment magnet are composed of tetra polar and bipolar magnets respectively, and are used for enhancing the focus quality similarly to the focus magnet.

2. FUNCTIONS OF MAJOR COMPONENTS

2-1. Outline

The optical system of P7300U is composed of the projection cathode ray tube and the lens as shown in Fig. 1-2. The screen is an optional parts. This unit can not only applied to the front projection system screen but also to the rear projection system screen.

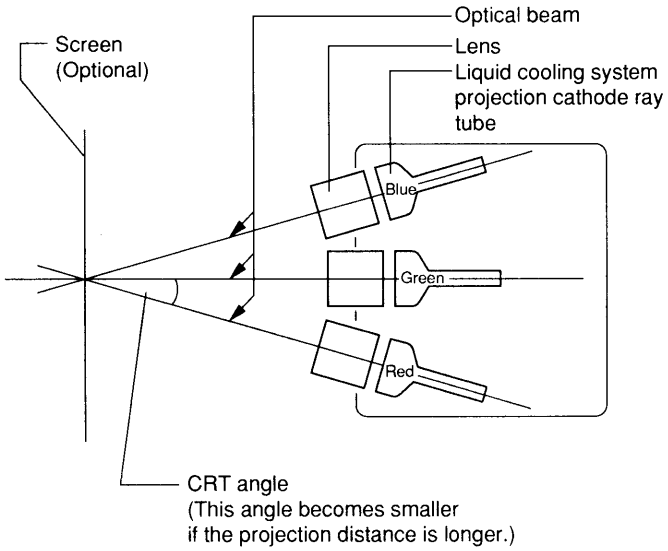


Fig. 1-2 Optical system components of P7300U

2-2. Air Coupling and Liquid Cooling System Projection Cathode Ray Tube

The projection cathode ray tube of this unit applies the liquid cooling system projection cathode ray tube which has the cooling function to the projection cathode ray tube itself as shown in Fig. 1-3. Apart from the projection cathode ray tube for optical coupling where the cooling liquid is sealed between the projection cathode ray tube and lens, this has no fear of cooling liquid leakage when replacing the projection cathode ray tube. In addition, the CRT angle and the lens angle meeting the projection distance and screen incidence angle can be set without replacing the lens holder as conventionally needed.

The CRT angle is the light beam angles of red and blue against that of green, and this angle needs to be made smaller as longer becomes the projection distance. The CRT angle of this unit employs 3-stage adjustable mechanism system and can be applied to this unit with its screen size from 70 to 300 inches.

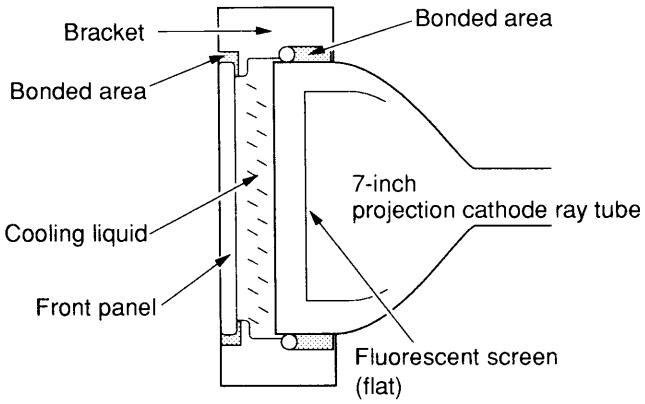


Fig. 1-3 Air coupling and liquid cooling system projection cathode ray tube

When the light beam does not enter on the screen vertically as shown in Fig. 1-4, the difference in the distance from the lens (projection cathode ray tube) in the screen vertical (horizontal) direction is brought forth. This cuases the imbalance of the focus quality in vertical (or horizontal) direction of the screen.

To correct the imbalance, the lens angle is provided between the lens axis and the projection cathode ray tube.

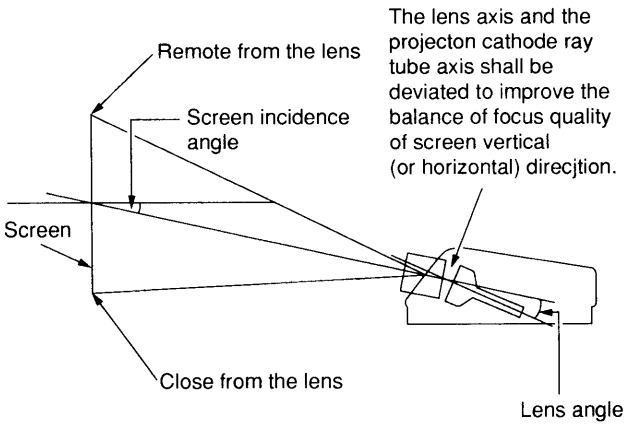


Fig. 1-4 Lens angle

The setting of CRT angle and lens angle can be adjusted by the mechanism shown in Fig. 1-5 according to the unit installation conditions. For the detailed adjustment method, refer to the installation manual.

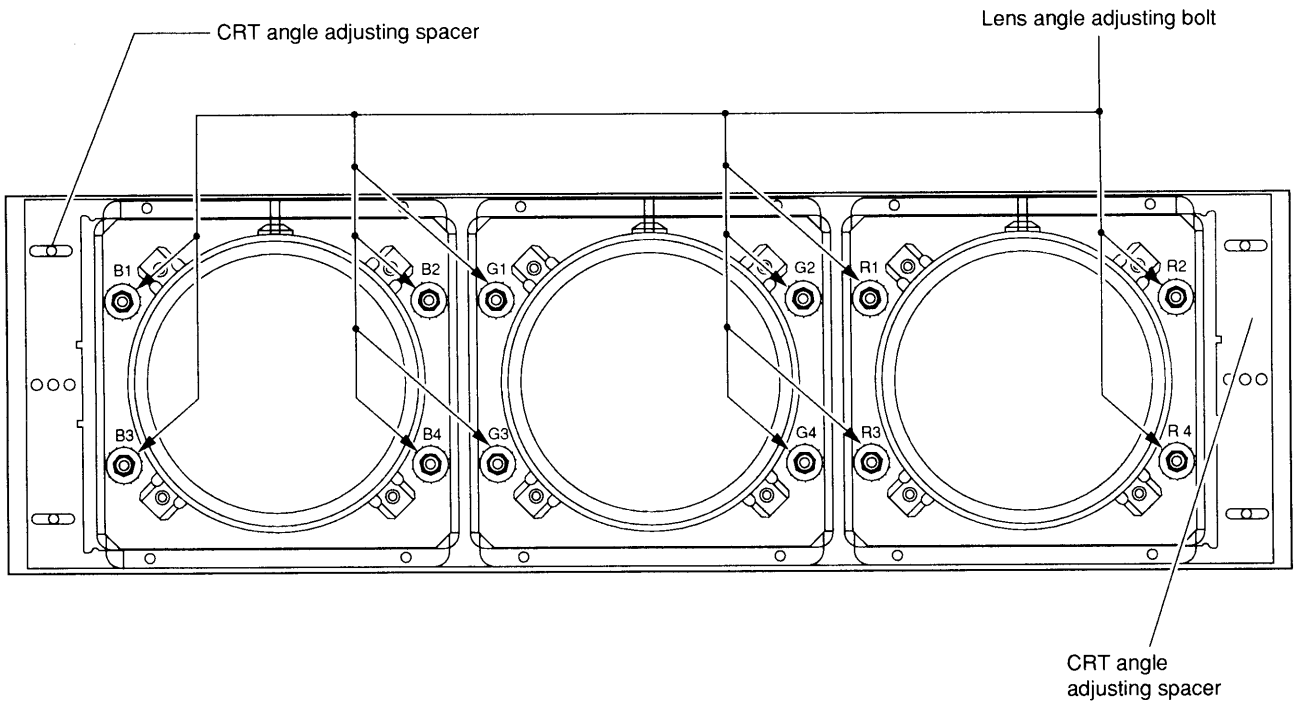


Fig. 1-5 Adjustment mechanism of CRT angle and lens angle

2-3. Lens

The lens forms the image on the face plate of projection cathode ray tube on the screen. The lens used in this set are provided with the adjusting nut (projection cathode ray tube side) to improve the focus quality at the screen center (entirety) and that to only improve the focus quality at the peripheral portion of the screen as shown in Fig. 1-6. First, the focus at the screen center is adjusted and then the focus at the periphery of screen is adjusted.

Moreover, the lenses for green and red are provided with the color filters for respective colors and function to enhance the purity of respective colors.

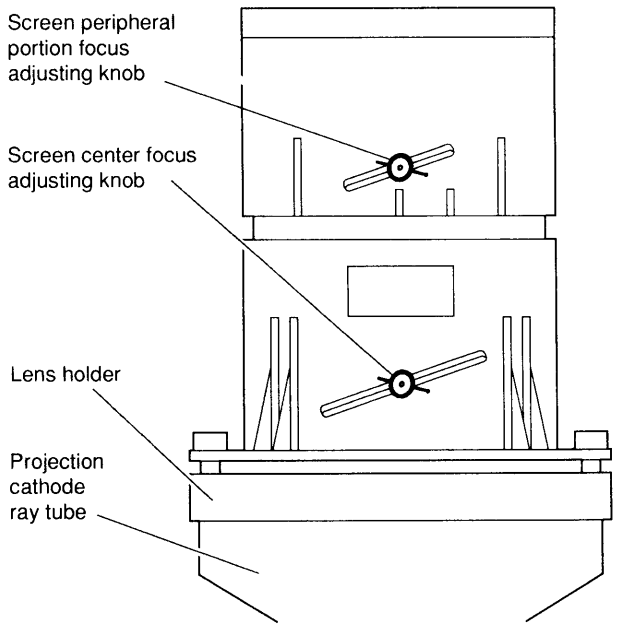


Fig. 1-6 Lens

SECTION II
POWER SUPPLY CIRCUIT

1. OUTLINE

The block diagram of power supply circuit of this set is shown in Fig. 2-2.

The power supply circuit is composed of 3 PC boards of P-RECT/HV, POWER-1 and POWER-2.

The P-RECT/HV PC board is mainly composed of the stand-by power supply, AC rectifier circuit, the power supply for high voltage circuit, the protection circuit to stop the set in an emergency case and a part of high voltage circuit.

POWER-1 is mainly composed of 2 DC/DC converters.

POWER-2 is mainly composed of 3 DC/DC converters.

2. P-RECT/HV PC BOARD

With the main power supply turned on, the AC power supply is supplied to the AC/DC converter (Z899) outputting the stand-by 5V. The converter inputs the commercially available power supply to obtain the insulated 5V, and is of module type. The output is supplied to the microprocessor controlling the system control of the set, and also supplied to the interface circuit for inputting and outputting the remote control input circuit and external control signal. The output is supplied to the CONTROL PC board (microprocessor, etc.), HD/VIDEO PC board (interface circuit, wired remote control input circuit) and RGB PC board (remote control light receptacle).

When the power supply of the set is turned ON using the remote control or external control terminal, the ON/OFF output terminal of microprocessor develops Hi. The terminal signal is supplied to pin 2 of P851 of this PC board via the resistor, and Q853 is turned on.

With Q853 turned on, the current flows into the control circuit of SSR (solid state relay, S802) with the standby 5V as its power supply, connects the AC side circuit and supplies the power supply to the rectifier circuit in the next stage. The AC rectifier circuit performs the double voltage rectification. The operation is explained hereunder.

When the positive half cycle is input with A-point as its reference, the current not only flows to the AC line via D1 and C1 but also charges the C1 and develops the voltage of the peak value. The peak value is the root twice of input voltage (effective value).

Further, the negative half cycle current not only flows into the AC line via C2 and D2 but also charges C2. The voltage becomes the value of peak value with the B-point being negative if viewed with A-point as a reference.

Because the output voltage between B-point and E-point equals to the total of voltages charged to C1 and C2, it becomes twice the input voltage and moreover the root twice.

The rectifier circuit is composed of 4 circuits of D801 to D804. The rectification output of D803 is supplied to POWER-1, the rectification outputs of D801 and D802 are supplied to POWER-2 and become the input of DC/DC converter in the next stage. The rectification output of D804 is supplied to the DC/DC converter (composed of Q850, etc.) supplying the power of high voltage circuit inside this PC board.

The operation principle of DC/DC converter is explained hereunder. (The projector uses 6 DC/DC converters except for the standby power supply. The operation principle is quite the same).

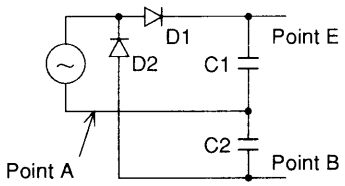


Fig. 2-1

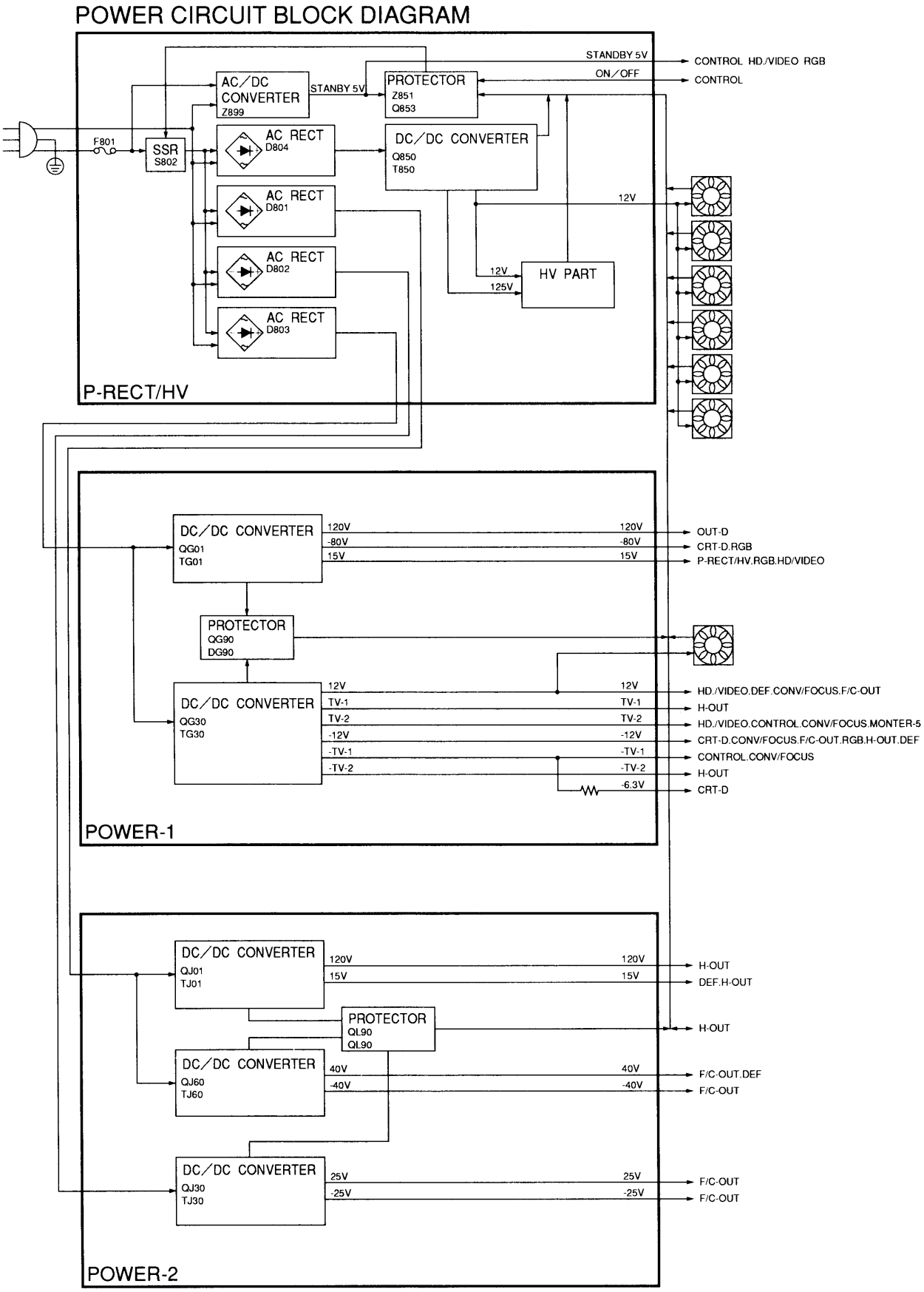


Fig. 2-2 Power supply block diagram

The converter system is the switching power supply of the fly-back system, and the element used is STR-S6709. This IC has the following functions.

Table 2-1

Pin No.	Function
1	Collector of switching transistor.
2	Emitter of the switching transistor and ground for HIC.
3	Base of switching transistor.
4	Pulling the base accumulated charge when turning off the switching transistor.
5	Supplying the base current to turn on the switching transistor.
6	Input to detect the over-current of switching transistor.
7	Feedback terminal to keep the output voltage to be constant.
8	Input to stop the switching.
9	Power supply for HIC.

2-1. Start-up Operation

When the input (primary rectification voltage) is applied to the converter, the capacitor C854 is charged via the starting resistances R862 and R866. The voltage at both ends of capacitor gradually goes up as the charging time passes, and the voltage of pin 9 of hybrid IC Q850 connected to C854 goes up in the same way. Pin 9 of Q854 is used as the power supply pin, and when the voltage of pin 9 becomes higher than approx. 8V, Q850 starts its operation (the voltage stopping the operation after the start-up is lower than approx. 4.9V). When Q850 starts its operation, the switching transistor inside the HIC is turned on, and the power is supplied and stored in the converter transistor T850. When the switching transistor is turned off, the stored power is rectified by the diode of D856, and supplied to pin 9 of Q850 as the power supply for HIC via the series regulator Q851.

Then, the switching transistor is switched on and off again. When the secondary output voltage and the power supply voltage for HIC gradually go up and reach the specified value during this process, they are stabilized by the operation of feedback circuit.

Pin 9 of HIC also has the input function of over-voltage protection, and when the voltage of pin 9 has exceeded 10V, the operation is stopped and the stop state is latched with the current from the start-up resistance. This can be released by shutting off the input (or turning off the set) of converter.

The over-voltage protection using pin 9 of the converter operates when the power supply output voltage (cathode voltage of D856) for HIC becomes higher than approx. 35V.

The voltage is the total of the continuity voltages of D869 and D870 and the over-voltage operating point 10V of pin 9. If the over-voltage protection function of pin 9 is operated during a trouble, any of D869 and D870 gets shorted, so this should be kept in mind when performing the repair work.

2-2. Usual Operation

When the switching transistor is turned on after the completion of start-up operation, the current flows into the primary winding of converter transistor T850, and the power is stored to the converter transformer as the magnetic flux. (At that time, the diodes D860, D861 and D856 become inverted bias and are cut off). When the switching transistor is turned off, each output winding becomes the voltage in the direction with the positive bias applied to the diode, and hence D860, D861 and D856 are turned on, rectified, charge the smoothing capacitor, obtain the constant voltage and further supply the power to the load. The output voltage on the secondary side is stabilized by controlling the ON time of the switching transistor. The converter detects 125V of secondary output line and feeds it back to Q850 of primary HIC.

When the pin 7 of HIC, Q850 is the input pin for feedback and the primary supply power increases, the current input to pin 7 is lessened and the ON time of switching transistor is elongated by the control circuit inside the HIC and thus a constant voltage can be supplied.

2-3. Error Amplifier and Protection Circuit (on the HIC1016 Z851)

The HIC1016 is used as the error amplifier, the protection circuit, and the output element of the entire set protection circuit.

The feedback voltage is input to pin 1 of Z851, compared with the internal reference voltage and output to pin 3. The output of pin 3 is input to the current amplifier Q852, and connected to the primary circuit via the photo coupler Q856.

The over-voltage protection of 125V line similarly divides the voltage input to pin 1 of Q851 with the resistor inside Z851, triggers the internal SCR (thyristor) when the voltage exceeded the threshold level, and turns on the internal transistor (the emitter is at the ground potential) outputting with the open collector from pin 16. Because the standby 5V is supplied to the SCR, the transistor of open collector continues to be open until the main power supply of set is switched off, and the output of pin 16 becomes the ground potential. Further, the over-voltage protection of 125V operates at the level higher than approx. 141V.

The over-current protection of 125V line inputs the both end voltage of resistor R863 to pin 1 and pin 2 of Z851, and when the voltage is higher than approx. 0.7V, the protection triggers the above mentioned SCR, and makes the pin 16 of Z851 to be the ground potential similarly to the above mentioned case. The gate pin of above mentioned SCR is connected to pin 14 of Z851, and the protection function works and turns off the set by applying the voltage to the pin during another abnormal mode. The over-voltage protection of 12V line of DC/DC converter consisting of Q850 connects to pin 14 of Q851 via the Zener diode of D864 or the diode D865 for OR circuit and the protection function works when the 12V line voltage becomes higher than approx. 22V. The mode, etc. where the protection function works will be explained separately. When the protection circuit works and the potential of pin 16 of Z851 becomes the ground, Q853 is turned off and the SSR is turned off. As described before, the main power supply switch of set needs to be turned off for releasing this.

2-4. Fan Stop Protection Circuit

This set uses many cooling fans. For preventing the heating when any of the fans should stop, the stop of fan actuates the protection circuit and switches off the set. A rotation stop sensor is built-in inside the used fan, and the impedance of sensor output terminal becomes greater when the fan stops. (The sensor output terminal of fan outputs with the open collector (the emitter is at the ground potential), its transistor is turned on during the rotation and turned off during the stop). This set uses many fans, but the operation is identical in all the fans, so the operation is to be explained with reference to the fan connected to P850. Pin 1 of P850 is the power supply for fan, and supplies 12V.

The stop sensor of fan is input to pin 3 of P850, and connects to the R890 as the load resistance of open collector transistor inside the fan. Since the transistor inside the fan is turned on during the usual rotation, pin 3 of P850 becomes almost the ground potential. Because the transistor is turned off during the stop, the potential of pin 3 goes up to approx. 8V which is the potential where the power supply voltage 12V is divided with the R890, R885 and R891, and the base of transistor Q854 becomes almost 4V via the diode D868.

Further, the signal is supplied to pin 14 of HIC Z851 for protection via the emitter follower of Q854 and switches off the set. When any of many fan stop signals should be stopped in the OR circuit of D868, the set is securely turned off.

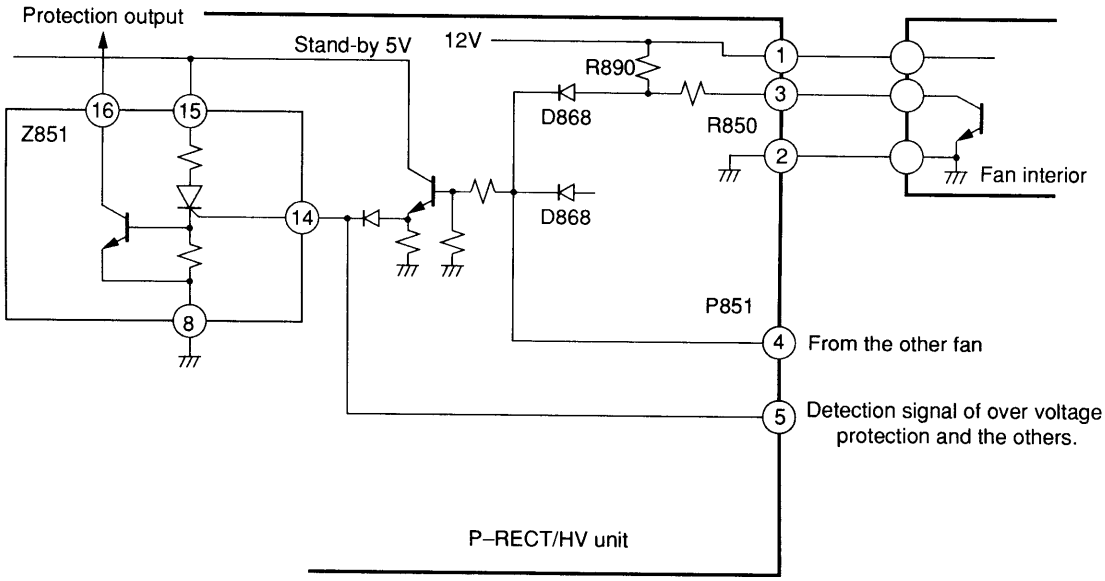


Fig. 2-3

3. POWER-1 PC BOARD

The POWER-1 PC board uses as its input the AC rectification output from the above mentioned P-RECT/HV PC board, forms the necessary secondary voltage with two DC/DC converters and supplies it to the load.

The DC/DC converter composed of QG01, etc. supplies the power supply to the video circuit. The output voltages are 3 kinds of 120V, –80V, and 15V.

The DC/DC converter composed of QG30, etc. forms the ±12V and ±7V and supplies them to each circuit. The ± 7V uses 2 systems each of rectification circuit because the supplied current is much, and is supplied to the load as 7V–1 and 7V–2 and –7V–1 and –7V–2.

The over-voltage protection circuit is in the positive output line, and works when the threshold voltages of Zener diodes are exceeded respectively.

During the over-voltage, the voltage is applied to the SCR and the gate of DG90 via DG20, DG18, DG49, DG50 and DG51 for OR circuit from the Zener diode. When the SCR is turned on, the luminous diode DG91 illuminates, and moreover the transistor QG90 is turned on and the collector develops approximately 5V of the power supply voltage. The collector of QG90 is connected to pin 14 terminal of HIC1016 via the diode DG92 for OR circuit and the connector P851 pin 5 of P-PECT/HV PC board. Therefore, the set is turned off when QG 90 is turned on. Further, since the power supply of SCR uses the standby 5V, the luminous diode is lighted up until the main power supply of set is switched off.

4. POWER-2 PC BOARD

The POWER-2 PC board forms the necessary secondary voltage with 3 DC/DC converters and supplies it to the load with the AC rectifying output from the above mentioned P-RECT/HV PC board as its input.

The DC/DC converter composed of QJ01, etc. supplies the power mainly to the horizontal deflection circuit. The voltages output are 2 kinds of 120V and 15V.

The DC/DC converter composed of QJ60, etc. supplies the power to the output circuit of horizontal dynamic focus. The voltages output are 2 kinds of ±40V.

The DC/DC converter composed of QJ30, etc. supplies the power to the convergence output circuit. The voltages output are 2 kinds of ±25V.

The over-voltage protective circuit is in the positive output line, and designed to work when the threshold voltages of Zener diodes are exceeded respectively. The operation is similar to the above mentioned POWER-1.

5. PROTECTION CIRCUIT

This circuit has a function to switch off the set during an abnormality. The mode for its function operated is shown in table 2-2.

There are abnormality detecting circuits of mentioned items 1 through 15 in table 2-2. Since any of the detection circuit operations switches off the SSR (Solid State Relay (S802 inside the P-RECT/HV PC board)) of set, the set stops its operation. Its state is maintained while the standby 5V is supplied. For releasing it, the AC input power supply must be switched off to stop the supply of standby 5V.

Table 2-2

No.	Detection mode	PC board	Detection line	Operation confirmation point	Remarks
1	Over voltage	P-RECT/HV	125V	125V line voltage	Operating at the voltage higher than 134V.
2	Over voltage	P-RECT/HV	12V	12V line voltage	Operating at the voltage higher than 22V.
3	Over current	P-RECT/HV	125V	Both ends voltage of R863	Operating at the serial current higher than 1.3A.
4	Over voltage	POWER 1	120V	120V line voltage	Operating at the voltage higher than 140V.
5	Over voltage	POWER 1	15V	15V line voltage	Operating at the voltage higher than 22V.
6	Over voltage	POWER 1	12V	12V line voltage	Operating at the voltage higher than 18V.
7	Over voltage	POWER 1	7V	Voltage of LG46	Operating at the voltage higher than 10V.
8	Over voltage	POWER 1	7V	Voltage of LG45	Operating at the voltage higher than 20V.
9	Over voltage	POWER 2	120V	120V line voltage	Operating at the voltage higher than 140V.
10	Over voltage	POWER 2	15V	15V line voltage	Operating at the voltage higher than 22V.
11	Over voltage	POWER 2	40V	40V line voltage	Operating at the voltage higher than 51V.
12	Over voltage	POWER 2	25V	25V line voltage	Operating at the voltage higher than 30V.
13	Fan stops	All fans	Rotation stops	Presence or absence of rotation	Rotation stop sensor is built-in for all fans
14	X-ray protection	P-RECT/HV	High voltage control voltage	DB18 cathode	Operating at the voltage higher than 20V.
15	Horizontal sweep stop	H-OUT	Presence or absence of fly-back pulse	DA13 cathode	Operating at the voltage higher than 7V.

For checking which abnormality detecting circuit is operating and the set stops, investigate the voltage in the operation confirmation point in the above table based on the value given in the remarks column. If the over-voltage protective circuit of power supply line inside the POWER-1 should operate, DG91 (LED) inside the POWER-1 comes on. This LED continues to get lighted until the main power supply of set is switched off. Similarly, if the over-voltage protective circuit of power supply line inside the POWER-2 should operate, DJ91 (LED) inside the POWER-2 comes on.

6. TROUBLESHOOTING

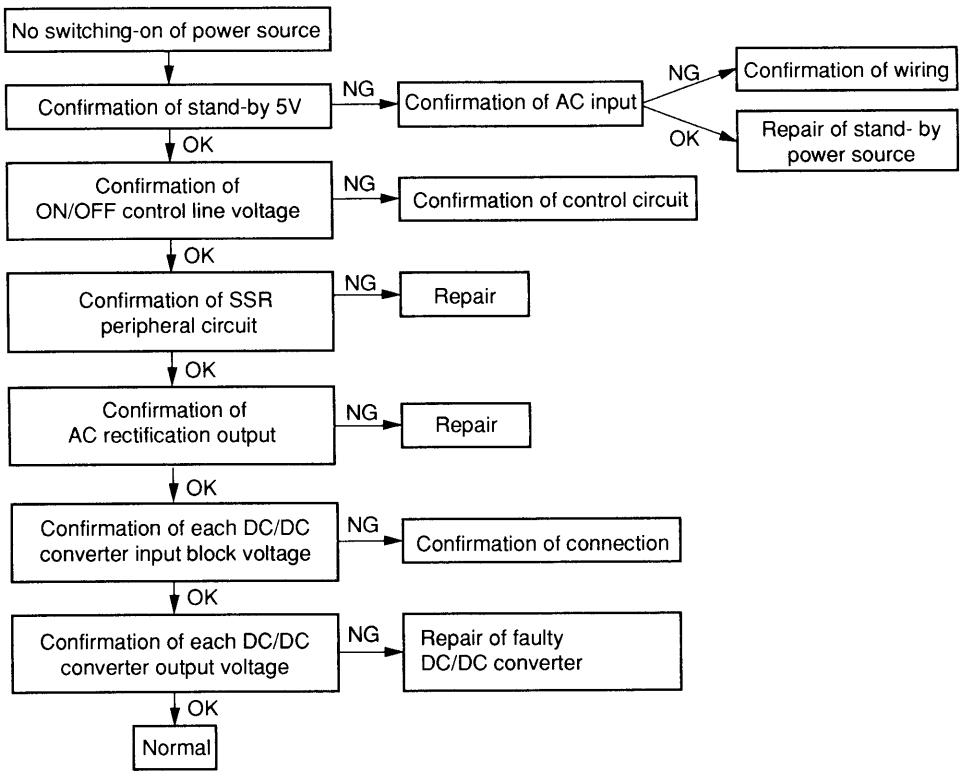
6-1. Precautions during the Repair

Because this paragraph includes the contents concerning the PL, you are requested to surely perform the work.

(1) When replacing the fuse (F801 inside the P-RECT/HV unit) of AC input block, be sure to solder the lead wire of fuse to the wiring board. (If the wire is not soldered, the fuse may radiate heat with the contact resistance of the holder and be broken.).

(2) When mounting the P-RECT/HV unit block (the assembled block with the unit, fan, power supply switch, AC inlet and metal parts) to the main body, surely tighten the fixing screws (3 screws of 4 mm) with the chassis. (The chassis is grounded with the connection of these screws. Improper connection may cause the danger for electric shock).

(3) The position of internal wiring and the protection parts (tube, binding band, tape, etc.) for wire materials must be returned to the previous state without fail. (The danger for electric shock due to the contact to heating parts, the contact between charged block and non-charged block and the damage to the cover may occur).



When the protection circuit operates and the set is turned off after supplying the power, check to see in which mode the protection circuit operates referring to the protection circuit section of the service data. After that, perform the followings depending on the cause for the protection circuit to operate.

(1) Protection operation due to the over-voltage
Check the applicable DC/DC converter.

(2) Protection operation due to the over-current
Check the high voltage circuit (loaded circuit).

(3) Protection operation due to the fan stop
Check the fan and its periphery circuit.

(4) Protection operation due to the X-ray protection
Check the high voltage circuit.

(5) Protection operation due to the horizontal sweep stop
Check the horizontal deflection circuit.

When the switching transistor built-in inside the HIC (STR-S6709) which is used for the DC/DC converter is short-circuited and defective, the following cases may be considered that the fuse in DC/DC converter input block may break and/or the Zener diode connected to the ground from pin 2 of HIC may be short-circuited. When the Zener diode is short-circuited, the protection circuit limiting the collector current of the switching transistor doesn't operate. In case of the trouble phenomenon as described above, check the Zener diode.

When the fuse FJ07 of 40V line of DC/DC convertor consisting of QJ40 of POWER-2, etc. breaks, the Zener diodes DJ81 and DJ82 may be short-circuited. Further, when the 25V line fuse FJ04 of DC/DC converter consisting of QJ30, etc. breaks, the Zener diodes DJ51 and DJ80 may be short-circuited. When the Zener diodes are short-circuited, the over-voltage protection of pin 9 of switching HIC operates and stops the switching function.

SECTION III
MICROPROCESSOR (CONTROL)

1. OUTLINE OF SYSTEM

The system microprocessor of P7300U is developed as the program with consciousness paid to the easiness of maintenance such as the use of external program ROM, inscription of construction, realization of modular parts, realization of multi files and control by mode.

Fig. 3-1 shows the system block diagram.

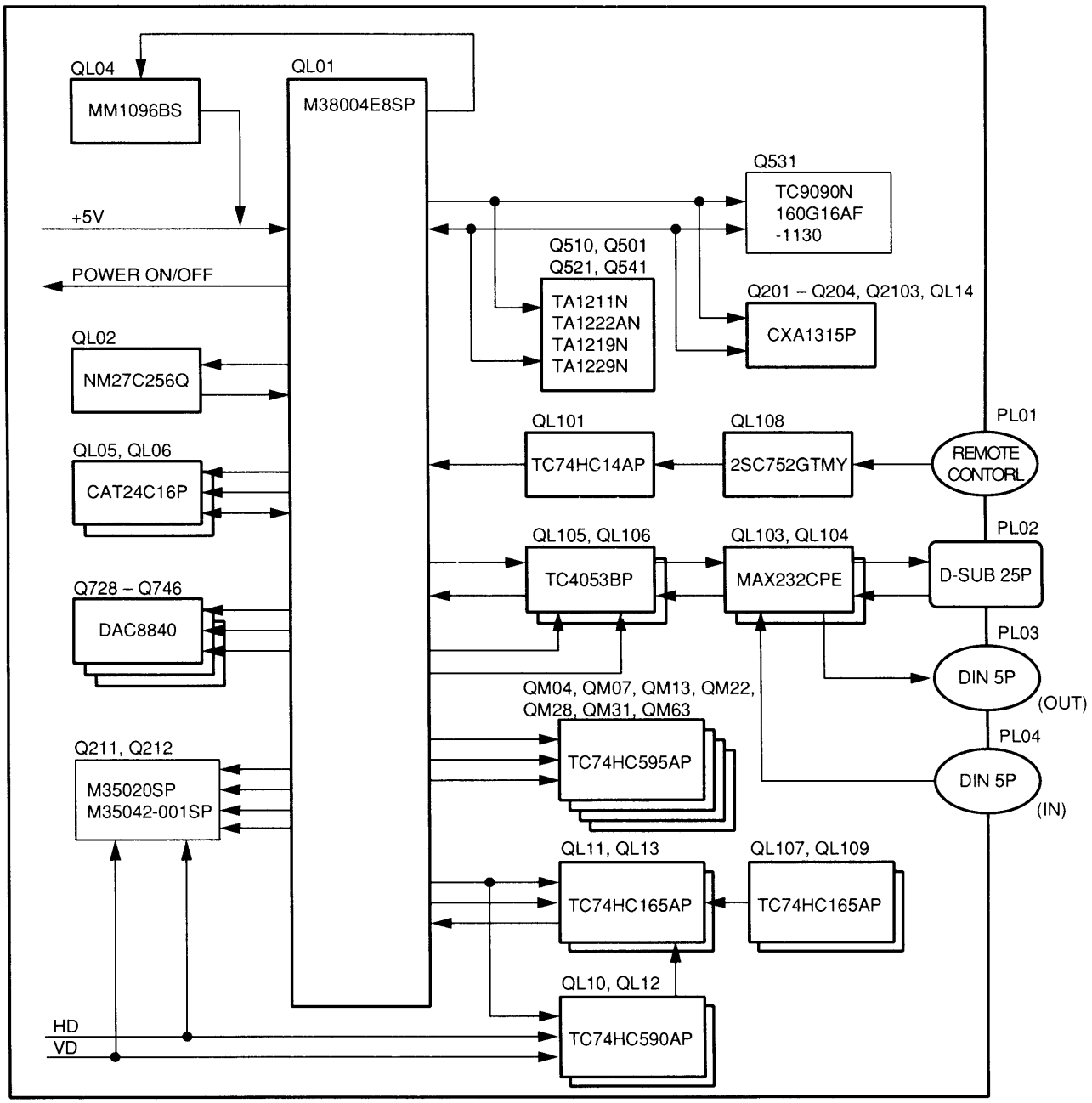


Fig. 3-1 System control block diagram

The main functions of system microprocessor is described below.

- Control input relation

  Remote control reception processing, RS-232C transmission and reception processing, RS-422 transmission and reception processing, input signal type identification process.

- System control relation

  Non-volatile memory control processing, on-screen display processing.

- Deflection/convergence system control relation

  Deflection system control processing, centering control processing, analog convergence control processing.

- Video system control relation

  Video adjustment control processing, white balance control processing, shading correction processing, color signal control processing.

The main special features in this machine model are listed below.

1-1. Convergence Circuit

The convergence circuit is controlled by the analog convergence control by the S/P control DAC, the fine adjustment is available for every point similarly to the digital convergence, and adopts the picture pursuit system where the convergence hardly gets deviated even when changing the picture size.

1-2. Input Signal Automatic Identification

The convergence bank and the source bank are identified by judging the vertical frequency/horizontal frequency of input signal. The convergence bank can memorize 7 modes in total of 15 to 18 kHz, 19 to 25 kHz, 26 to 33 kHz, 34 to 44 kHz, 45 to 59 kHz, 60 to 79 kHz and 80 to 100 kHz of horizontal frequency with the convergence adjustment/deflection adjustment data as its center, while the source bank can identify the difference of horizontal and vertical frequencies and memorize 30 modes such as picture size, picture phase, contrast, brightness, color, tint and sharpness data, which can judge the signal every time when the input signal changes, and automatically call out the adjustment data meeting it.

1-3. Adjustment Data Reading Function by Control RS-232C/RS-422

The adjustment data can be read out by controlling the RS-232C and RS-422 from the outside, and the read/write processing can be made by the dedicated software, thus facilitating a variety of adjustments.

2. SYSTEM MICROPROCESSOR BLOCK

As the system microprocessor of QL01, the 8-bit microprocessor controller (M38004E8SP) is employed.

This system microprocessor doesn't use the program area existing inside, but uses the EPROM (NM27C256Q) as the program ROM outside the QL02, thereby making it easier to change the specifications of system microprocessor and to repair the bug and to maintain the machine.

Further, the system microprocessor controls all the controls such as the input system control process, deflection system control process, video system control process, display system control process, input identification process and adjustment data input/output process, etc. as shown in Fig. 3-2 and table 3-1.

Table 3-1 Pin function

Pin No.	Name	Function	I/O
1	VCC	Power supply	I
2	SCL	I^2C bus clock for video	O
3	SDA	I^2C bus data for video	I/O
4	DAC	Clock for DAC8840/Load 1 for on-screen	O
5	DAD	Data for DAC8840/Load 0 for on-screen	O
6	DG1	Gate 1 for DAC8840/Data for on-screen	O
7	DG0	Gate 0 for DAC8840/Clock for on-screen	O
8	DA3	Data 3 for DAC8840/Load for serial parallel	O
9	DA2	Load data 2 forDAC8840/Data for serial parallel	O
10	DA1	Load data 1 for DAC8840/Clock for serial parallel	O
11	DA0	Load data 0 for DAC8840	O
12	SEL	DAC8840 OR on-screen, serial/parallel control select	O
13	PSL	Load for parallel/serial	O
14	PSD	Data for parallel/serial	I
15	PSC	Clock for parallel/serial	O
16	RCK	Load for horizontal frequency	O
17	ED1	Data 1 for non-volatile memory	I/O
18	ED0	Data 0 for non-volatile memory	I/O
19	ECK	Clock for non-volatile memory	O
20	RPC	Personal computer sending enable	O
21	TPC	Personal computer reception enable	O
22	TXD	RS-232C sending data	O
23	RXD	RS-232C reception data	I
24	VDP	Vertical retrace period pulse	I
25	RMC	Remote control reception data	I
26	CNV_{SS}	Operation mode setting	I
27	RST	External reset	I

Pin No.	Name	Function	I/O
28	RXE	RS-232C reception enable	O
29	TXE	RS-232C sending enable	O
30	XI	Input for oscillation	I
31	XO	Output for oscillation	O
32	GND	GND	I
33	D7	Data for external ROM (MSB)	I
34	D6	Data for external ROM	I
35	D5	Data for external ROM	I
36	D4	Data for external ROM	I
37	D3	Data for external ROM	I
38	D2	Data for external ROM	I
39	D1	Data for external ROM	I
40	D0	Data for external ROM (LSB)	I
41	A15	Address for external ROM (MSB)	O
42	A14	Address for external ROM	O
43	A13	Address for external ROM	O
44	A12	Address for external ROM	O
45	A11	Address for external ROM	O
46	A10	Address for external ROM	O
47	A9	Address for external ROM	O
48	A8	Address for external ROM	O
49	A7	Address for external ROM	O
50	A6	Address for external ROM	O
51	A5	Address for external ROM	O
52	A4	Address for external ROM	O
53	A3	Address for external ROM	O
54	A2	Address for external ROM	O
55	A1	Address for external ROM	O
56	A0	Address for external ROM (LSB)	O
57		N.C.	O
58		N.C.	O
59		N.C.	O
60		N.C.	O
61		N.C.	O
62	ONW	External weight	I
63		N.C.	O
64	SWT	Power supply switch	O

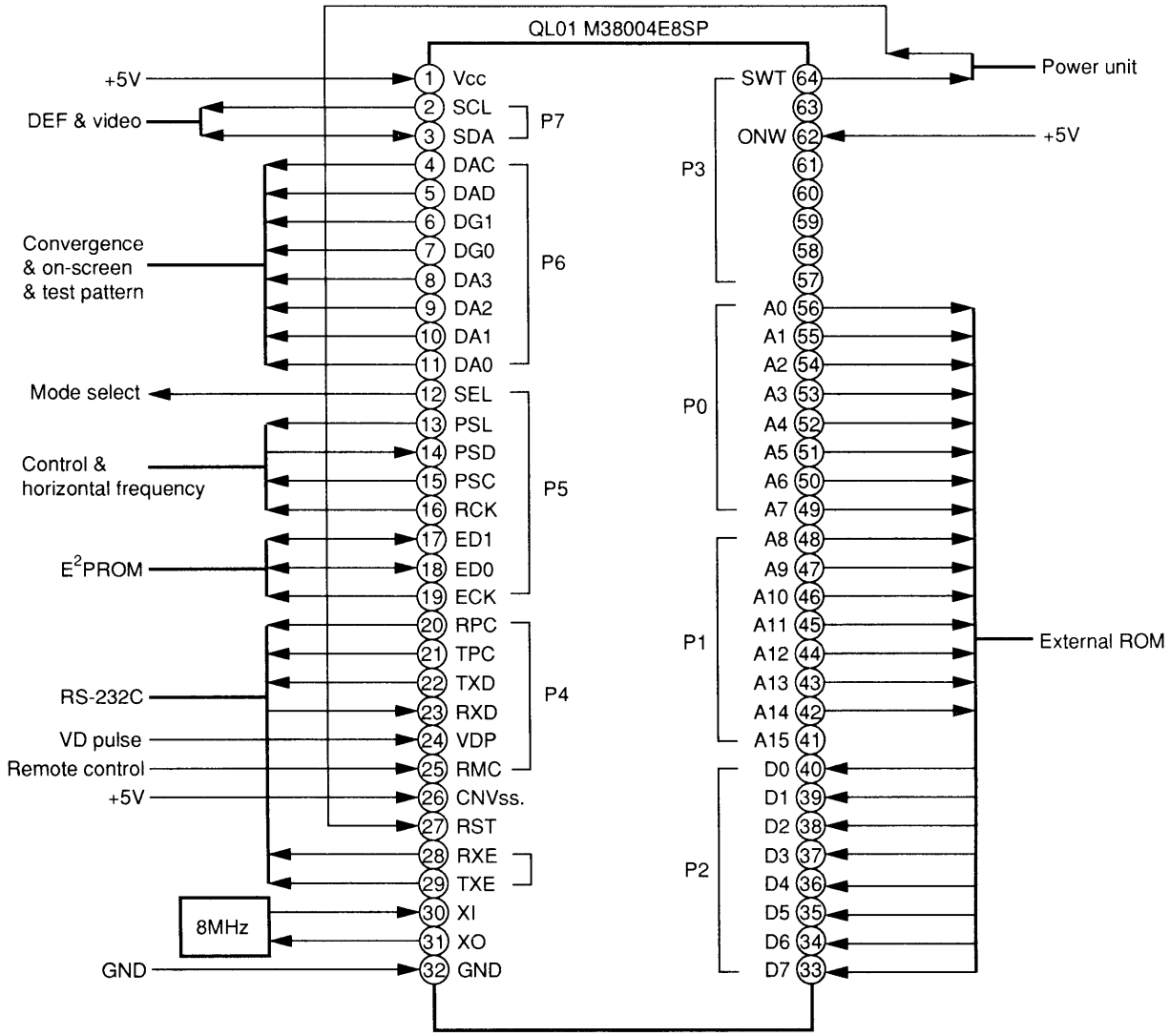


Fig. 3-2 Pin layout

3. MICROPROCESSOR RESETTING BLOCK

As shown in Fig. 3-3, the microprocessor resetting block adopts the watch dog timer (MM1096BS) of QL04 as the reset IC.

The reset IC of QL04 uses as input the clock signal for non-volatile memory described later, judges that the system microprocessor (M38004E8SP) of QL01 is running recklessly if the clock signal is absent for about 1 second, and supplies the reset signal to the system microprocessor of QL01 at the timing as shown in Fig. 3-4.

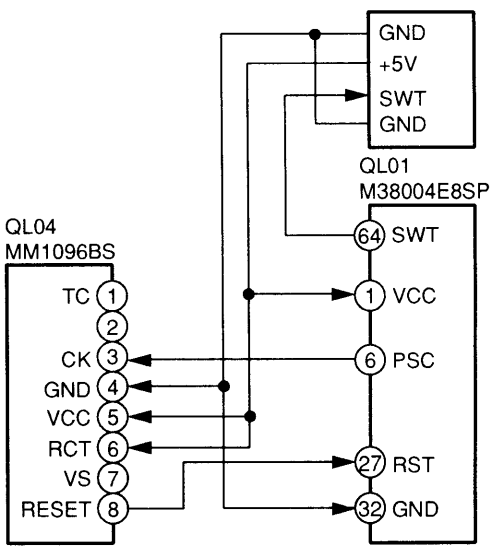


Fig. 3-3 Power source resetting block

4. REMOTE CONTROL RECEPTION BLOCK

The remote control reception block converts the remote control signal of 3 V supplied from the accessory remote control unit (CT-9847) connected to the remote control terminal into the level of 5V by the transistor (2SC752GTMY) of QL108 as shown in Fig. 3-5, and after passing it through the noise removal filter, shapes the waveform by passing it through the buffer (TC74HC14AP) of QL01.

And, because the wireless remote control light reception sensors are arranged on front and rear of the unit, the signal is selected by the AND gate (TC74HC08AP) and is supplied to the system microprocessor of QL01 at the timing as shown in Fig. 3-6.

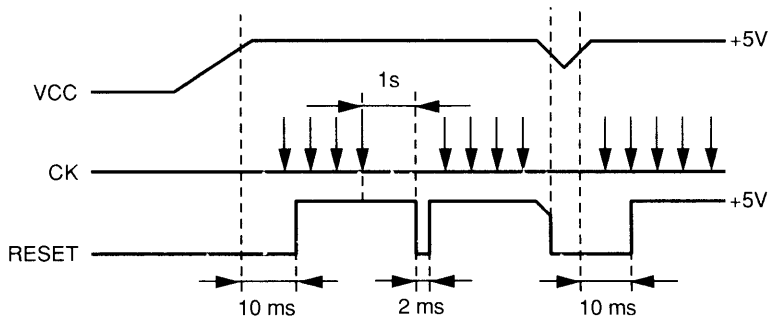


Fig. 3-4 MM1096BS reset timing diagram

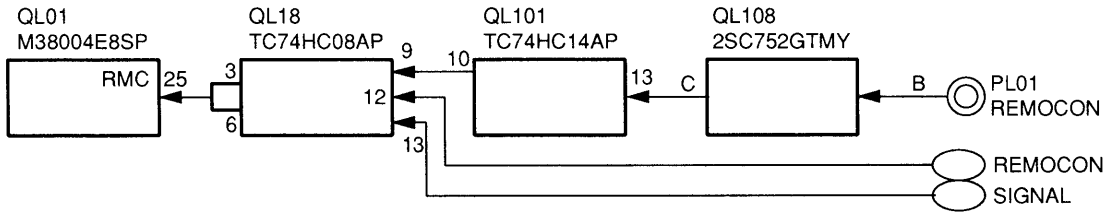


Fig. 3-5 Remote control reception block

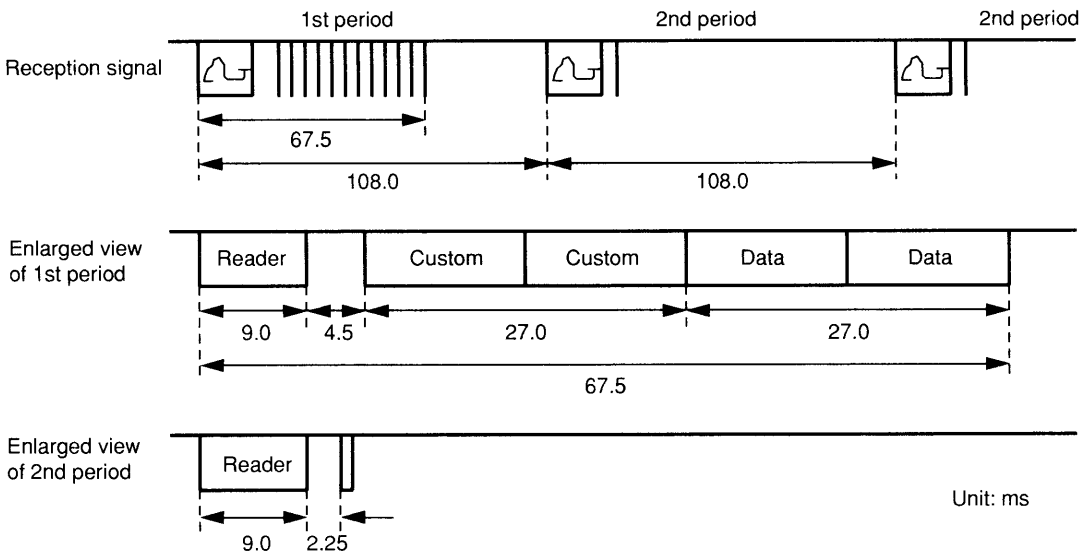


Fig. 3-6 Remote control reception signal timing diagram

5. RS-232C TRANSMITTER/ RECEIVER BLOCK

In the RS-232C transmit/receive section, as shown in Fig. 3-7, RS-232C transmit/receive signals with timings as shown in Fig. 3-8 sent from PL02 RS-232C connector (D-SUB 25P), PL04 system bus input connector (DIN 5P), and PL03 system bus output connector (DIN 5P) are level-converted by the RS-232C DC/DC converter consisting of QL103, QL104. While the RS-422 transmit/receive signal is level-converted by RS-422 driver/receiver consisting of QL102 (DS8921AN). And one of them is selected in passing through analog switches (TC4053BP) of QL105 and QL106.

In this instance, they operate as the switching circuit in the transmitter/receiver of RS-232C and RS-422 according to the combination of DSR signal of pin 20 of PL02 and each signal of pin 20 (RPC), pin 21 (TPC), pin 28 (RXE) and pin 29 (TXE) of QL01.

As an example of communication conditions, Fig. 3-8 is calculated upon the transmission speed of 4800 bps, no parity bit and with the bit length being 8-bit and stop bit being 1 bit.

The timing of RS-422 is identical to the above mentioned RS-232C, but the information is transmitted with the balance transmission structured of two equal signal lines.

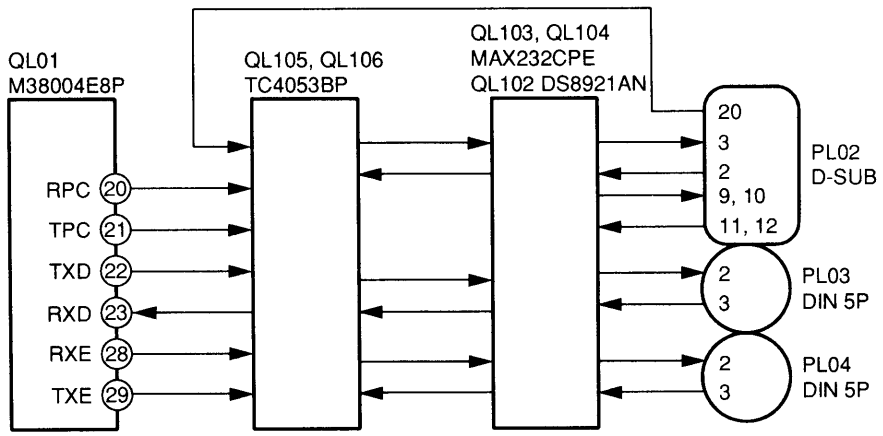
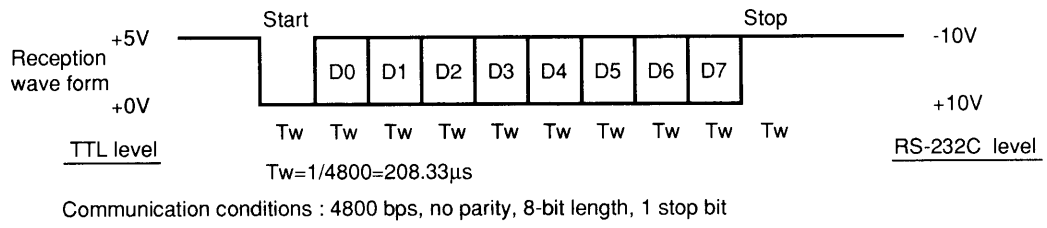


Fig. 3-7 RS-232C/RS-422 transmitter/receiver block



Communication conditions : 4800 bps, no parity, 8-bit length, 1 stop bit

Fig. 3-8 RS-232C timing diagram

6. CONTROL MODE READING BLOCK

The control reading block reads two kinds of data as shown in Fig. 3-9 at the timing as shown in Fig. 3-10 .

The 1st data reads the SL01 dip switch state and the mode states of wired remote control, RS-232C and RS-422 by using the P/S (TC74HC165AP) of QL107 and QL109.

The 2nd data reads the number of horizontal scanning lines for input signal identification described later by using the P/S (TC74HC165AP) of QL11 and QL13.

In the input signal type identification process, the value of counter (QL10, QL12) by the HD pulse from the outside is read out as shown in Fig. 3-9, and moreover the interruption process is conducted by the system microprocessor of QL01 and the VD pulse is discriminated by checking the time of vertical feedback period of input signal and the number of scanning lines during that period.

Thereby, 7 kinds of convergence bank signal and 30 kinds of source bank signal are identified, and the adjusted values of analog convergence and user adjustment item are controlled by mode respectively.

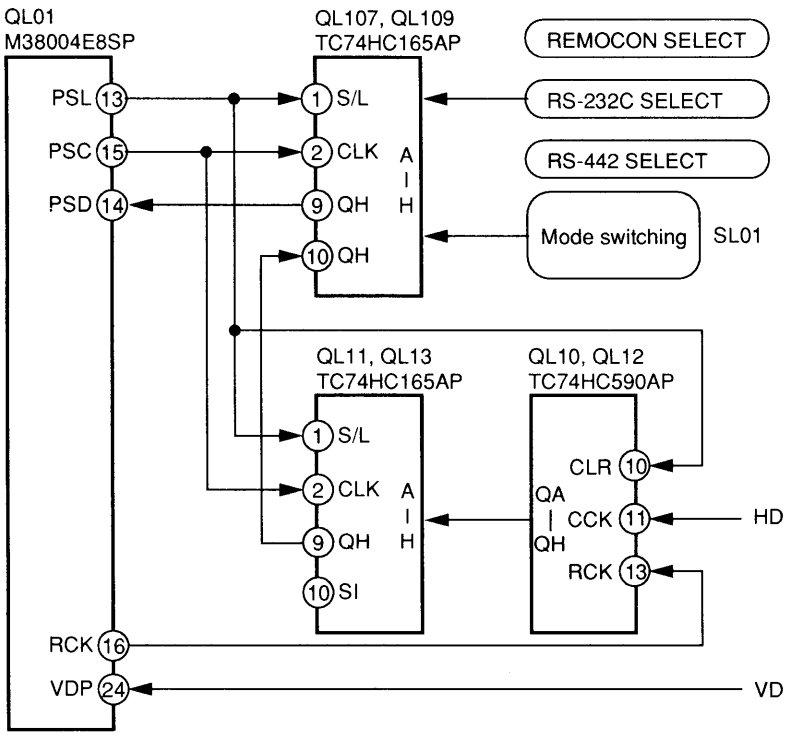


Fig. 3-9 Control mode taking block

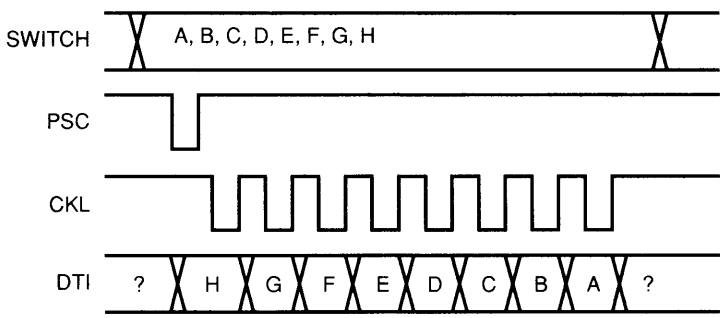


Fig. 3-10 TC74HC165AP timing diagram

7. NON-VOLATILE MEMORY BLOCK

The non-volatile memory block is used for storing each of adjusting data to the nonvolatile memory (CAT24C16P) of QL05 and QL06 as shown in Fig. 3-11.

The system microprocessor of QL01 reads out and writes in all the adjusting data at the timing as shown in Fig. 3-12 when the power source is switched on (AC ON), thereby maintaining the previous state.

However, if any trouble (power source shut-off, etc.) should happen when writing the adjusting data, an error may happen to the written data, and if it is judged to be an error, the initial data which is stored into the system microprocessor of QL01 is read out and written.

Here, the adjusted value of convergence bank is stored to the non-volatile memory of QL05 and the adjusted value of source bank is stored to the non-volatile memory of QL06.

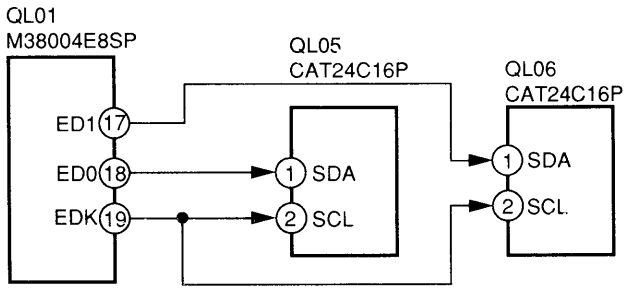


Fig. 3-11 Non-volatile memory block

8. ON-SCREEN DISPLAY BLOCK

The control signal is supplied at the timing as shown in Fig. 3-14 and Fig. 3-15 which is further shown in Fig. 3-13, and the on-screen display block generates the signal for on-screen character inscription at the timing predetermined by the self-running oscillation frequency in accordance with the VD pulse and HD pulse which are supplied separately.

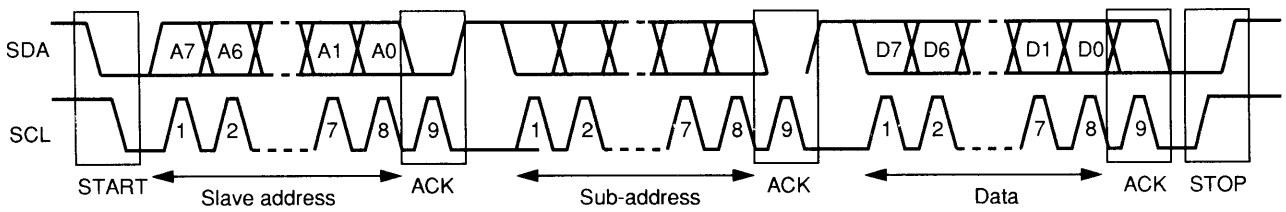


Fig. 3-12 I²C bus timing diagram

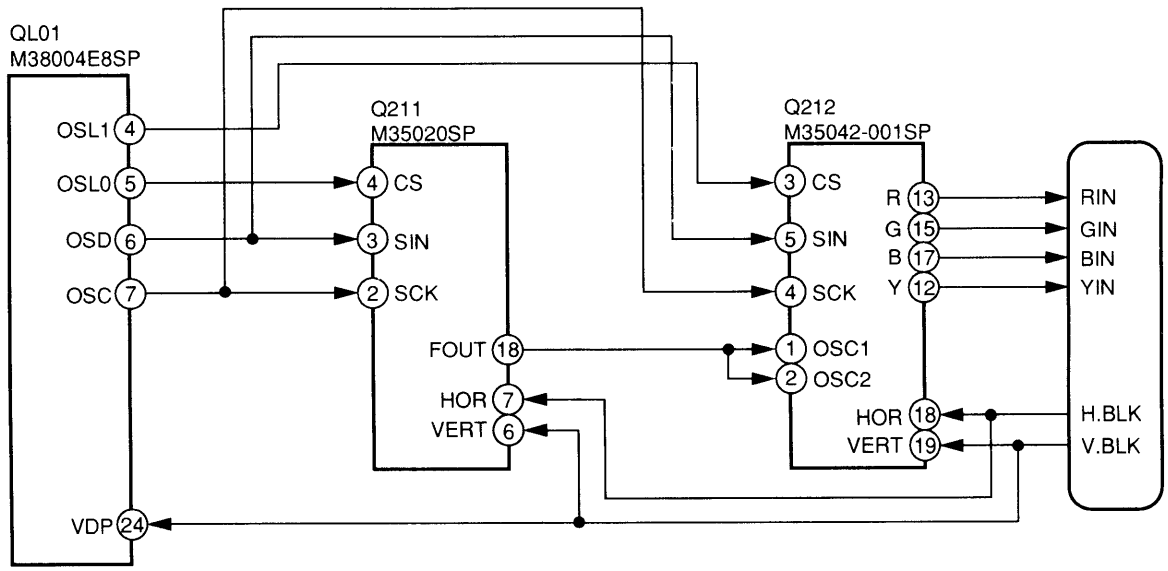


Fig. 3-13 On-screen display block

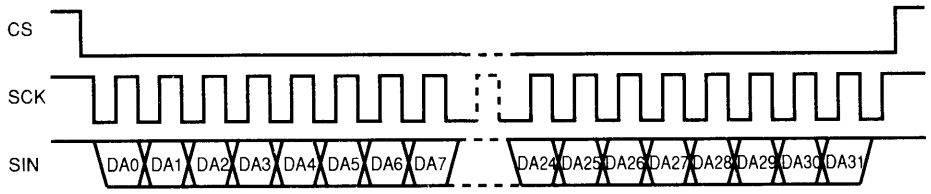


Fig. 3-14 M35020SP timing diagram

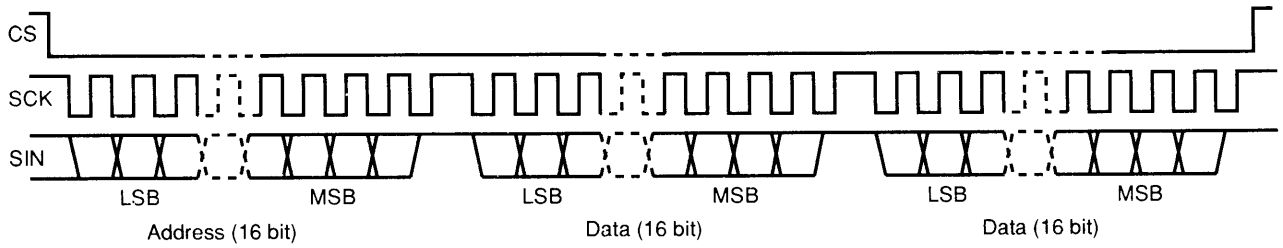


Fig. 3-15 M35042-901SP timing diagram

9. CONVERGENCE/DEFLECTION SYSTEM CONTROL BLOCK

The deflection system control block performs the analog convergence/deflection system control at the timing as shown in Fig. 3-16 as illustrated in Fig. 3-17.

The load signal of gain DAC (DAC8840) is supplied for its operation by setting the data to the decoder IC (TC74HC4514AP) of Q726 and Q727 from the microprocessor of QL01.

These signals maintain the previous state in the full adjusting data reading when the power source is ON, and restores the state if the trouble such as noise should happen and the data becomes abnormal to the output signal in the refresh process (periodical data output process).

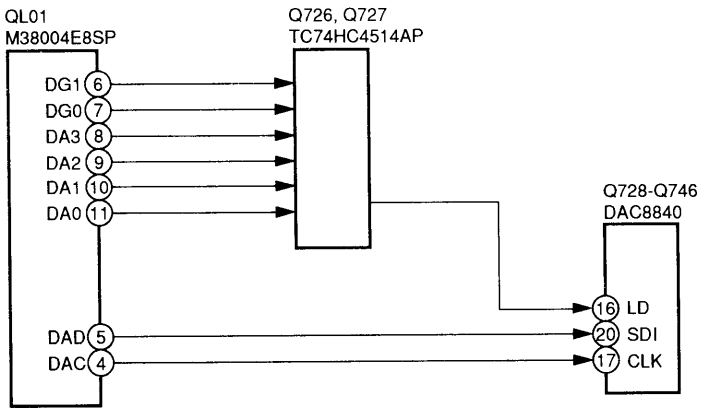


Fig. 3-16 Convergence/deflection system control block

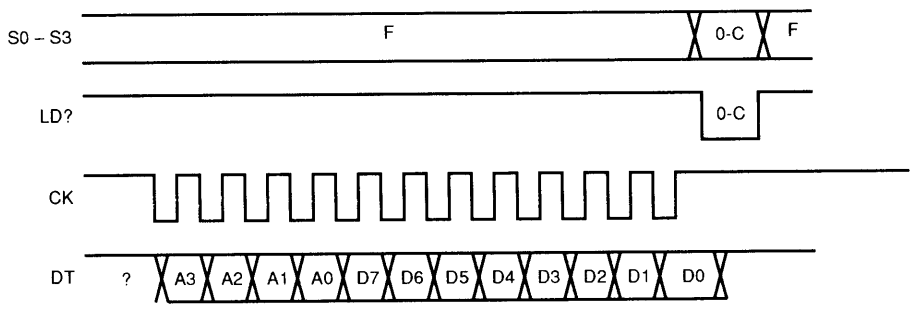


Fig. 3-17 DAC8840 timing diagram

10. VIDEO SYSTEM CONTROL BLOCK

The video control block performs the video process, color signal process, color temperature process and moreover switching control process at the timing as shown in Fig. 3-12 and also the shading process at the timing as shown in Fig. 3-17 as illustrated in Fig. 3-18.

(1) Q510 (TA1211N), Q501 (TA1222AN), Q521 (TA1219), Q541 (TA1229N) and Q531 (TC9090C) of video control LSI:

The control signals for adjusting various images

(2) The up-converter gate array (160G16AF-1130):

NTSC conversion and process

(3) I^2C DAC (CXA1315P) of Q201 to Q204, Q2103 and QL14:

Contrast adjustment, brightness adjustment, color temperature adjustment, trimming adjustment and switching control

(4) Gain DAC (DAC8840) of Q206:

Control signal for correcting the shading

These signals maintain the previous state in the full adjusting data read when the power source is ON and restore the normal state when the trouble such as noise happens and the data becomes abnormal to the output signal in the refresh process (periodical data output process).

11. VARIOUS CONTROL MODES

This system covers various control modes in the operation as shown in Fig. 3-19.

At first the system becomes the "initialization mode" after the AC is turned on, reads the previous adjustment data from the non-volatile memory, and sets various operation states according to that state.

The state where the sub-power source is off is called the "stand-by mode", and only the main power switch is accepted in this mode.

The state where the sub-power source is on is called the "normal mode", and the usual operation is done with this mode as its standard.

The "normal mode" of usual operation can be shifted to the "test mode" for various kinds of adjustment, while the "test mode" can be shifted to the ID controlling "ID mode", the video system controlling and setting "video mode", the unit adjusting "service mode", the state displaying "special mode, the CONV bank data setting "CONV mode" and the SOURCE bank data setting "SOURCE mode".

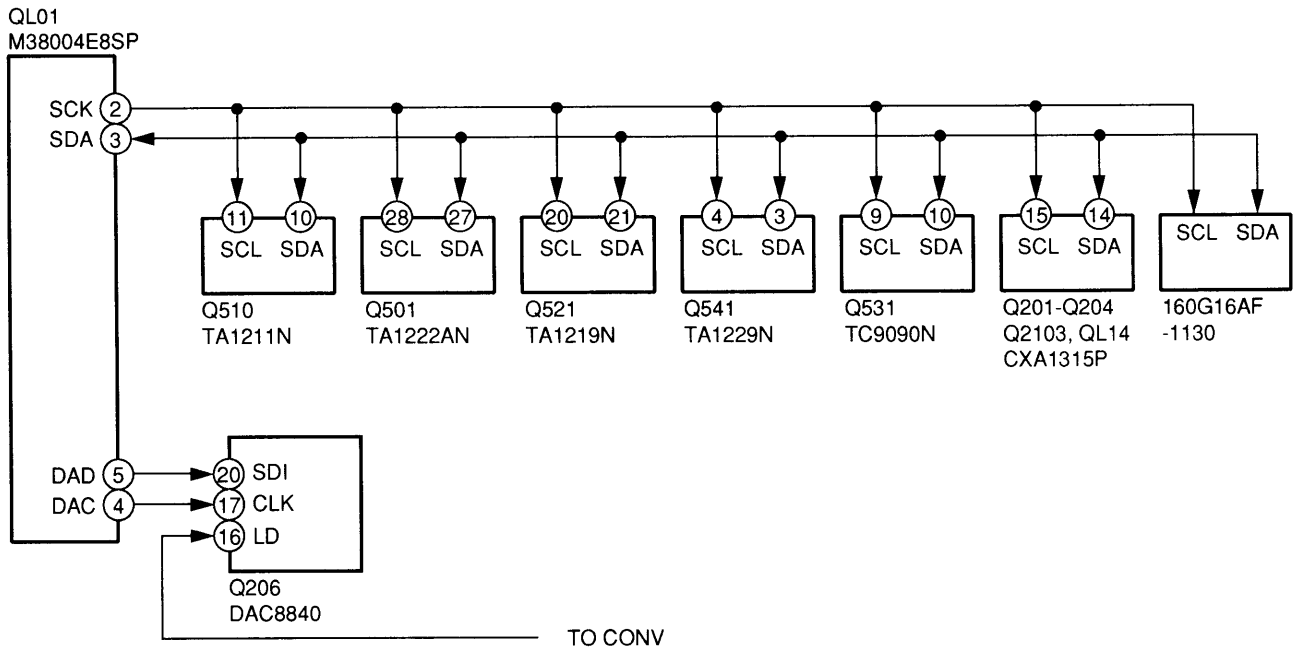


Fig. 3-18 Video system control block

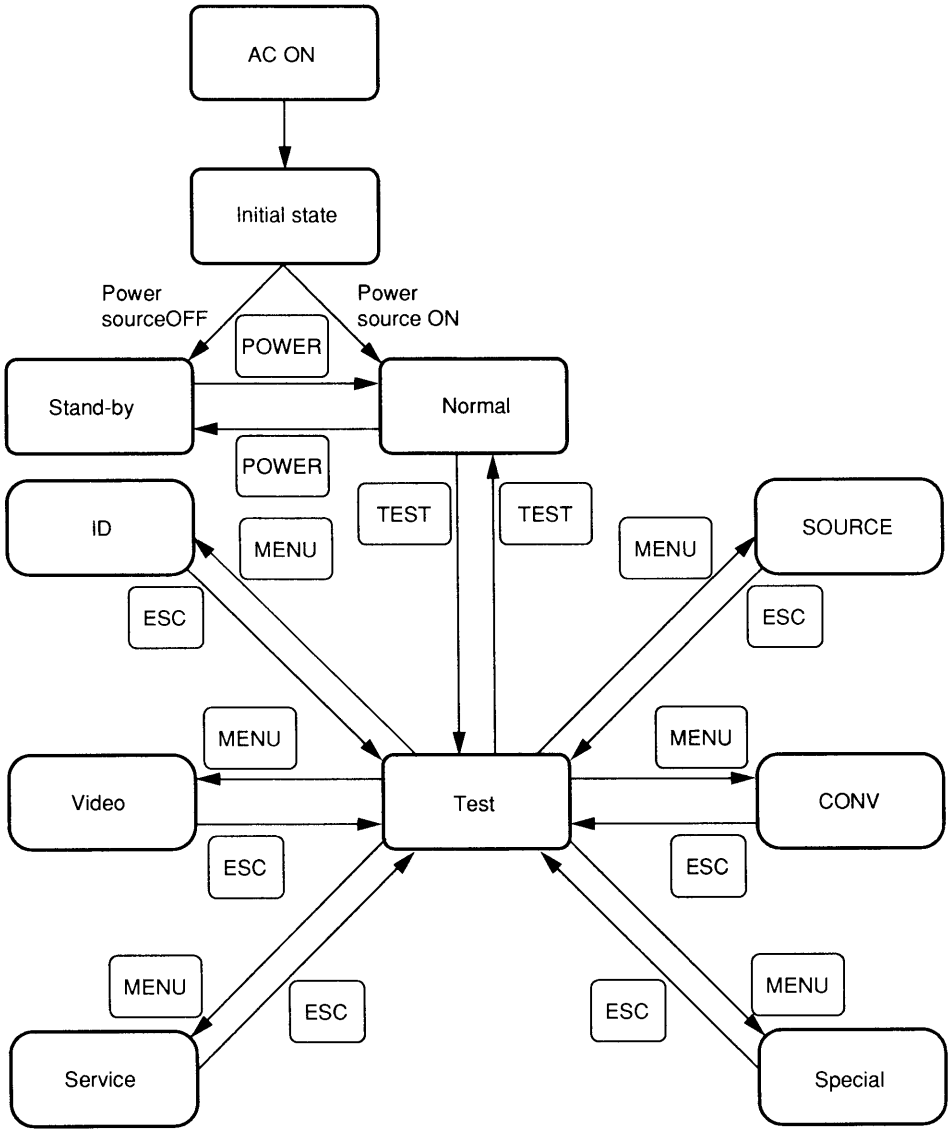


Fig. 3-19 Various control mode transmission diagram

12. RS-232C/RS-422 CONTROL METHOD

The external control method by the RS-232C/RS-422 is to be explained hereunder.

The signals shall be connected in straight system at the D-SUB25 pin connector of PL02 as shown in table 3-2 and table 3-3. This is because the signals are connected in such that they may cross inside the main body.

Table 3-2 RS-232C connection conditions

Pin No.	Name of signal	Contents of signal	Input/output		Signal from external source
2	RXD	Reception data	I	←	TXD
3	TXD	Transmission data	O	→	RXD
4	CTS	Transmission permission	I	←	RTS
5	RTS	Transmission request	O	→	CTS
6	DTR	Data terminal ready	O	→	DSR
7	S.G	Signal ground	I	←	S.G
20	DSR	Data set ready	I	←	DTR

Table 3-3 RS-422 connection conditions

Pin No.	Name of signal	Contents of signal	Input/output		Signal from external source
7	S.G	Signal ground	I	←	S.G
9	RXD (+)	Reception data	I	←	RXD (+)
10	RXD (–)	Reception data	I	←	RXD (–)
11	TXD (+)	Transmission data	O	→	TXD (+)
12	TXD(–)	Transmission data	O	→	TXD(–)
13	SEL	RS-422 select	I	←	S.G

The communication conditions should be set as shown in table 3-4.

Table 3-4 RS-232C/RS-422 communication conditions

	Condition
System	Transmission speed - 4800, Parity bit - Non, Data length - 8 bits, Stop bit - 1 bit Communication style
Format	1 block should be composed of STX (1 byte) + ID (2 bytes) + CMD (3 bytes) + ETX (1 byte). Here, the STX is 02h, the ETX is 03h, the ID is alpha numerical letter (0 to F) + aster isk (*) and the CMD is the RS-232C/RS-422 command letter line (capital letter) shown in Table 3-5 – Table 3-12.

The ID is the individual identification numbers when multiple projectors are connected, makes it possible to control them at the same time and usually is set to "01". If the ID number has not been set, no RS-232C command can be accepted.

The ID type basically adopts 2 bytes (0 to F) in hexadecimal digit and can be set to 256 types from "00" to "FF". Further by using the asterisk (*) when controlling the set, the multiple sets can be controlled simultaneously instead of all the hexadecimal characters. However, the asterisk (*) can not be used when setting the identification of projector.

As the care when sending the command, at least the time interval of around 100 ms must be provided when sending the commands. If the interval should be too short, the set doesn't work due to the erroneous recognition of command.

Especially when sending more than 3 commands continuously in the item which requires a long process time such as the power source ON/OFF and input switching, the time interval from 3 to 7 seconds must be provided on and after the 3rd command.

To the contrary, in case of the time interval of more than 1 minute, the commands which have thus far been recognized become invalid.

13. TABLE OF CONTROL ITEM BY EACH CONTROL MODE

The table of control items that can be operated for each control mode is listed in the table of control items of table 3-5. This table lists up the operation operable mode for every item, remote control code and RS-232C/RS-422 command.

Some commands of common mode don't work depending on the selected item.

Table 3-5

Item	Contents in normal mode	RS-232C/RS-422 CMD			
Power ON/OFF	Power ON/OFF	PWR	PON	POF	
VIDEO	Video input selection	VNA			
Y/C	Y/C input selection	VNB			
S-VIDEO	S-VIDEO input selection	VNC			
RGB1	RGB1 input selection	VND			
RGB2	RGB2 input selection	VNE			
YPbPr	YPbPr input selection	PBR	PBO	PBF	
MUTE ON/OFF	Video mute	MSW	MON	MOF	
MENU	Display mode switching	MNU			
PICTURE MENU	Video system adjustment	PMU			
PICTURE REST	Video system adjusting reset	PRS			
CENTERING	Centering adjustment	CEN	CER	CEG	CEB
SHIFT	Horizontal/vertical picture position adjustment	SFT			
SIZE	Horizontal/vertical picture size adjustment	SIZ			
SOURCE MODE 1-30	SOURCE mode	SMA	S01	→	S30
TEST MODE	Test mode switching	AJY			
ID SET	ID setting	IDS			

Table 3-6

Item	Contents in test mode	RS-232C/RS-422 CMD
TEST PATTERN	Test pattern switching	TST
SHIFT	Horizontal/Vertical picture position adjustment	SFT
SIZE	Horizontal/Vertical picture size adjustment	SIZ
CONV MODE	Convergence adjusting mode	CNV
CONV SIZE	Convergence size adjustment	CSZ
LIN	Linearity adjustment	LIN
TILT	TILT adjustment	TIL
BOW	BOW adjustment	BOW
KEY	KEY adjustment	KEY
PIN	PIN adjustment	PIN
FOCUS	Focus adjustment	FCS
WHITE BALANCE	White balance adjustment	WHT
TRIMMING ADJ	Trimming adjustment	TRM
MENU	Display mode switching	MNU
NORMAL MODE	Test mode releasing	AJN

Table 3-7

Item	Contents in ID mode	RS-232C/RS-422 CMD
ID. CLR	ID erasing	IDC
ID. SET	ID setting	IDS
ID. ALL	* input	IDA
0	0 input	VN0
1	1 input	VN1
2	2 input	VN2
3	3 input	VN3
4	4 input	VN4
5	5 input	VN5
6	6 input	VN6
7	7 input	VN7
8	8 input	VN8
9	9 input	VN9
A	A input	VNA
B	B input	VNB
C	C input	VNC
D	D input	VND
E	E input	VNE
F	F input	VNF

Table 3-8

Item	Contents in video mode	RS-232C/RS-422 CMD
ABL	ABL level adjustment	VN0
S. VER	Shading vertical direction adjustment	VN1
S. AMP	Shading amplifier adjustment	VN2
S. BAL	Shading balance adjustment	VN3
EB. SW	Black expansion ON/OFF	VN4
COLOR SW	Color switch ON/OFF	VN5
COMBI	Combination ON/OFF	VN6
MULTI	Multi mode ON/OFF	VN7
TRIMMING	Trimming mode ON/OFF	VN8

Table 3-9

Item	Contents in service mode	RS-232C/RS-422 CMD
MONITOR	Monitor select (Y/B – Y/R – Y/G – Y)	VN0
BELL FIL	Bell adjustment	VN1
SECAM R – Y	Black level (R – Y) adjustment	VN2
SECAM B – Y	Black level (B – Y) adjustment	VN3
SUB CONTRAST	Sub contrast adjustment	VN4

Table 3-10

Item	Contents in special mode	RS-232C/RS-422 CMD
0	RAM area (040-05F)	VN0
1	RAM area (060-07F)	VN1
2	RAM area (080-09F)	VN2
3	RAM area (0A0-0BF)	VN3
4	RAM area (0C0-0DF)	VN4
5	RAM area (0E0-0FF)	VN5
6	RAM area (100-11F)	VN6
7	RAM area (120-13F)	VN7
8	RAM area (140-15F)	VN8
9	RAM area (160-17F)	VN9
A	RAM area (180-19F)	VNA
B	RAM area (1A0-1BF)	VNB
C	RAM area (1C0-1DF)	VNC
D	RAM area (1E0-1FF)	VND
E	RAM area (200-21F)	VNE
F	RAM area (220-23F)	VNF

Table 3-11

Item	Contents in normal mode	RS-232C/RS-422 CMD		
UP	Item select UP	VUP		
DOWN	Item select DOWN	VDW		
LEFT	Item select LEFT	VLF		
RIGHT	Item select RIGHT	VRG		
MEMORY	Adjusting data write	MEM	MEO	MES
ESCAPE	Item releasing	ESC		

Table 3-12

Item	Contents in normal mode	RS-232C/RS-422 CMD		
R-ON/OFF	Raster R ON/OFF	RSW		
G-ON/OFF	Raster G ON/OFF	GSW		
B-ON/OFF	Raster B ON/OFF	BSW		
R-SEL	Raster R selection	SLR		
G-SEL	Raster G selection	SLG		
B-SEL	Raster B selection	SLB		
UP	Adjusting value vertical direction increase/Item select UP	VUP		
DOWN	Adjusting value vertical direction decrease/ Item select DOWN	VDW		
LEFT	Adjusting value horizontal direction decrease/item select LEFT	VLF		
RIGHT	Adjusting value horizontal direction increase/item select RIGHT	VRG		
SPEED	Adjusting value increase/ decreasee speed switching	VSP		
MEMORY	Adjusting data write	MEM	MEO	MES
ESCAPE	Item relasing	ESC		
FUNCTION	Multi-purpose key	FNC		

SECTION IV
CONTROL CIRCUIT

1. OUTLINE

The control circuit board is composed of 3 circuits shown below.

- Microprocessor circuit
- Internal sync signal generating circuit
- Test pattern generating circuit

The present paragraph explains the details of sync signal generation circuit and test pattern generation circuit. (For the microprocessor circuit, refer to section 3).

2. INTERNAL SYNC SIGNAL GENERATION CIRCUIT

2-1. Outline

This is the circuit to generate the horizontal sync signal (fH) and vertical sync signal (fV) to be supplied to the system during no signal mode and the test mode.

The fH can output 7 kinds of frequency, namely 17 kHz, 24 kHz, 31 kHz, 37 kHz, 50 kHz, 70 kHz and 90 kHz corresponding to the convergence adjusting bank, and these frequencies is controlled by the microprocessor.

The fV is a single frequency of 60 Hz.

2-2. Construction

Each frequency of fH and fV is generated by dividing the basic clock of 3.58 MHz respectively. Fig. 2-1 shows this situation.

QM60 is C-MOS.NOT gate, which, together with a crystal vibrator, build up an oscillator. QM61 and QM62 are the frequency dividers for fV, and the frequency division ratio is fixed to 1/59648. On the other hand, QM64 is the frequency divider for fV, and the frequency division ratio is determined by the parallel data of 8 bits given from QM63. QM63 is the serial/parallel conversion IC, and the serial data given from the microprocessor is converted into the parallel data by the IC.

QM65 is a flip-flop and is used to synchronize fH with fV. fV is latched with fH to assort the edge of fV with that of fH. In addition, the frequency divider QM61 is reset at the front edge of fV for keeping the cycle of fV to be constant.

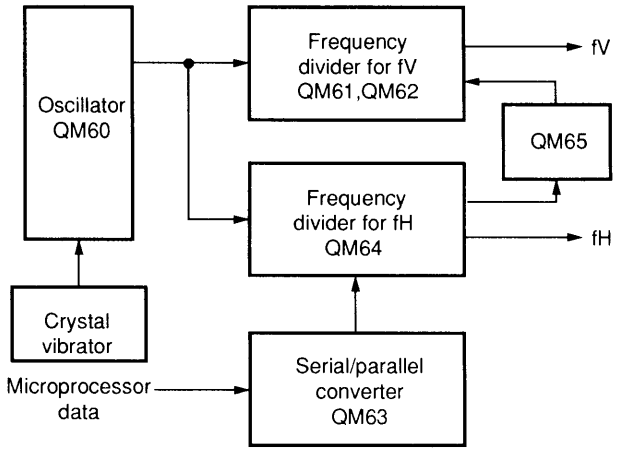


Fig. 4-1 Internal sync signal generation circuit

3. TEST PATTERN GENERATION CIRCUIT

When entering the test mode, the external video sync signal is switched from the internal sync signal described in the preceding Item 2. The test pattern generation circuit outputs various patterns in synchronizing with the internal signal. Fig. 4-2 shows the outline of test pattern generation circuit.

The test pattern generation circuit is composed of the PLL block and the pattern generation block. In PLL block, the internal signal is synchronized and the reference clock (64 fH) of pattern generation is also generated.

The kinds of pattern that is generated in the pattern generation block are 5 kinds of cross pattern, coarse cross hatch, close cross hatch, H-character and dot. In addition, when adjusting the convergence, it is also possible to display the marker showing the present adjusting point. The details of each circuit are described in the following pages.

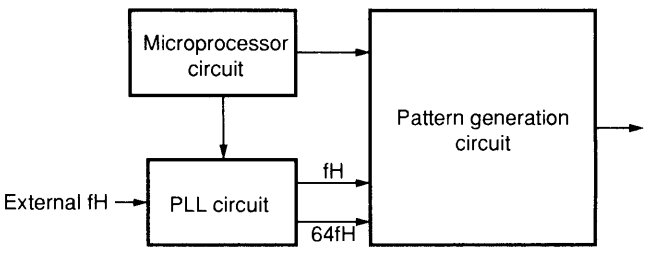


Fig. 4-2 Test pattern generation circuit

3-1. PLL Block

3-1-1. Outline

The vertical line of test pattern is formed with the 64 fH as the reference clock. In PLL block, the internal sync signal is synchronized and 64 fH which becomes the system clock of pattern generation circuit is generated. (Refer to Fig. 4-3.)

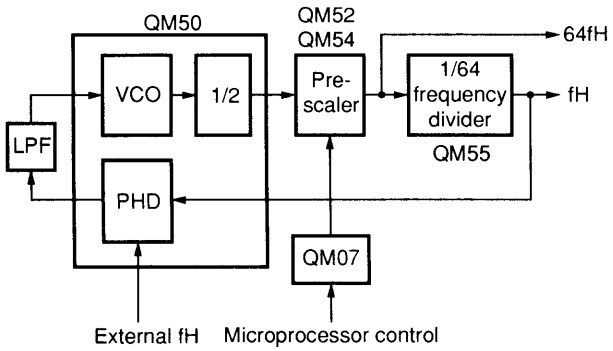


Fig. 4-3 PLL circuit

3-1-2. Configuration

The circuit is composed of the PLL dedicated IC : TLC2932 (QM50) which can build up the PLL with 1 chip. VCO and the phase comparator are accommodated into 1 chip of the IC, and the oscillation range of VCO is within approx. 20 MHz to 70 MHz.

The frequency divider used in the PLL circuit is composed of the pre-scaler and 64-frequency divider. The pre-scaler is composed of QM52 and QM54, and can set 4 kinds of frequency division ratio of 1/2, 1/4, 1/8 and 1/16.

The performance of IC can oscillate up to approx. 70 MHz as described above, but the maximum oscillation frequency is set to around 40 MHz as the EMC countermeasure. VCO output from QM50 (which is already divided into 1/2 frequency inside the IC) is further divided from 1/2 to 1/16 frequency with the pre-scaler. The signal becomes the reference clock of 64 fH.

Further the signal is divided in 1/64 frequency by QM55 and becomes fH. The phase comparator compares fH with the phase of input internal sync signal.

QM54 consisting of the pre-scaler is the buffer equipped with the enable terminal, and selects which signal should be enabled out of 1/2 division to 1/16 division output from the counter (QM52). The division ratio of pre-scaler can be set with the parallel data of 4 bits given from QM07. QM07 is a serial/parallel conversion IC and the data is supplied from the microprocessor.

3-2. Pattern Generation Block

3-2-1. Outline

The kinds of pattern generated from the pattern generation block are 5 kinds of cross pattern, coarse cross hatch, close cross hatch, H-character and dot. When adjusting the convergence, the block also generates the marker showing the present adjusting point. These patterns are formed by combining, according to the purpose, the vertical line and horizontal line output from the vertical line generation circuit and horizontal line generation circuit which is as described as follows.

3-2-2. Vertical Line Generation Block

The vertical line of pattern is formed on the basis of the reference clock of 64 fH generated by the PLL circuit. Therefore, what 1H is divided into 64 becomes the minimum unit of vertical line.

To indicate the vertical line, it is decided first which clock is set to the 1st line (start line). Next, it is decided every how many clock (interval) the line is output. Referring to Figs. 4-4 and 4-5, the circuit operation is explained. QM05 is the counter to set the start line.

(1) The initial value is loaded with the horizontal sync signal as the reset signal.

(2) The count operation is started with the 64 fH (2) as a clock.

(3) Reaching the specified count value, QM05 changes to "H" level from "L" level.

(4) QM05 signal alone doesn't become the line signal. This signal and a signal delayed by 1 clock in QM12 flip-flop are NORed, and the resultant 1 clock pulse signal is used as a signal for first line.

(5) QM05 not only decides the position to the 1st line but also makes QM06 for interval count to be the enable state.

QM06 in the enabled state outputs 1 clock width pulse at every preset interval.

(6) This pulse signal is combined with the signal (4) after delaying 1 clock with the flip-flop of QM12-2, and then formed the vertical line signal pulse. The starting position and interval data are given to QM05 and QM06 from the serial/parallel conversion IC (QM04).

The pattern generation circuit can also output the convergence adjusting marker. The marker is of square shape which surrounds the cross point of cross hatch pattern.

The vertical line forming the marker uses the lines before and after 1 clock of cross hatch pattern. The vertical line generation circuit forms the vertical line for marker at the same time. Namely, the circuit forms the line with 3 lines/set against 1 line.

(7) The procedure to form the line of 3 lines/set is as follows;

The pattern position signal formed in (6) is input to the shift register QM36 and the pattern position signal of 3 different kinds of phase is extracted.

The first phase signal (6) corresponds to the left line of marker and the second phase signal (7) to the cross hatch signal. Next, the third phase signal (8) corresponds to the right line of marker.

(8) The pulse of pattern position signal as mentioned above has 1 clock width of system clock (64 fH) of pattern generation circuit. When the signal is projected to a large type screen like a projector, it becomes a considerably thick pattern. A fine pattern (9) is created by differentiating the pattern signal obtained there. The differentiation circuit is formed with the circuit consisting of QM45 as its center. The OP amp. QM47 gives the offset to the signal which is differentiated on the basis of the FV conversion voltage given from the microprocessor. Thereby, the threshold of differentiation waveform vertically moves according to the frequency of input signal so that the pattern having a constant thickness at all times is obtained (9).

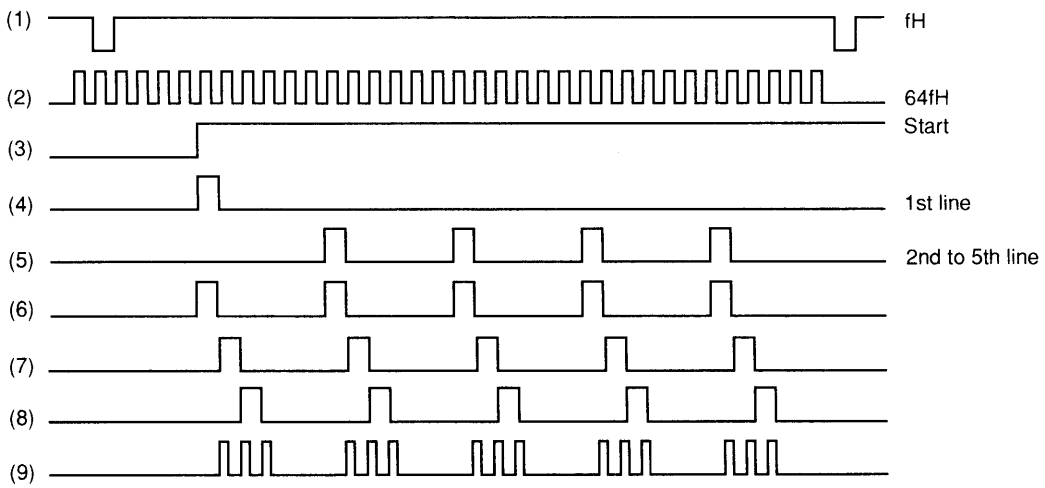


Fig. 4-4 Timing chart

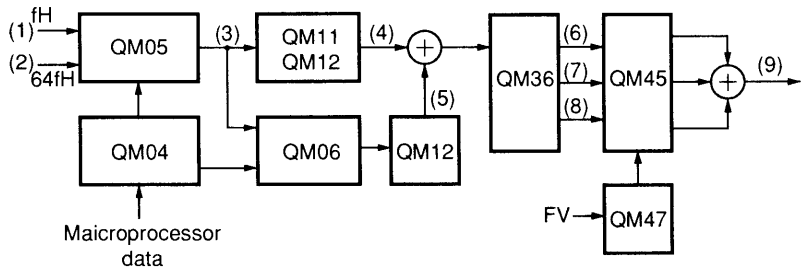


Fig. 4-5 Vertical line generation circuit

3-2-3. Horizontal Line Generation Block

The horizontal line generation circuit is basically identical to the vertical line generation circuit. What differs from the latter is to use the horizontal 1 line to form the line instead of using the clock signal. The horizontal line generation circuit counts the number of horizontal lines. Further, when forming the horizontal line above and below the marker, the former uses the fore and after lines having the space of 1/8 the pattern interval instead of using the line before and after 1 line.

This is for making the apparent marker size to be constant even if the signals of various line numbers is input. The pattern start position is set to the counter composed of QM14 and QM15, and the pattern interval is set to the counter composed of QM23 and 24. QM21 is the counter to form the space of 1/8 the pattern interval.

The vertical line is also formed with 3 lines/set.

3-2-4. Cross Hatch Pattern

This is the circuit to output the cross hatch necessary to adjust the convergence. The cross hatch pattern is formed by the logical OR of each center line of 3 lines/set that obtained by the vertical and horizontal line generation circuit. The cross hatch pattern can output the coarse cross hatch of 5 x 5 and the close cross hatch of 13 x 11.

The horizontal line is formed with 1 scanning line as earlier described. Which line should be set to the 1st line of cross hatch with the vertical sync signal as the reference is the pattern start position data. In addition, every how many line the line should be output with the pattern start position is the pattern interval data. The number of scanning lines varies with the frequency of signal input. Therefore, these start position data and interval data need to set the adequate data for every bank of convergence adjusted.

On the other hand, the vertical line is formed on the basis of the clock with 64 times frequency as the horizontal sync signal. Namely, since the pattern signal is formed on the basis of the point dividing the horizontal 1 line into 64, the pattern start position and interval don't vary greatly with the signal input.

(1) Coarse pattern

The pattern interval data and line start position data of horizontal line generation circuit and vertical line generation circuit are set for the coarse pattern so that 5 lines is output. (Refer to Fig. 4-6.)

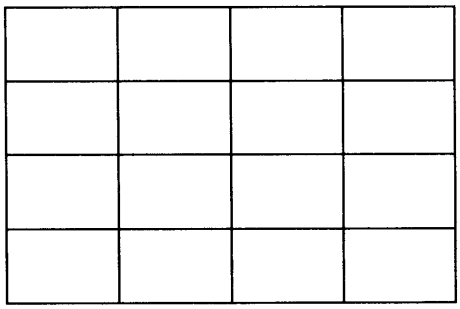


Fig. 4-6 Cross hatch coarse pattern

(2) Close pattern

The pattern interval data and line start position data of horizontal line generation circuit and vertical line generation circuit are set to the close pattern so that vertical 13 and horizontal 11 lines is output.

3-2-5. Cross Pattern

The cross pattern (Fig. 4-7) extracts the vertical and horizontal center portions from the coarse cross hatch pattern (Fig. 4-6). The extracted area is output from QM40. (Fig. 4-8). The cross pattern is formed by taking the logical AND of the area signal and the coarse cross hatch signal.

The difference between the cross pattern and the coarse cross hatch pattern is the difference of the area signal being ANDed. The cross hatch patter is obtained when the area signal is as shown in Fig. 4-9, and the cross pattern is obtained when the signal is as shown in Fig. 4-8.

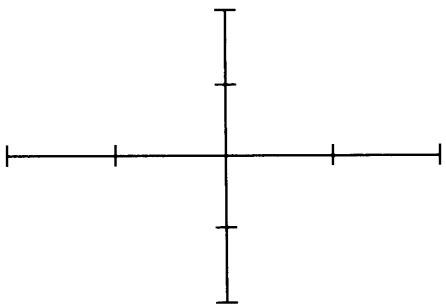


Fig. 4-7 Cross pattern

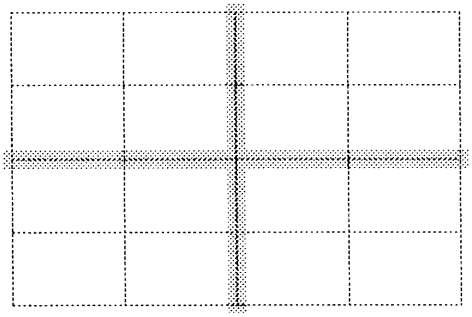


Fig. 4-8 Pattern extracting area (cross pattern)

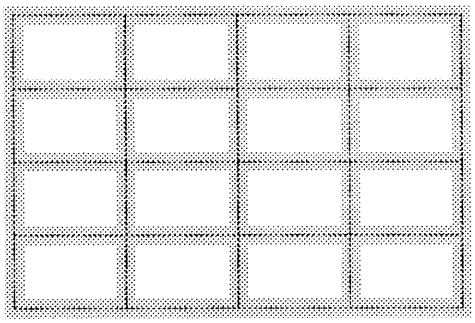


Fig. 4-9 Pattern extracting area (hatch pattern)

3-2-6. Marker Generation Circuit

This circuit forms the marker necessary when correcting the convergence. The marker indication locations are 25 points with 5 points in horizontal direction and 5 points in vertical direction. The marker is indicated at an optional location among these 25 points by giving the horizontal and vertical coordinates from the microprocessor. The marker frame forming circuit is the circuit to extract the 1st and 3rd lines respectively out of vertical and horizontal 3 lines prepared in the preceding items 3-2-2 and 3-2-3. The logical OR of 1st line and 3rd line is taken for each vertical and horizontal line. Further, the pattern as shown in Fig. 4-10 is formed by taking the logical OR of these vertical and horizontal signals.

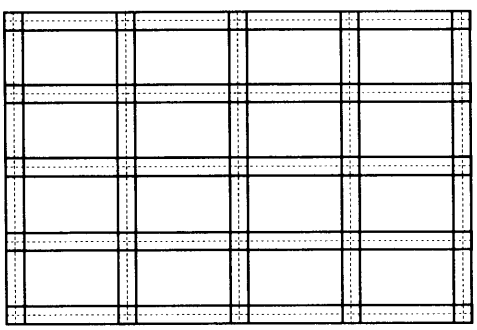


Fig. 4-10 Pattern for marker

Next, Fig. 4-11 shows the display area generation circuit. QM26 counts the number of vertical line position pulses generated in QM11. Similarly, QM27 counts the number of horizontal line position pulses generated in QM16. QM29 and QM30 compares the marker display data sent from the microprocessor and the count value of the position pulse. When the microprocessor data coincides with the position pulse data, QM38 develops "H" level. The signal becomes the marker indication enable area signal (Fig. 4-12), and the marker indicating position is decided (Fig. 4-13) by taking the logical AND of the value and the signal shown in Fig. 4-10. This is similarly applicable to the case of close cross hatch pattern.

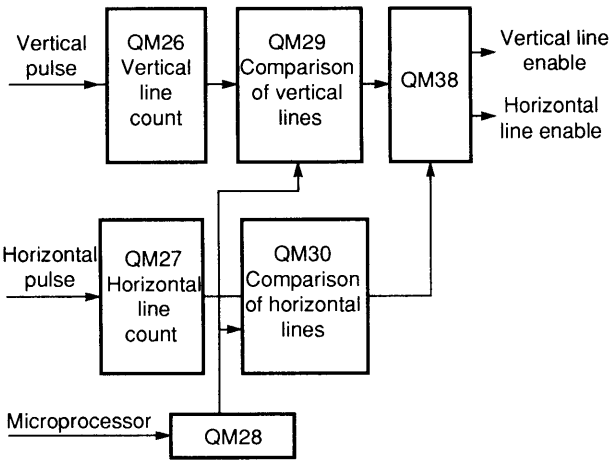


Fig. 4-11 Indication area preparing circuit

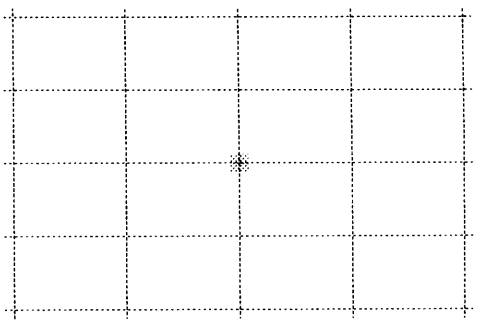


Fig. 4-12 Marker extracting area

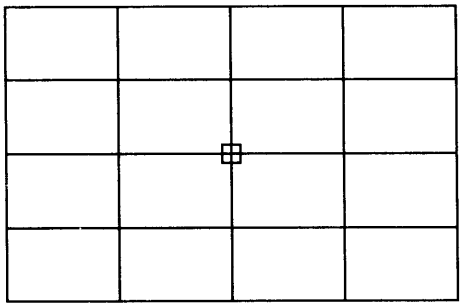


Fig. 4-13 Marker output state

3-2-7. H-character

The H-character uses the line for close cross hatch pattern. The 2nd and 3rd lines out of 3 lines/set of vertical line and the 2nd line out of 3 lines/set of horizontal line are assembled to form the H-character. (Refer to Fig. 4-14.)

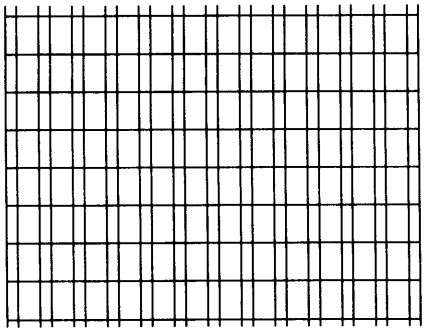


Fig. 4-14 Pattern for H-character pattern

Further, the output enable area of H-character is the area which the output signal from pin 6 of QM39 and the output signal from pin 6 of QM38 are assembled.
(Refer to Fig. 4-15.)

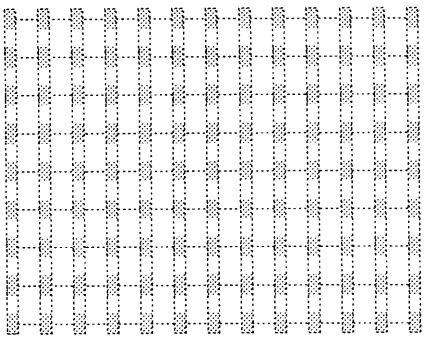


Fig. 4-15 H pattern extracting area

The H-pattern as shown in Fig. 4-16 is formed by taking the logical AND of the pattern shown in Figs. 4-14 and 4-15.

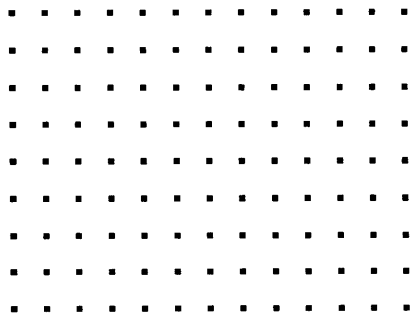


Fig. 4-16 H pattern

3-2-8. Dot Pattern

While the cross hatch pattern is formed by the logical OR of horizontal line and vertical line, the dot pattern is formed by the logical AND of them. (Refer to Fig. 4-17.)

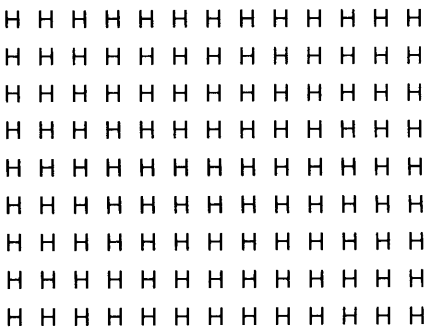


Fig. 4-17 Dot pattern

4. VARIOUS DATA

4-1. Internal Sync Signal Generator

The oscillation frequency, frequency division ratio and control data in each bank are shown in tables 4-1 and 4-2.

Table 4-1 Horizontal sync signal

Bank	Frequency	Frequency division ratio
Bank 1	17 kHz	210
Bank 2	24 kHz	149
Bank 3	31 kHz	115
Bank 4	37 kHz	97
Bank 5	50 kHz	72
Bank 6	70 kHz	51
Bank 7	90 kHz	40

Table 4-2 Vertical sync signal

Bank	Frequency	Vertical sync signal
Bank 1 – 7	60 kHz	59648 (fixed).

4-2. PLL Data

The set values of VCO oscillation frequency and pre-scaler in each bank are shown in table 4-3.

Table 4-3

Bank	Frequency	VCO frequency	Pre-scaller
Bank 1	17 kHz	34.4 MHz	1/16
Bank 2	24 kHz	24.6 MHz	1/8
Bank 3	31 kHz	31.7 MHz	1/8
Bank 4	37 kHz	37.9 MHz	1/8
Bank 5	50 kHz	25.6 MHz	1/4
Bank 6	70 kHz	35.8 MHz	1/4
Bank 7	90 kHz	46.8 MHz	1/4

4-3. Pattern Data

The vertical line/horizontal line start position data and line interval data in each bank are shown in table 4-4.

Table 4-4

Bank	Vertical line starting position	Vertical line interval	Horizontal line starting position	Horizontal line interval
Bank 1	8	12	10	62
Bank 2	8	12	13	90
Bank 3	8	12	16	116
Bank 4	9	12	20	136
Bank 5	9	12	26	186
Bank 6	11	12	36	258
Bank 7	12	12	44	329

SECTION V
VIDEO CIRCUIT

1. OUTLINE

Corresponding to each TV system of NTSC/PAL/SECAM/HDTV (YPbPr), the video circuit performs the signal switching and video color processing. Further, the NTSC system employs the NTSC up-converter circuit for converting the scanning frequency into the horizontal 33 kHz and vertical 120 Hz frequencies.

2. FLOW OF SIGNAL

Fig. 5-1 shows the block diagram of video circuit. In the NTSC/PAL system, the composite video signal is separated to the YC signal by the comb filter, switched with the external YC signal (Y/C and S-VIDEO input) by the input signal switching IC (Q521) and input to the video color IC (Q501).

Thereafter in the NTSC system, the YUV signal demodulated by the video color IC is converted into the YUV signal of horizontal 33.73 kHz and vertical 120 Hz frequencies by the up-converter circuit.

In addition, in the PAL/SECAM system, the signal is demodulated by the video color IC, SECAM demodulation IC (Q541) and 1H delay line IC (Q542) and finally converted into the RGB signal by the video color IC.

In the HDTV system on the other hand, the YPbPr signal input-selected by the RGB circuit is supplied to the NTSC/HD switching IC (Q2201) and switched with the NTSC signal (up-converter).

After the NTSC/HD switching, the signal is processed commonly in the NTSC and HDTV, the picture quality is corrected by the gamma correction circuit and contour correction circuit and input into the RGB processor IC (Q510).

The color and tint are adjusted in the RGB processor, then the signal is converted into the RGB signal, and switched over for its output with the RGB signal of the PAL/SECAM systems.

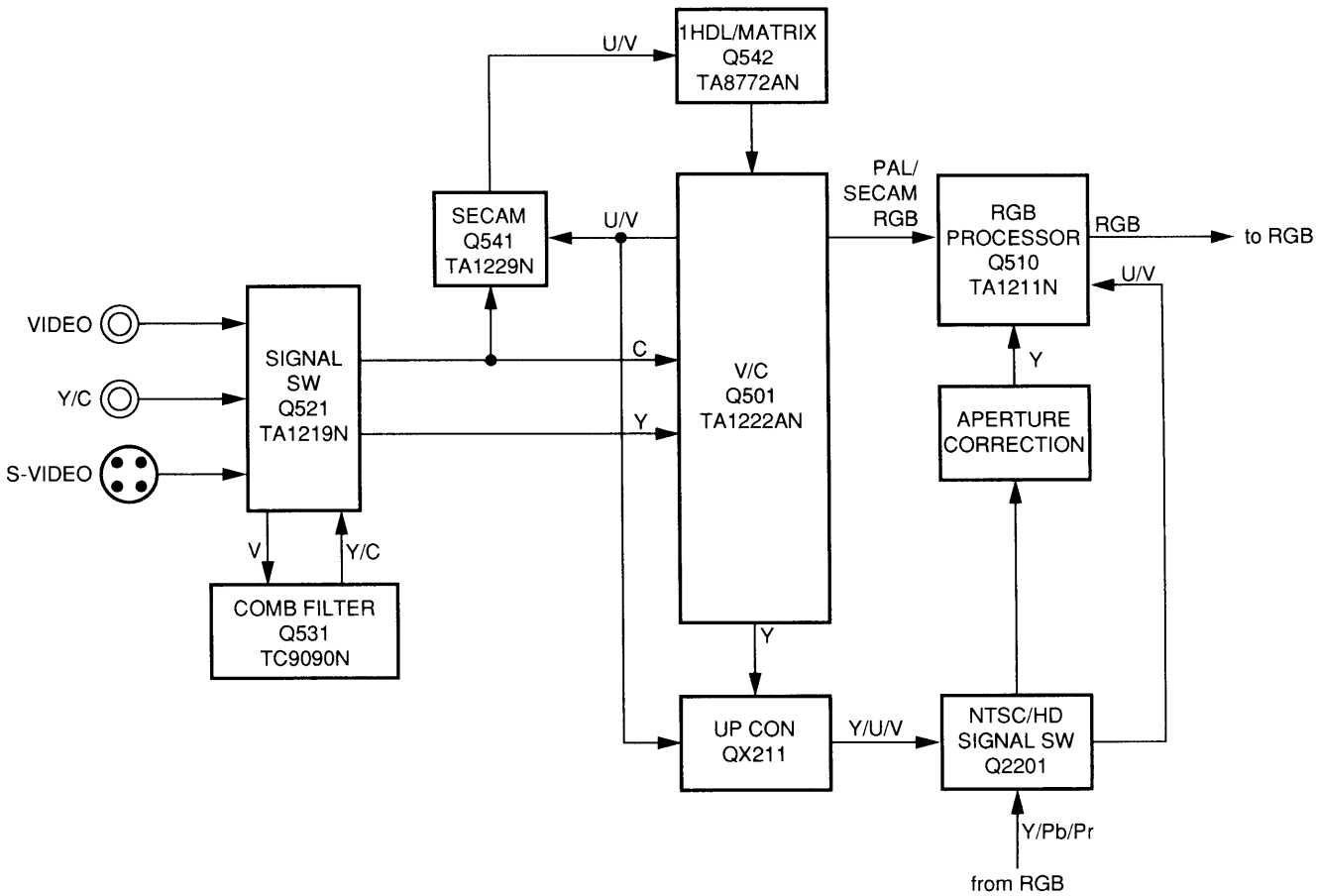


Fig. 5-1 Video circuit block diagram

3. SIGNAL SWITCHING CIRCUIT

3-1. Outline

In the signal switching circuit, the video signal from input terminal is selected and the signal is supplied to the video color circuit. The selection of signal is controlled via I^2C by the microprocessor.

3-1-1. Circuit Operation

(1) Composite video signal

The composite video signal from INPUT A is input to pin 8 of Q521, and switched as described below by the color system identification information from the V/C IC (Q501).

During B/W:

The composite signal is output to pins 32 (Y OUT) and 30 (C OUT) of Q521.

During PAL/NTSC:

The composite video signal is output to pin 34 of Q521, separated to the YC signal by the digital comb filter Q531, and then input to pins 26 (Y IN) and 28 (C IN), and output from pins 32 (Y OUT) and 30 (C OUT).

During SECAM/4.43NTSC:

The circuit operation during SECAM/4.43NTSC mode is identical to that during B/W. However, the I/O 2 output of pin 18 develops Hi level, and the trap circuit of pin 32 (Y OUT) line is turned on (and the others are turned off).

(2) YC Signal

The YC signal from the INPUT B (Y/C) is input to pins 14 and 16 of Q521, and the YC signal from the INPUT C (S-VIDEO) is input to pins 10 and 12 of Q521, and the YC signal selected to pins 32 (Y OUT) and 30 (C OUT) is output.

4. DIGITAL COMB FILTER

4-1. Features

The following features are obtained by applying three line digital comb filter IC (TC9090N) inside the circuit.

(1) Higher separation with less variations

(2) One line dot countermeasure circuit built-in

(3) No adjustment

(4) 4fsc PLL circuit built-in

(5) Vertical contour correction logic circuit built-in

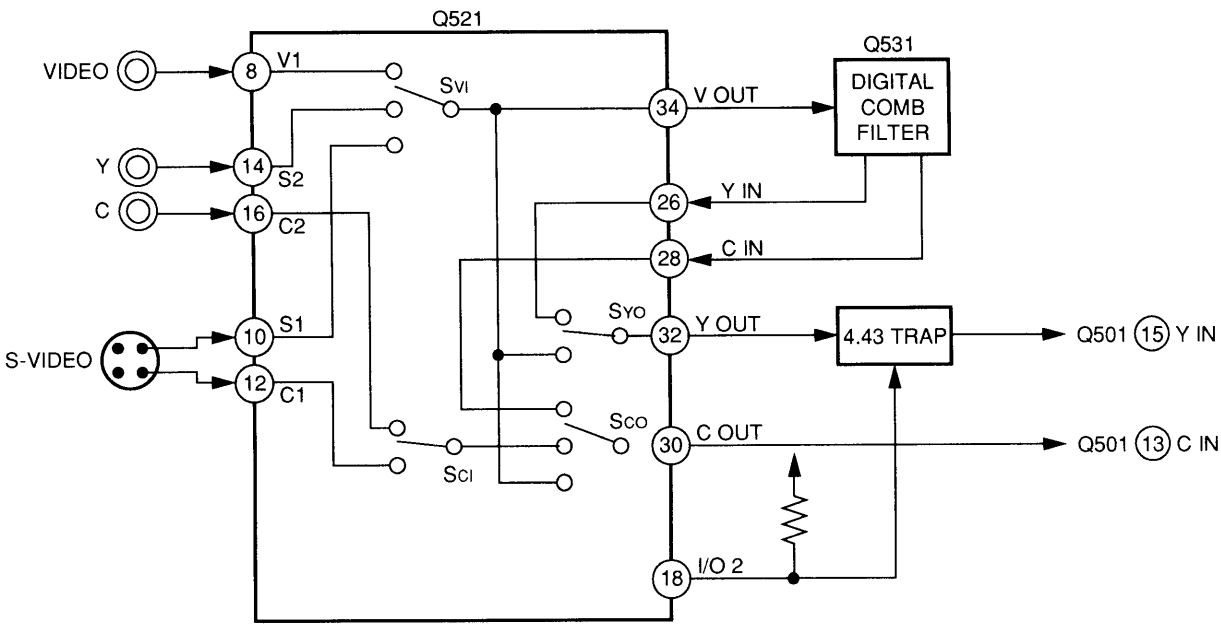


Fig. 5-2 Signal switching circuit block diagram

4-2. Circuit Operation

Description will be give by referring to a block diagram shown in Fig. 5-3.

(1) The composite video signal input from the signal switching circuit is limited in its band width by a LPF provided to remove aliasing noises and consisting of L5301, etc. and then enters pin 3 of Q531.

(2) On the other hand, fsc (3.58 MHz or 4.43 MHz) being oscillated in the video color IC (Q501) enters pin 19 of Q531 and converted into a 4fsc (14.3 MHz or 17.7 MHz, drive clock frequency) inside Q531.

(3) The video signal entered pin 3 of Q531 is converted into a digital signal by the built-in 8 bit A/D converter and then returned to an analog signal again by an 8 bit D/A converter after various operations are carried out inside the IC, thus providing the Y signal to pin 25 and color signal to pin 23.

(4) The Y signal output from pin 25 of Q531 passes through a LPF (L5307) which removes clock components, amplified by a 6 dB amplifier Q532, and outputs as the Y signal. Moreover, in this circuit, a vertical contour correction is carried out on the Y signal after the Y signal and the color signal are separated.

(5) At the same time, the color signal output at pin 23 of Q531 passes through a LPF (L5306) for removal of the clock signal components, amplified by twice in Q535 and outputs as a color signal in passing through a buffer Q536.

(6) Identified result for TV systems is controlled with I^2C bus data sent from the microcomputer.

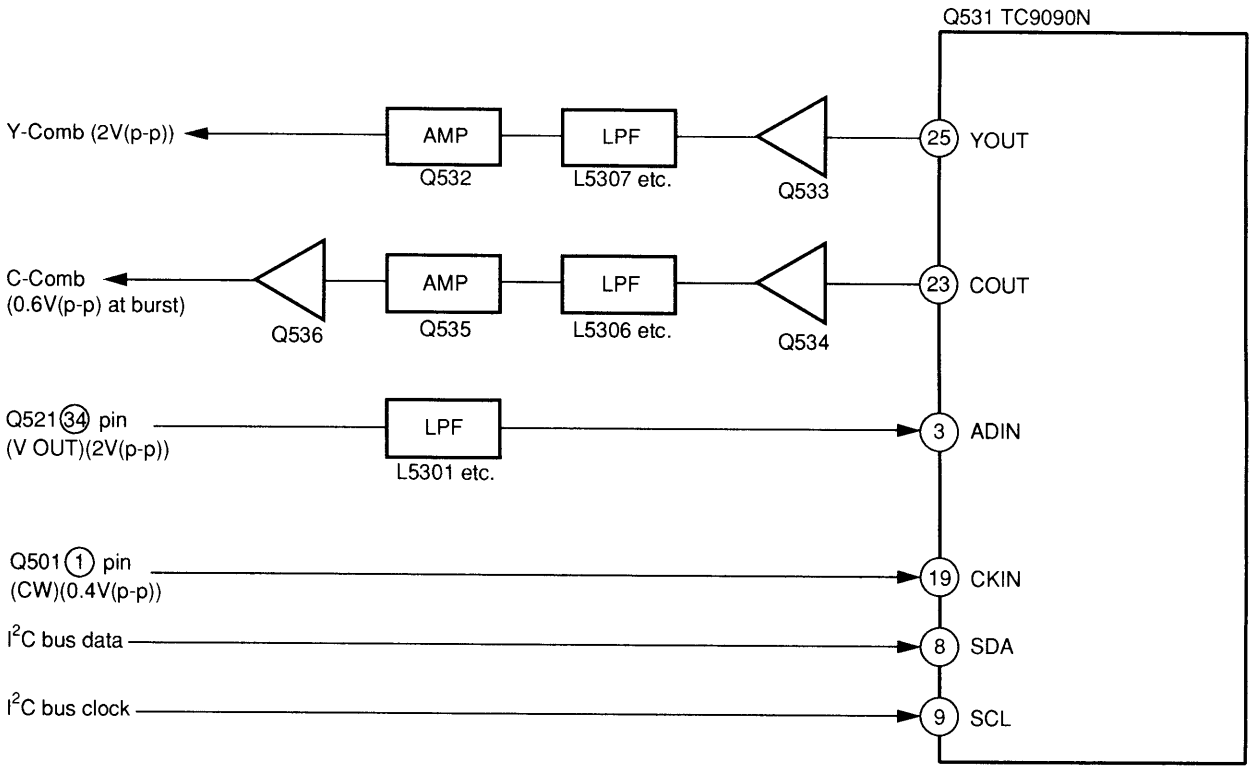


Fig. 5-3 Digital comb filter block diagram

4-3. Description of Q531 (TC9090N)

4-3-1. Pin Layout (TC9090N)

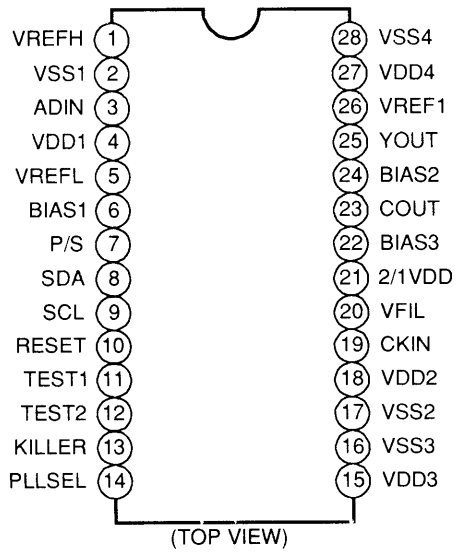


Fig. 5-4

4-3-2. Pin Function (TC9090N)

Table 5-1

Pin No.	Name	Function
1	VREFL	Bias for ADC
2	VSS1	GND for ADC
3	ADIN	Video input
4	VDD1	VDD for ADC
5	VREFH	Bias for ADC
6	BIAS1	Bias for ADC
7	P/S	Select function control
8	SCL	I²C bus clock input
9	SDA	I²C bus data input, Acknowledge output
10	RESET	I²C bus reset
11	TEST1	Test terminal
12	TEST2	Test terminal
13	KILLER	Clock killer switch
14	PLLSEL	Select input clock
15	VDD3	VDD for digital
16	VSS3	GND for analog
17	VSS2	GND for PLL
18	VDD2	VDD for PLL
19	CKIN	Clock input
20	VFIL	VCO filter
21	1/2 VDD	Bias for line memory
22	BIAS3	Bias for DAC
23	COUT	C output
24	BIAS2	Bias for DAC
25	YOUT	Y output
26	VREF1	Bias for DAC
27	VDD4	VDD for DAC
28	VSS4	GND for DAC

4-3-3. Block Diagram (TC9090N)

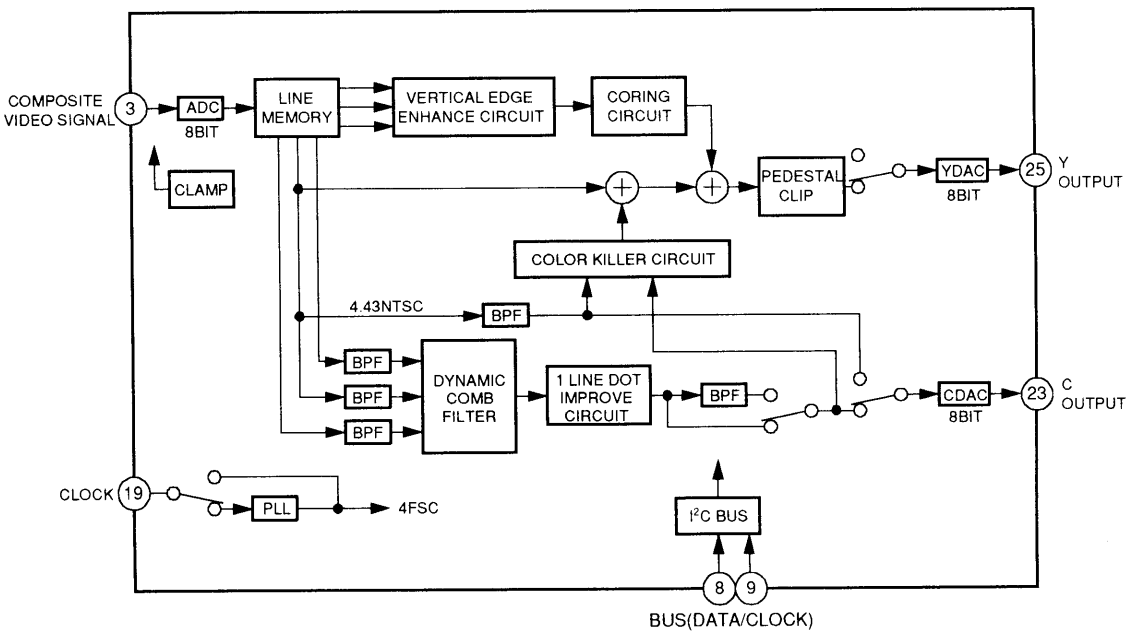


Fig. 5-5

5. PAL/SECAM PROCESSING CIRCUIT

5-1. Outline

The video color circuit of P7300U is composed of the following 3 kinds of IC corresponding to the multi color system

(1) TA1222AN (PAL/NTSC, VIDEO/COLOR/DEF process IC)

(2) TA1229N (SECAM demodulation IC)

(3) TA8772AN (Base band 1H delay IC)

For information the NTSC system uses only the color demodulation and synchronism separation out of the functions of TA1222AN.

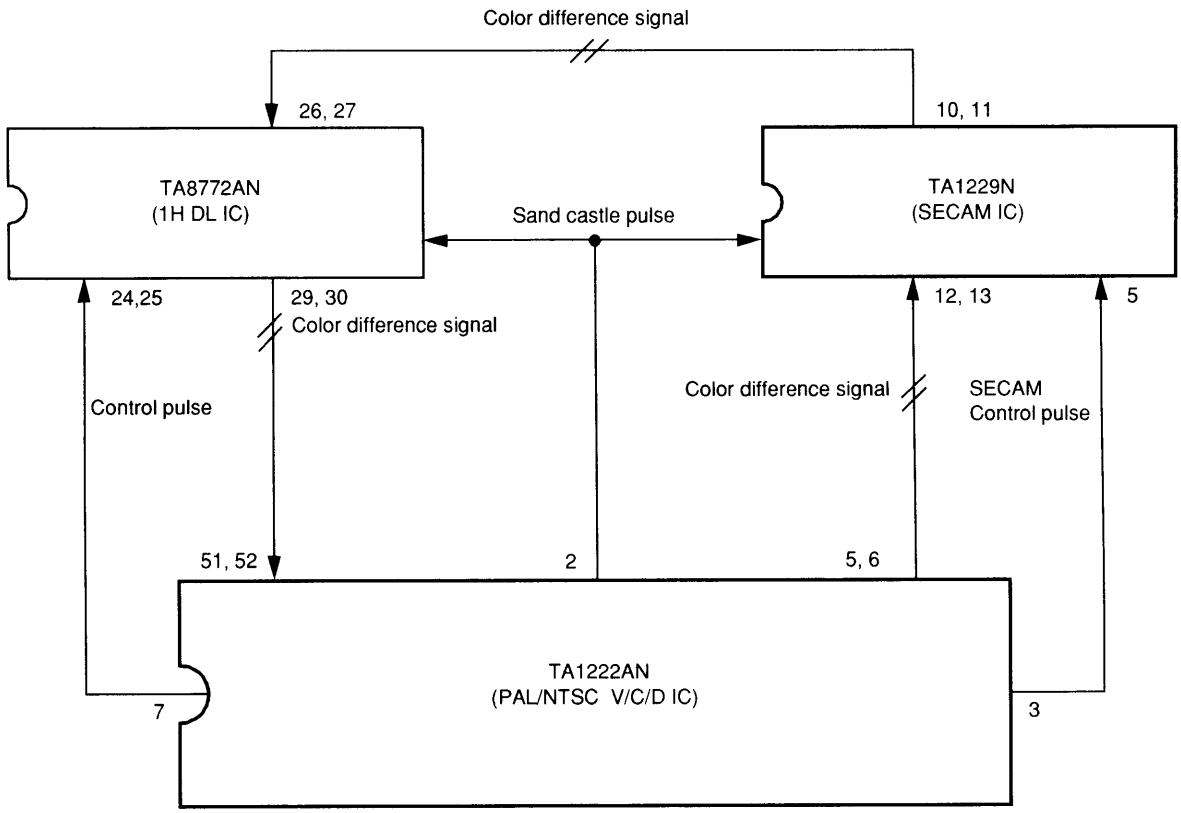


Fig. 5-6 Multi-color system

5-2. TA1222AN

5-2-1. Outline

This IC TA1222AN enables more precise picture setting than that of the conventional IC (TA8845AN) used in the projection TV by means of large scale employment of I^2C bus, and reduces many peripheral components by containing filters inside.

The main features (comparing TA8845AN) are as follows:

(1) Large scale employment of bus control of parameter for picture controls

- Soft method of picture making

Table 5-2

	Former TA8845AN	TA1222AN
Black expanding start point	External constant	Bus control
DC transmission correction quantity point	External constant	Bus control
Black level correction quantity	External constant	Bus control
Each ABCL characteristic	External constant	Bus control

(2) Employment of containing each video band filter inside

- Employment of automatic adjustment circuit by Fsc to absorb deviation
- Employment of deviation absorbing method by high S/N filter and mask trimming using fixed CR

Table 5-3

	Former TA8845N	TA1222AN
Y-DL	Apa-con DL inside	Inside
Color TOF/BPF	External	Inside
Velocity modulation processing circuit	External	Inside
Fsc trap for color demodulation output	External	Inside

(3) Employment of containing each filter (for S/H: Sample & Hold) inside

- Circuit operation by extremely low current
- Employment of leak current cancel circuit
- Employment of detection circuit which does not suffer from influence of stray capacity

Table 5-4

	Former TA8845N	TA1222AN
Color ACC/Killer filter	External	Inside
Y/Color difference clamp filter	External	Inside
Filter for filter automatic adjustment	External	Inside
AFC 2 filter	External	Inside

5-2-2. V/C/D Block Diagram (TA1222AN)

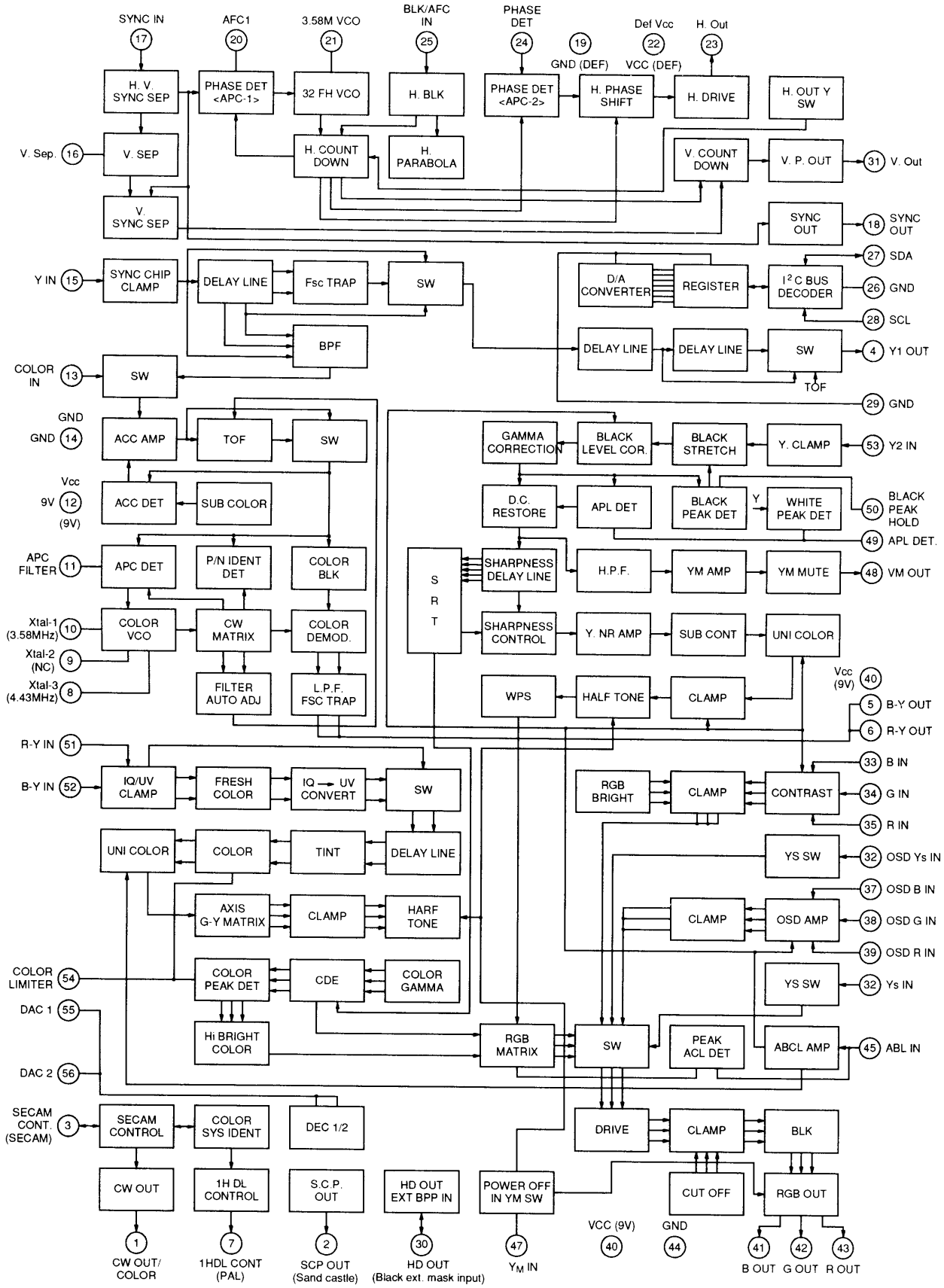


Fig. 5-7

5-2-3. Pin Function

The main terminals are explained hereunder.

Table 5-5

Pin No.	Name	Function
1	CW output	The CW (3.58/4.43 MHz) sync with the burst is output. The output is used as the clock for digital comb filter.
2	SCP	Signal where the burst gate and blanking pulses are imposed. The signal is used as the timing pulse of SECAN IC (TA1229N) and 1HDL IC (TA8772AN).
3	SECAM	Outputs the SECAM IC (TA1229N) controlling voltage. (Lo level during the SECAM and Hi during the other cases).
4	Y1 OUT	Outputs the luminance signal input from pin 15 through the delay line.
5	B – Y OUT	Outputs the color demodulated B-Y signal.
6	R – Y OUT	Outputs the color demodulated R-Y signal.
7	1HDL CONT	Outputs the 1HDL IC (TA8772AN) controlling voltage (PAL: 9 V, SECAM: 4.5V, NTSC: 0 V).
8	Xtal-3	Oscillation crystal terminal for 4.43 MHz.
10	Xtal-1	Oscillation crystal terminal for 3.58 MHz.
11	APC FILTER	Phase detection (and oscillation frequency control) terminal for color sync.
13	COLOR IN	Color signal input terminal.
15	Y IN	Luminance signal input terminal.
18	SYNC OUT	The sync signal sync-separated is output.
41	B OUT	B output terminal.
42	G OUT	G output terminal.
43	R OUT	R output terminal.
49	APL DET	Detects the black area of video signal to correct the direct current transmission.
51	R – Y IN	R-Y signal from the 1HDL IC (TA8772AN) is input.
52	B – Y IN	B-Y signal from the 1HDL IC (TA8772AN) is input.
53	Y2 IN	Luminance signal from Y1 OUT is input.
54	COLOR LIMITER	Peak-hold terminal of color limiter.
55	DAC 1	Test point (P501) terminal. This outputs the waveform during the service mode.

5-3. TA1229N

Fig. 5-9 shows a block diagram of TA1229N and its pin layout.

5-3-1. Bell Filter

As stated previously, HF pre-emphasis is applied to the carrier color signal in the SECAM system. This is to obtain compatibility with black/white TVs, and has an effect to reduce screen interference caused by the carrier color signal mixed in the Y signal during low tint color reproduction.

The pre-emphasis is called an inverted bell filter because of its form of characteristic curve. On the other hand, the filter used for de-emphasis is called a bell filter. F_O is adjusted to 4.286 MHz by adjusting bus data (BELL FIL) (In practice, oscilloscope waveform is adjusted while receiving a signal.)

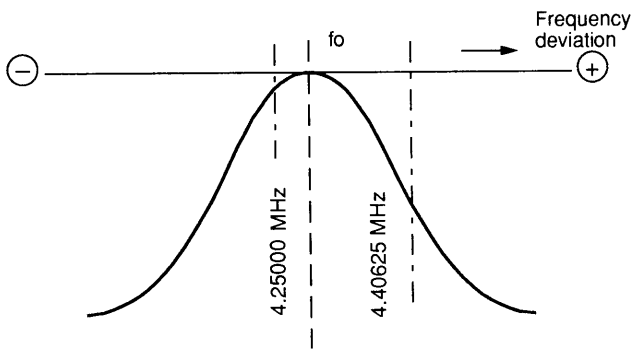
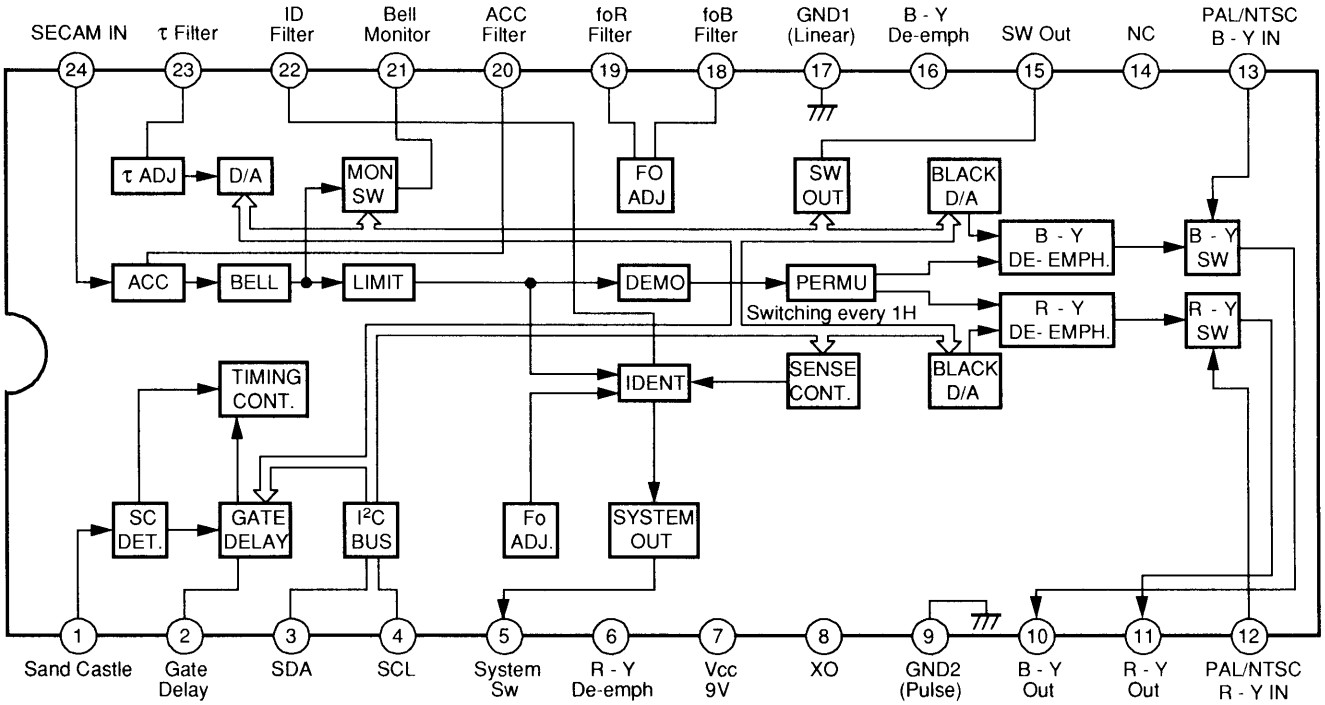


Fig. 5-8 Bell filter characteristic



Develops R - Y, B - Y by switching every 1H with PERMU.

Fig. 5-9 Pin layout of TA1229N

Table 5-6 Pin function

Pin No.	Function	Pin No.	Function
1	SCP in	13	PN B – Y in
2	Gate delay	14	Not used
3	SDA	15	SW out
4	SCL	16	B – Y de-emphasis
5	SYSTEM SW	17	LINEAR GND
6	R – Y de-emphasis	18	F_O B FILTER
7	V_{CC}	19	F_O R FILTER
8	XO	20	ACC FILTER
9	PULSE END	21	BELL MONITOR
10	B – Y out	22	ID FILTER
11	R – Y out	23	γ FILTER
12	PN R – Y in	24	COLOR in

5-4. TA8772AN

Fig. 5-10 shows a block diagram and pin layout of the TA8772N.

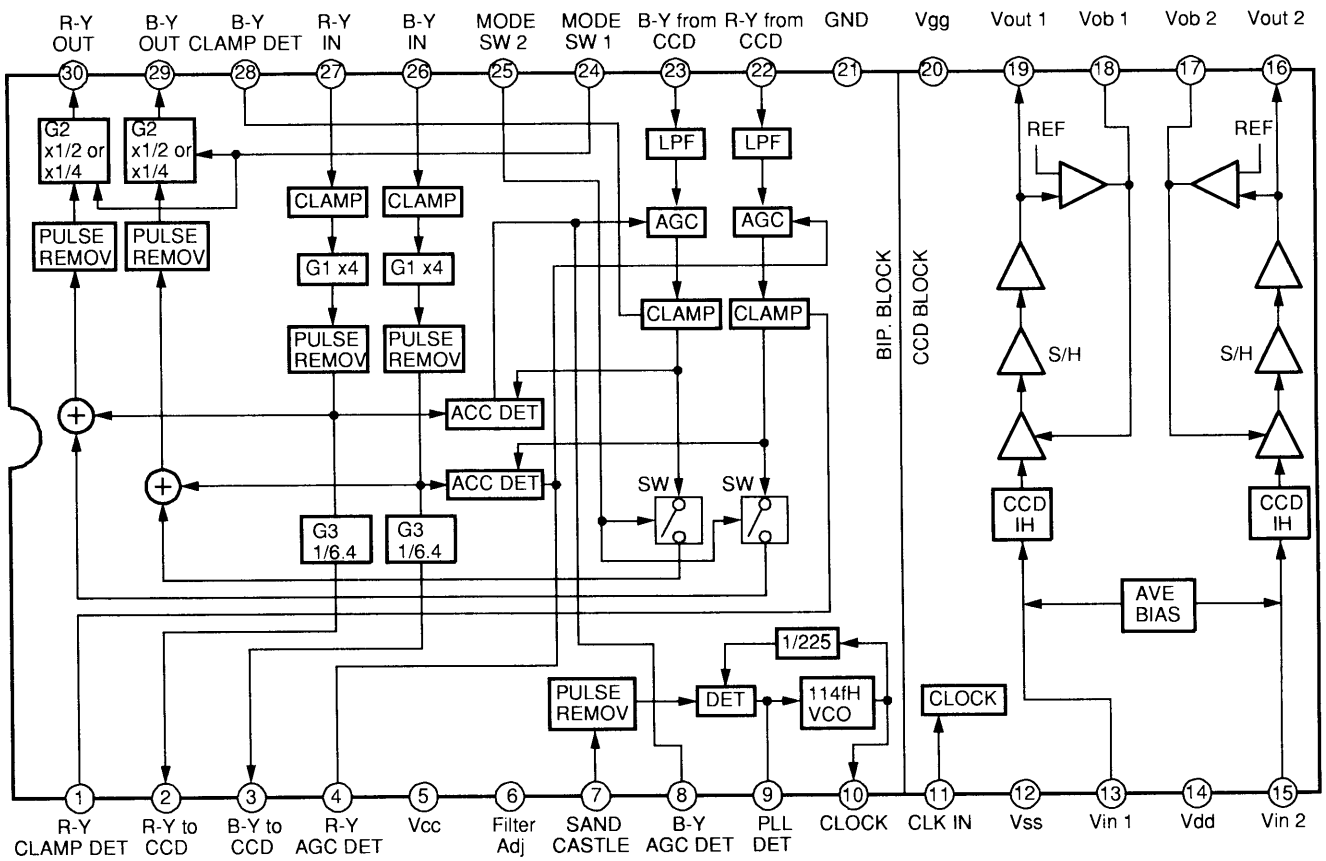


Fig. 5-10 Pin layout of TA8772AN

Table 5-7 Pin function

Pin No.	Function	Pin No.	Function
1	R – Y CLAMP DET	16	Vout 2
2	R – Y to CCD	17	Vob 2
3	B – Y to CCD	18	Vob 1
4	R – Y AGC DET	19	Vout 1
5	VCC	20	Vgg
6	Filter adj.	21	GND
7	SAND CASTLE	22	R – Y from CCD
8	B – Y AGC DET	23	B – Y from CCD
9	PLL DET	24	MODE SW 1
10	CLOCK	25	MODE SW 2
11	CLK IN	26	B – Y IN
12	V_{SS}	27	R – Y IN
13	Vin 1	28	B – Y CLAMP DET
14	V_{DD}	29	B – Y OUT
15	Vin 2	30	R – Y OUT

5-4-1. Control Pulse Signals

TA8772AN is a base band 1H delay line and delays a color signal by 1H after the demodulation by using CCDs. In this case, the delaying operation is carried out by each matrix for NTSC, PAL and SECAM with control pulse signals from the TA1222AN.

- NTSC: Through mode
- PAL: PAL matrix
- SECAM: SECAM matrix

5-5. Color Circuit

5-5-1. Demodulation Circuit Operation in PAL Signal Reception

Fig. 5-11 shows a block diagram when the demodulation circuit operates while receiving a PAL signal. The color signal input is demodulated to R – Y and B – Y signals through the demodulation circuit inside Q501. After demodulation, the signals are input to Q542 (1H DL), added to a delay signal and then input to Q501 again. The matrix circuit inside Q501 converts these signals to RGB signals and they are output to RGB circuit.

5-5-2. Demodulation Circuit Operation in SECAM Signal Reception

Fig. 5-12 shows a block diagram when the demodulation circuit operates while receiving a SECAM signal. The color signal output from the signal switching circuit (Q521) enters Q541 at first.

Inside Q541, the demodulated signal processed through the bell filter is switched by every 1H period by SECAM switch circuit and output as R – Y and B – Y signals. In this status, waveforms for these signals are observed by every 1H period.

The signals are input to Q542 (1H DL), added to a delay signal, output as color difference signals, and then input to Q501 again.

5-5-3. Demodulation Circuit Operation in NTSC Signal Reception

When the NTSC signal is received, the signal flow is entirely the same as that of PAL signal reception. (Fig. 5-11)

However, R – Y/B – Y signal passes through 1H-DL and is input to RGB MATRIX.

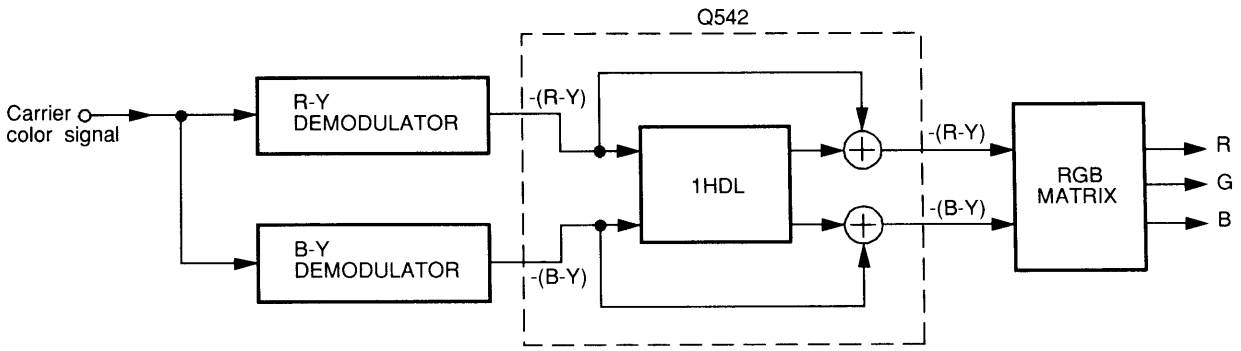


Fig. 5-11 Color signal demodulation in PAL signal reception

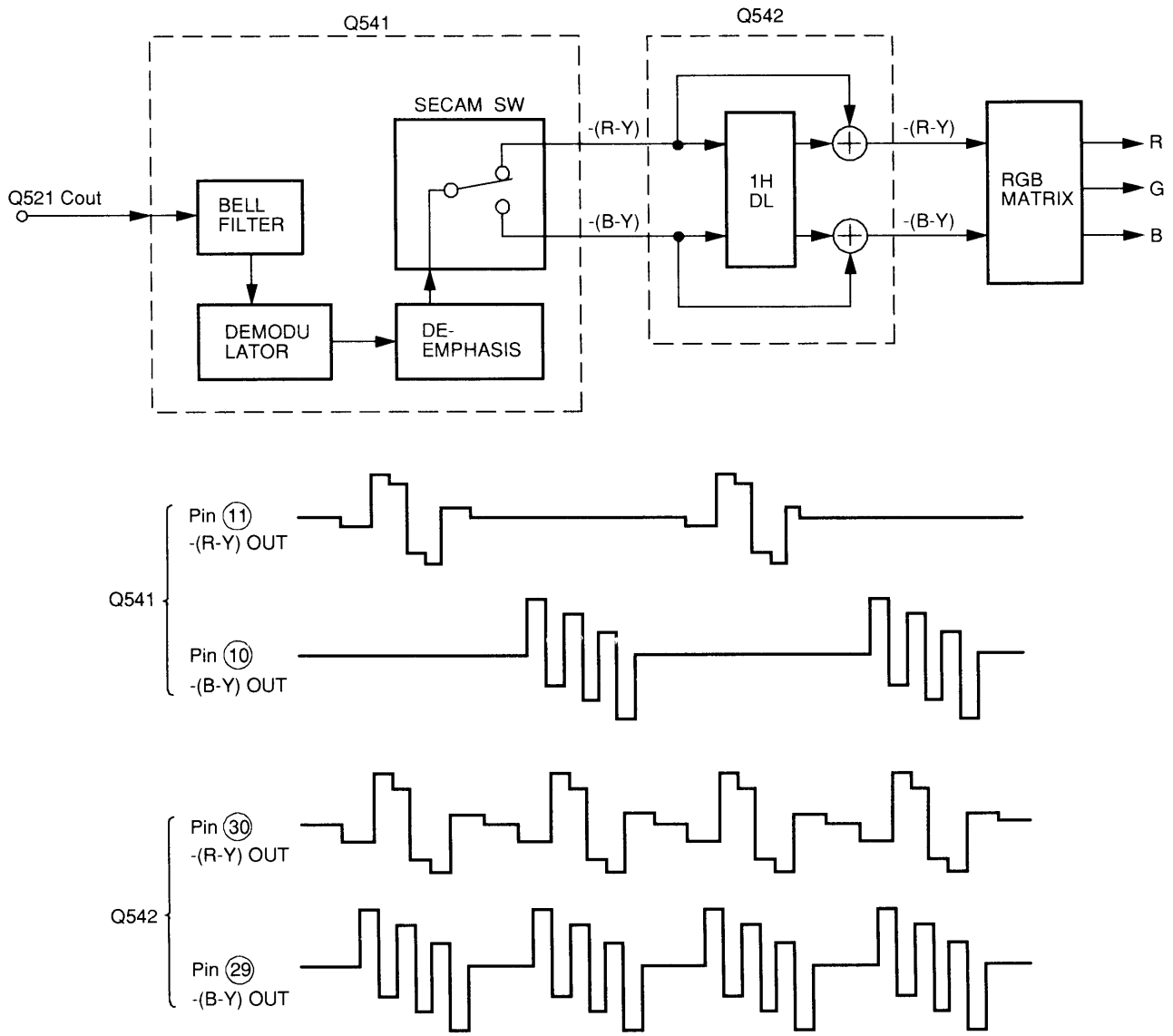


Fig. 5-12

5-6. Color Trap Circuit

A color trap circuit (3.58 MHz/4.43 MHz) is built-in on TA1222AN (Q501).

Signal system identification and S composite identification (bus control from the microprocessor) are carried out inside the circuit and one of 3.58/4.43/through is selected. (Fig. 5-13)

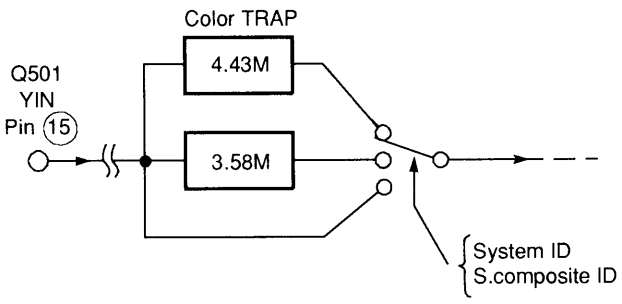


Fig. 5-13 Color trap circuit

5-7. Y-DL and Aperture Control Circuit

Y-DL circuit in Q501 has 2 variable steps by using 1DLs.
These steps are set by a bus data.

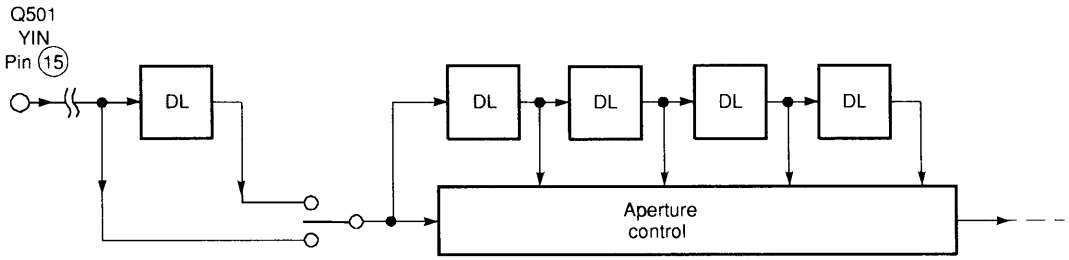


Fig. 5-14 Y-DL aperture control circuit

6. UP-CONVERTER CIRCUIT

6-1. Outline

For reducing the large picture flicker, P7300U employs the "up-converter circuit" to convert the horizontal scanning frequency of NTSC into 33.75 kHz identical to the HDTV and to convert the vertical scanning frequency into 120 Hz which is twice.

6-2. Operation Principle

The horizontal scanning frequency is converted into 33.75 kHz identical to the HDTV, while the vertical scanning frequency is converted into 120 Hz which is twice the NTSC.

For this purpose, the image signal of 1 field is scanned twice on the same scanning line, and moreover the total of scanning lines of 4 fields is compressed to 1125 lines.

Concretely, the scanning lines are time compressed by inputting the NTSC signal into the field memory and making the ratio of input clock frequency and output clock frequency to be 1125/525 (= 15/7). Further, the roundness is maintained by extending the amplitude at the ratio of 562.5/525 in the vertical direction.

6-3. Circuit Operation

6-3-1. Circuit Construction

This up-converter circuit is composed of the following 8 chips (Refer to Table 5-8.) and peripheral circuits (LPF, MPX, CLAMP, etc.) as shown in Fig. 5-15.

Table 5-8

QX211	Up-convert G/A (TC160G16AF-30)
QX212, QX213	2M memory (MSM518221-30)
QX106, QX114	A/D converter (TLC55101)
QX201, QX207	Input/output PLL (TA8667F)
QX301	D/A converter (MB40978)

6-3-2. Actual Circuit Operation

Concerning the image signal:

(1) The Y signal input from pin 4 of Q501 (V/C/D IC) is converted into the digital signal with the A/D converter QX106, then input into the G/A QX211 via the memory QX212.

(2) Similarly, the U and V signals are multiplexed in analog, then A/D converted by QX114 and input to QX211 via the memory QX213.

(3) The Y, U and V signals input to QX211 simply add the sync signals at an optional level and are delay-adjusted, then output, converted into the analog signal with the D/A converter QX301, and then output to the NTSC/HDTV switching circuit.

Further, concerning the sync signal:

(4) The HD pulse of 15.75 kHz is converted into 33.75 kHz at the ratio of input/output clock frequencies, and output to the horizontal deflection circuit.

(5) The VD pulse of 60 Hz is converted into 120 Hz with 60 - 120 conversion block inside QX211, and output to the vertical deflection circuit.

(6) Further, the up-converter circuit generates and outputs the timing pulse (clamp, black peak mask) used at the RGB processor IC (Q510).

(7) These timings or the delay adjustment, etc. of (3) are controlled by the I^2C Bus.

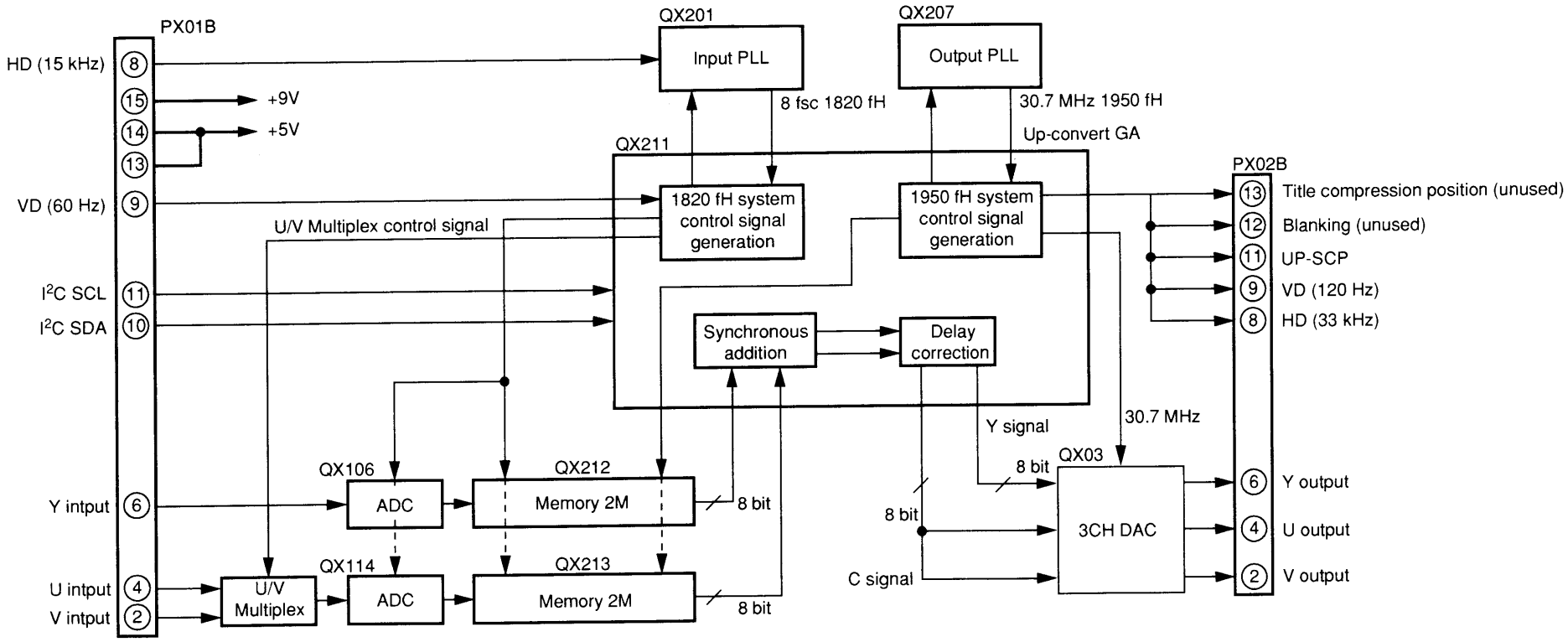


Fig. 5-15 P7300U NTSC up-converter block diagram

6-4. Input/Output Interface

Table 5-9 Input (PX01B)

Pin No.	Name	Level
1	GND	
2	V in	0.7V(p-p)
3	GND	
4	U in	0.7V(p-p)
5	GND	
6	Y in	0.7V(p-p)
7	GND	
8	HD in	5V, 15.75 kHz
9	VD in	5V, 60 Hz
10	SDA	5V
11	SCL	5V
12	GND	
13	+5V	
14	+5V	
15	+9V	

Table 5-10 Output (PX02B)

Pin No.	Name	Level
1	GND	
2	V out	0.7V(p-p)
3	GND	
4	U out	0.7V(p-p)
5	GND	
6	Y out	0.7V(p-p)
7	GND	
8	RHD	5V, 33.75 kHz
9	RVD	5V, 120 Hz
10	GND	
11	SCP	CLAMP = 5V, MASK = 2.5V
12	BLK	V. BLK, 5V (Not used)
13	JIMAKU	On-screen character compression timing, 5V (Not used)

6-5. Description of Main ICs.

The pin layout and functions of QX211 up-convert gate array (TC160G16AF-1130) are described in Fig. 5-16 and table 5-11.

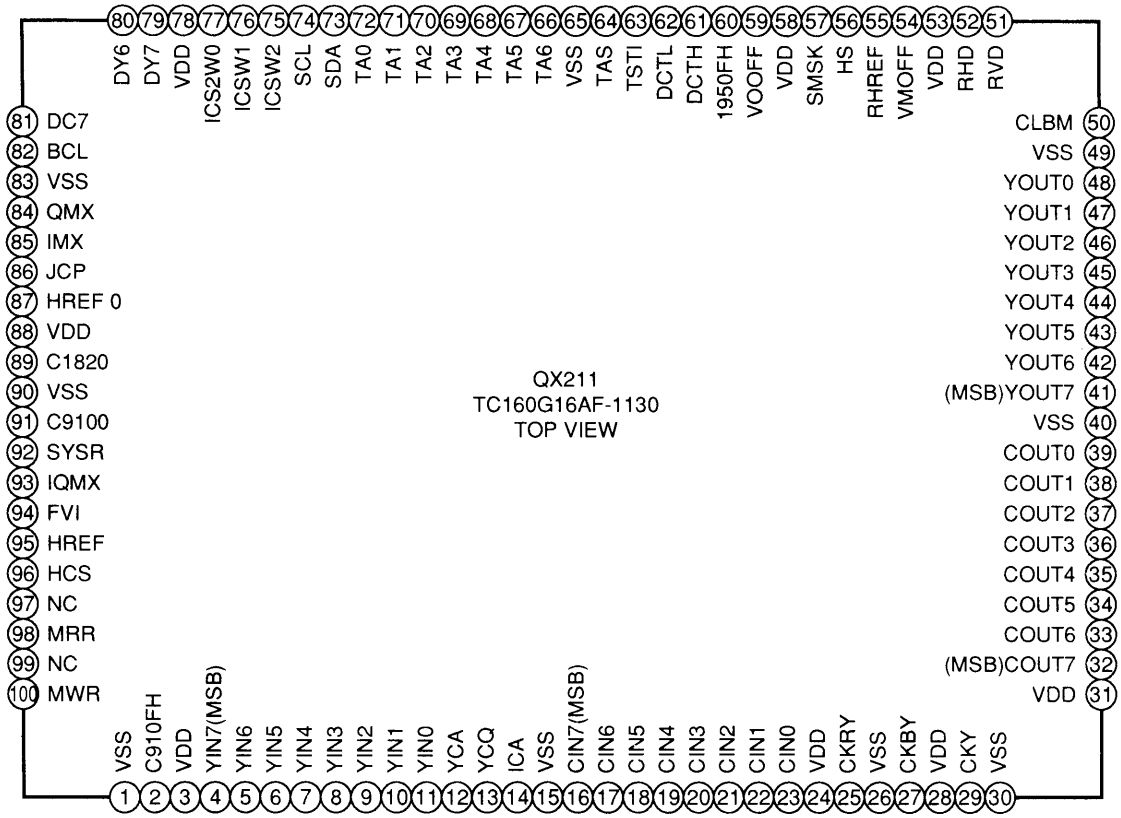


Fig. 5-16 Pin layout

Table 5-11 UPC gate array (TC160G16AF-1130) pin function (1/2)

Pin No.	Name	I/O	Used PAD	Function
1	VSS			
2	C910FH	I	TLCHT	910 fH clock input
3	VDD			
4	YIN7	I	TLCHT	Digital Y signal input (MSB)
5	YIN6	I	TLCHT	Digital Y signal input
6	YIN5	I	TLCHT	Digital Y signal input
7	YIN4	I	TLCHT	Digital Y signal input
8	YIN3	I	TLCHT	Digital Y signal input
9	YIN2	I	TLCHT	Digital Y signal input
10	YIN1	I	TLCHT	Digital Y signal input
11	YIN0	I	TLCHT	Digital Y signal input (LSB)
12	YCA	O	BT4	Y signal clamp controlling signal
13	QCA	O	BT4	Q signal clamp controlling signal
14	ICA	O	BT4	I signal clamp controlling signal
15	VSS			
16	CIN7	I	TLCHT	Digital C signal input (MSB)
17	CIN6	I	TLCHT	Digital C signal input
18	CIN5	I	TLCHT	Digital C signal input
19	CIN4	I	TLCHT	Digital C signal input
20	CIN3	I	TLCHT	Digital C signal input
21	CIN2	I	TLCHT	Digital C signal input
22	CIN1	I	TLCHT	Digital C signal input
23	CIN0	I	TLCHT	Digital C signal input (LSB)
24	VDD			
25	CKI	O	B4	Clock output for I signal D/A
26	VSS			
27	CKQ	O	B4	Clock output for Q signal D/A
28	VDD			
29	CKY	O	B4	Clock output for Y signal D/A
30	VSS			
31	VDD			
32	COUT7	O	B4	Digital C signal output (MSB)
33	COUT6	O	B4	Digital C signal output
34	COUT5	O	B4	Digital C signal output
35	COUT4	O	B4	Digital C signal output
36	COUT3	O	B4	Digital C signal output
37	COUT2	O	B4	Digital C signal output
38	COUT1	O	B4	Digital C signal output
39	COUT0	O	B4	Digital C signal output (LSB)
40	VSS			
41	YOUT7	O	B4	Digital Y signal output (MSB)
42	YOUT6	O	B4	Digital Y signal output
43	YOUT5	O	B4	Digital Y signal output
44	YOUT4	O	B4	Digital Y signal output
45	YOUT3	O	B4	Digital Y signal output
46	YOUT2	O	B4	Digital Y signal output
47	YOUT1	O	B4	Digital Y signal output
48	YOUT0	O	B4	Digital Y signal output (LSB)
49	VSS			
50	CLBM	O	BT4	Black peak detection mask/clamp signal

Table 5-11 UPC gate array (TC160G16AF-1130) pin function (2/2)

Pin No.	Name	I/O	Used PAD	Function
51	RVD	O	B4	Vertical drive signal
52	RHD	O	B4	Horizontal drive signal
53	VDD			
54	VMOFF	O	B4	Timing signal for speed modulation OFF
55	RHREF	O	B4	H reference for 1950 fH horizontal AFC
56	HS	O	B4	H sync for 1950 fH horizontal AFC
57	SMSK	O	B4	Phase comparison switch signal for 1950 fH horizontal AFC
58	VDD			
59	VOOFF	O	B4	Reference voltage source switch signal for 1950 fH horizontal AFC
60	1950 fH	I	TLCHT	1950 fH clock input
61	DCTTH	I	IBUF	DC test (Usual GND)
62	DCTTL	I	IBUF	DC test (Usual GND)
63	TSTI	I	IBUF	I^2C bus test (Usual VDD)
64	TAS	I	IBUF	Test control (Usual VDD)
65	VSS			
66	TA6	I	IBUF	I^2C bus main address (MSB)
67	TA5	I	IBUF	I^2C bus main address
68	TA4	I	IBUF	I^2C bus main address
69	TA3	I	IBUF	I^2C bus main address
70	TA2	I	IBUF	I^2C bus main address
71	TA1	I	IBUF	I^2C bus main address
72	TA0	I	IBUF	I^2C bus main address (LSB)
73	SDA	I/O	BD4SC	I^2C bus data input
74	SCL	I	SCHMITC	I^2C bus clock input
75	ICSW2	O	B4	I^2C control signal output
76	ICSW1	O	B4	I^2C control signal output
77	ICSW0	O	B4	I^2C control signal output
78	VDD			
79	DY7	I	TLCHT	A/D output Y signal MSB
80	DY6	I	TLCHT	A/D output Y signal 2'nd
81	DC7	I	TLCHT	A/D output C signal MSB
82	BCL	O	B4	A/D front clamp pulse
83	VSS			
84	QMX	O	B4	Q multiplex timing output
85	IMX	O	B4	I multiplex timing output
86	JCP	O	B4	Title compression position
87	HREFO	O	B4	Horizontal reference output for 1820 fH
88	VDD			
89	C1820	I	TLCHT	1820 fH clock input
90	VSS			
91	C9100	O	B4	910 fH clock output
92	SYSR	I	IBUF	System reset
93	IQMX	I	IBUF	IQ multiplex input
94	FVI	I	IBUF	Vertical sync input
95	HREF	I	IBUF	Horizontal sync input
96	HCS	I	TLCHT	Composite sync signal input
97	NC			
98	MRR	O	B4	Field memory read reset
99	NC			
100	MWR	O	B4	Field memory write reset

Used PADs:		
	IBUF	: CMOS input buffer
	TLCHT	: TTL input buffer
	SCHMITC	: CMOS schmitt input buffer
	B4	: Output buffer (4 mA)
	BT4	: 3-state output buffer (4 mA)
	BD4SC	: CMOS schmitt input/output (4 mA) two-way buffer

7. NTSC/HDTV PROCESSING CIRCUIT

7-1. NTSC/HDTV Video Switching Circuit

This circuit is composed of 2-input/1-output switch IC M52055P (Q2201) of 3 systems, and the control logic is as listed in table 5-13. This circuit controls pins 2, 7 and 12 of Q2201 via the DA converter Q2103 corresponding to I^2C bus by the microprocessor and selects the output signal.

Table 5-13

	Control voltage (pins 2, 7, 12)	Selection signal		
		Y (pin 3)	Pb/V (pin 5)	Pr/U (pin 6)
NTSC	H	pin 1	pin 14	pin 9
HDTV	L	pin 16	pin 11	pin 8

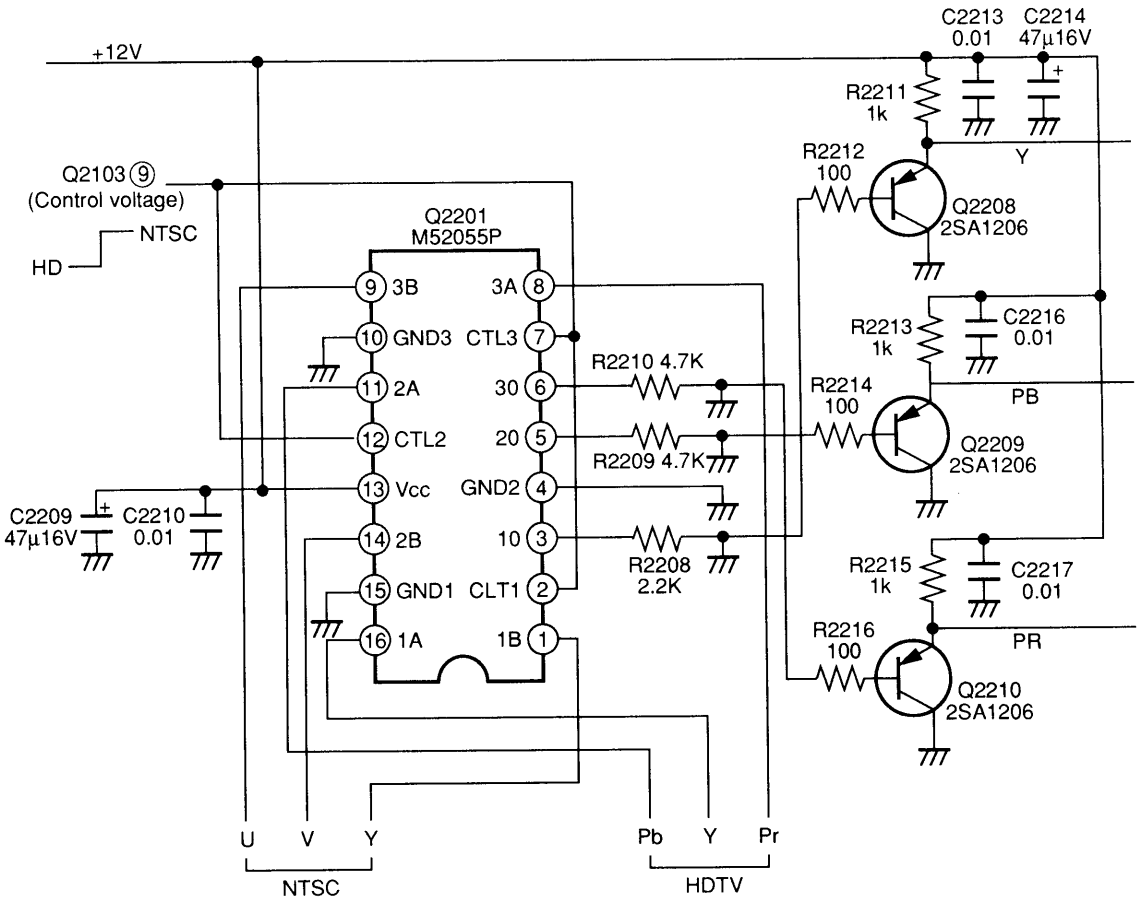


Fig. 5-17 NTSC/HDTV switching circuit

7-2. Picture Quality Correction Circuit

7-2-1. Gamma Correction Circuit

The output (Y) of NTSC/HD switching circuit, is impedance-converted by Q2208, and clamped by Q2225, Q2226 and Q2227. The clamp voltage Vclp is determined by R2265 and R2264, which is approx. 8V.

Next, the voltage is amplified by Q2228 and Q2229. In Q2229 collector, the high signal level components against the direct current voltage determined by R2270, R2271 and R2500 is compressed by the ON resistance of D2201. Namely, the circuit performs in non-linear operation by the direct current level of input signal.

Similarly, the circuit performs the non-linear operation also by D2123, R2286 and R2289, but rarely operates because the operation point is set to the level higher than 100 IRE.

Q2234 is controlled by pin 3 of Q510 and usually turned on, but doesn't perform the gamma correction operation because it is turned off during the sub contrast adjustment and the gamma correction point goes up to the power supply.

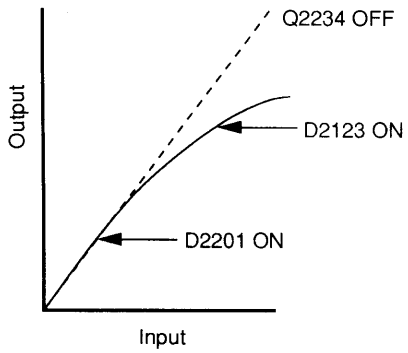


Fig. 5-18

7-2-2. Contour Correction Circuit

The signal input into the delay line (Z202) appears to the output terminal (B point) in delay (τ signal) by the delay time t (33nS). Further, the output end signal is reflected and appears in delay τ to the input terminal (A point), and is added with the input signal (0τ).

The signal of A-point is impedance-converted by Q2214, and the signal inverted and amplified the signal and B-point signal with Q2215 is added by the VR R2250 and is taken out at C-point as the secondary differential signal. At this time, R2250 is adjusted to obtain that the low band signal at C-point develops zero. The secondary differential signal has its peak at the 15 MHz.

The secondary differential signal is further inverted and amplified by Q2216, impedance-converted by Q2218 and added with the τ signal by R2236 and R2237.

Further by another delay line (Z203), the secondary differential signal (8 MHz peak) is similarly extracted to the emitter of Q2223 , and input to pin 30 (picture quality input terminal). In Q510, the signal is added with the τ signal input by pin 41. The amount to be added varies owing to the picture quality control.

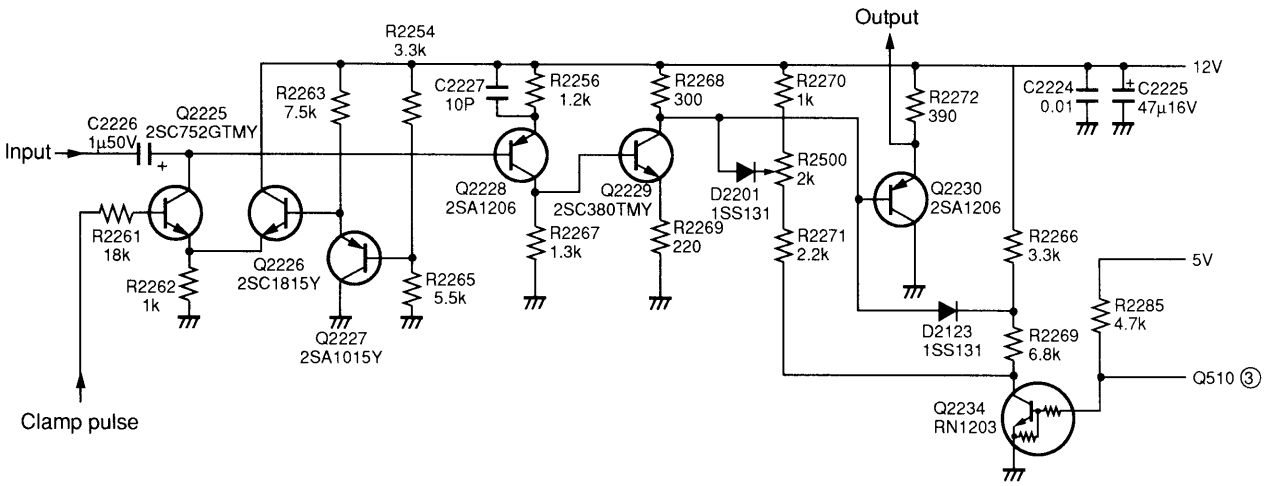


Fig. 5-19

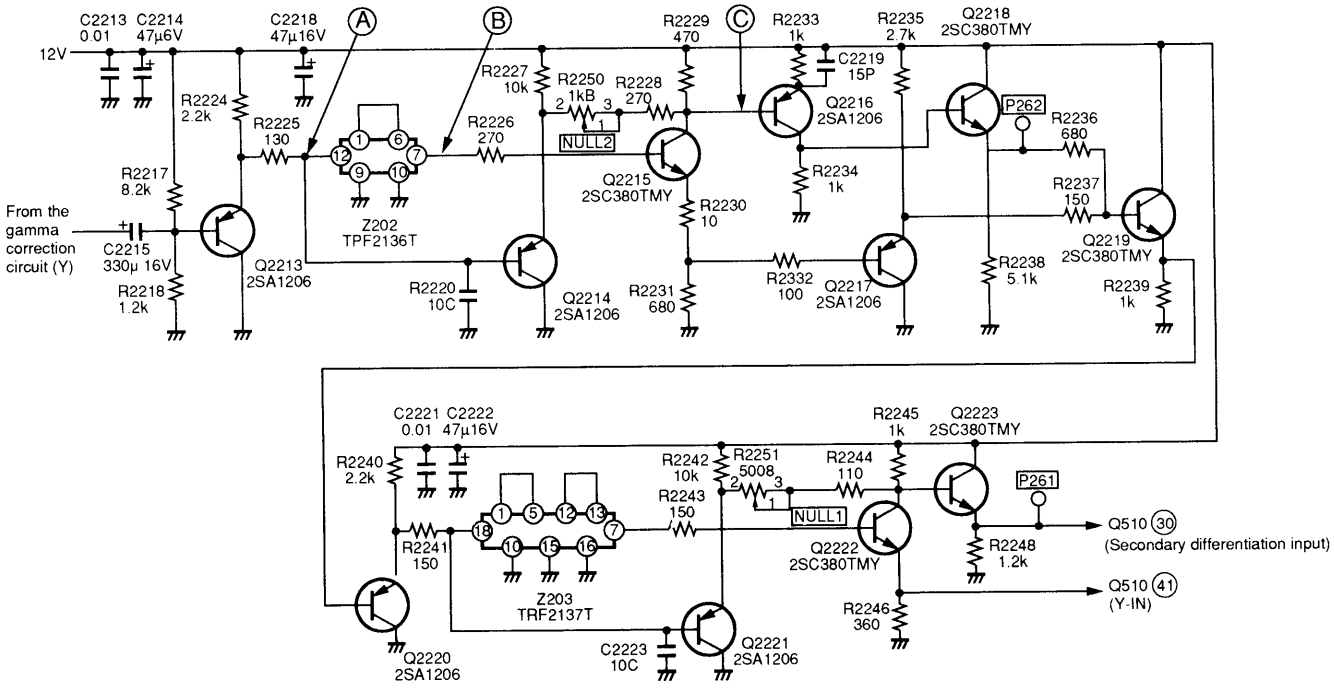


Fig. 5-20

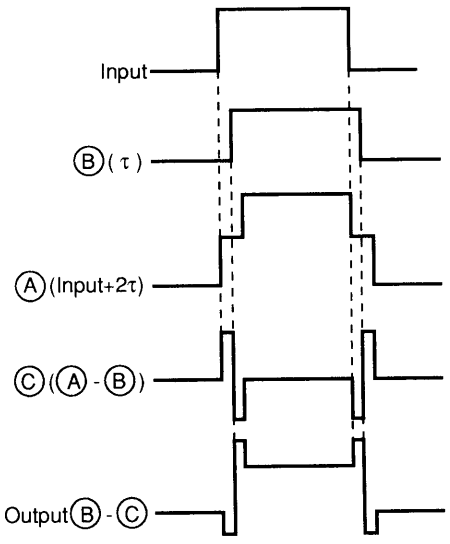


Fig. 5-21

7-2-3. RGB Processor

This block is composed of RGB processor IC TA1211N.

TA1211N has the following functions:

- Black extension circuit
- Contrast, bright adjusting circuit
- Color, tint adjusting circuit
- RGB matrix
- RGB switch
- White balance adjusting circuit

The contrast, brightness and white balance adjustments are carried out by the RGB unit (fixed in this IC).

The block diagram of TA1211N is shown in Fig. 5-22 while the pin functions are given in table 5-13.

Table 5-13 TA1211N pin function

Pin No.	Name	Function	Pin No.	Name	Function
1	DAC1	Direct current transmission volume correction switching	30	Secondary differential input	Picture quality correction signal (secondary differentiation signal) input
2	DAC2	Black expansion start point switching	31	Y CLAMP	Capacitor connection terminal for Y signal clamp
3	DAC3	Gamma correction switching	32	Color	Capacitor connection terminal for color limiter hold
4	TEST	NC	33	I/U-IN	I/U signal input
5	B – Y CLMP	Condenser connection terminal for B-Y clamp	34	Q/V-IN	Q/V signal input
6	Vcc	2.2 V (for IIL)	35	Monitor	Waveform adjusting terminal (sub-contrast)
7	SCP	Input terminal (SCP) sand castle pulse for clamp and black peak mask	36	B – Y	B-Y signal level adjusting terminal
8	BLK	Blanking pulse input terminal	37	G – Y	G-Y signal level adjusting terminal
9	GND		38	R – Y	R-Y signal level adjusting terminal
10	DSA	I^2C bus data	39	Vcc	12V
11	SCL	I^2C bus clock	40	D. ABL	Dynamic ABL terminal
12	GND		41	Y-IN	Y signal input
13	R-OUT	R output	42	DC. REST	Direct current transmission correction terminal
14	G-OUT	G output	43	BLK EXP POINT	Black expansion start point terminal
15	B-OUT	B output	44	BLK DET	Black expansion black peak hold (black area) terminal
16	Vcc	12V	45	C-IN	Not used
17	OSDYs	OSD Ys input (to be used for 3-value SYNC mask)	46	GND	
18	OSD R	Not used	47	ACC DC	Not used
19	OSD G	Not used	48	C-OUT	Not used
20	OSD B	Not used	49	Vcc	12V
21	V. MUTE	Video mute terminal	50	V-OUT	Not used
22	YM	Half tone switching (Not used)	51	CLMP DC	Not used
23	YS	PAL/SECAM RGB switching	52	GND	
24	R-IN	PAL/SECAM R input	53	V-IN	Not used
25	G-IN	PAL/SECAM G input	54	R – Y CLMP	Capacitor connection terminal for R-Y clamp
26	B-IN	PAL/SECAM B input			
27	RGB BRT	RGB input contrast terminal			
28	Uni-color	Uni-color control voltage terminal			
29	Bright	Brightness control voltage terminal			

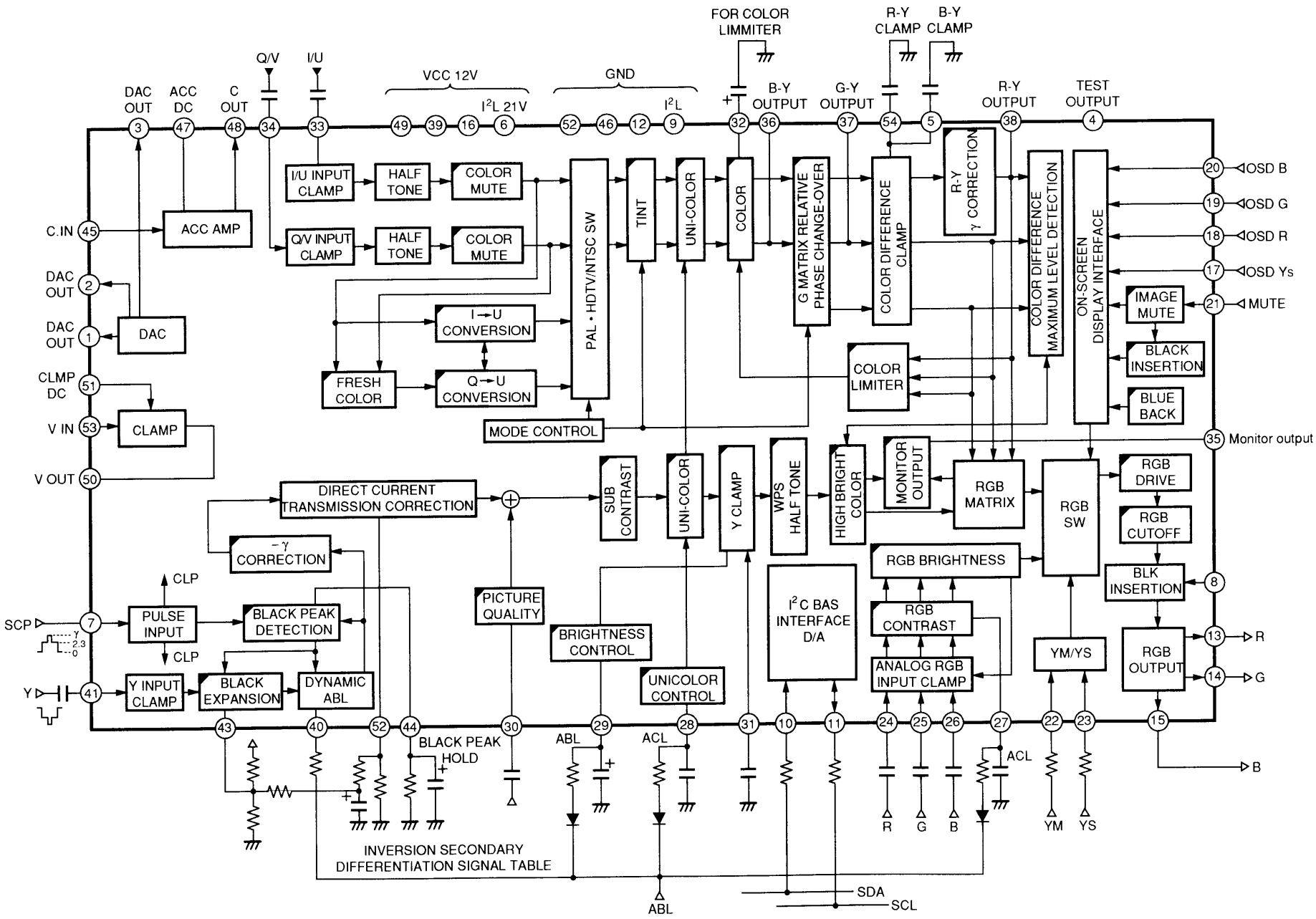


Fig. 5-22 TA1211N block diagram

8. CONTROL SYSTEM

A variety of controls of video circuit are all carried out by the bus control from the microprocessor. The main ICs of V/C IC (Q501), RGB processor IC (Q510), etc. are directly controlled by the bus control, and the other ICs are controlled by the I^2C bus corresponding DA converter Q2103 (CXA1315P). The pin functions of Q2103 are shown in table 5-14.

Table 5-14

Pin No.	Name	Function	Output level
2	SW0 (BPDET)	HDTV black area detection switching (Q2102) HDTV clamp pulse width switching (Q3307)	HDTV: 4.5V, others: 0V
1	SW1 (NOSYNC)	Clamp switching (Q2236) during no signal	7.5 V (fixed)
9	SW2 (HDTV/OTHER)	HDTV video, sync switching (video: Q2201, sync Q3200)	HDTV: 0V, others: 4.0V
10	SW3 (TV MUTE)	Video mute (Q510)	OFF: 0V (fixed)
7	DAC0 (UPC/OTHER)	Up-converter clamp pulse switching (Q3200)	NTSC: 4.5V, others: 0V
6	DAC1 (NTSC/PAL)	PAL/SECAM video, sync switching (video: Q2101, sync: Q3400)	PAL/SECAM: 0V, others: 9V
5	DAC2	Not used	
4	DAC3	Not used	
3	DAC4	Not used	

SECTION VI
RGB CIRCUIT

1. OUTLINE

The RGB circuit is composed of input signal switching circuit, video signal amplifier circuit, video blanking circuit, ON-SCREEN signal/test signal processing circuit, brightness control circuit, control circuit, sync signal processing circuit and trimming circuit.

2. INPUT SIGNAL SWITCHING CIRCUIT

The signal input to the RGB circuit is available in the RGB signal input from RGB1 and RGB 2, and the RGB signal supplied from the HD/VIDEO circuit. These signals are switched over by the relay. In addition, the signal supplied to the HD/VIDEO is also simultaneously switched.

The Fig. 6-1 shows the case where the RGB1 has been selected. At this time, S101, S102 and S108 are selected, and the input video signal is supplied to the next-stage amplifier circuit. Since S108 and S107 are selected at the same time, the input video signal is also supplied to the green on-sync separation circuit.

When RGB2 is selected, the S104 and S105 are selected and the signal is supplied to the next stage similarly to the above.

When signal of HD/VIDEO is selected, S108 is selected, the signal from HD/VIDEO is supplied to the next stage amplifier circuit. In this case, all the S101, S102, S104 and S105 are all switched off, and the signal input to RGB2 is supplied to the HD/VIDEO. This is because RGB2 is also used for the input terminal of high vision signal. At the same time, S107 is selected, and the signal of RGB2 is supplied to the green on-sync separation circuit. This is because the signal synchronizing process is carried out when the high vision signal input to RGB2 is selected.

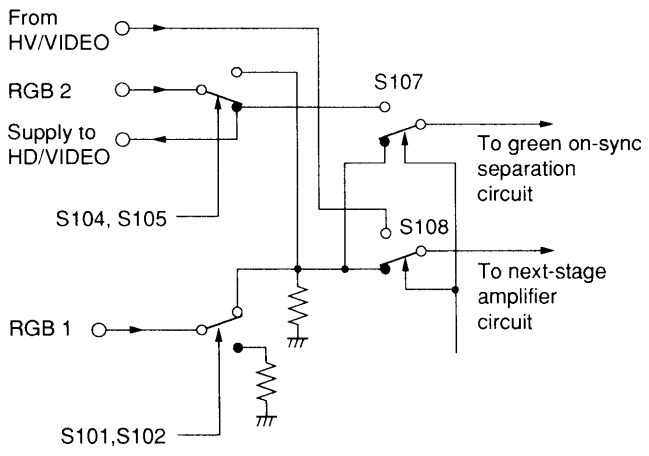


Fig. 6-1

3. VIDEO SIGNAL AMPLIFIER CIRCUIT

Fig. 6-2 shows the block diagram of video signal amplifier circuit. The R, G and B signals supplied from the pre-stage switching circuit are input to the contrast IC LM1201N (Q101, Q102 and Q103) respectively. The 3-axis identical bias voltage is usually supplied to the contrast terminals of the IC. During the video mute and the single color cutoff, the video signal level develops zero by developing each contrast terminal to Lo level.

The next stage Q104 is 3-channel video amplifier (M52320SP), and performs the contrast adjustment, R and B axis drive adjustment (G-axis is the reference and the gain is fixed), superimposing on-screen character and the direct current restoration (pedestal clamp) is carried out. Fig. 6-3 shows the block diagram of M52320SP.

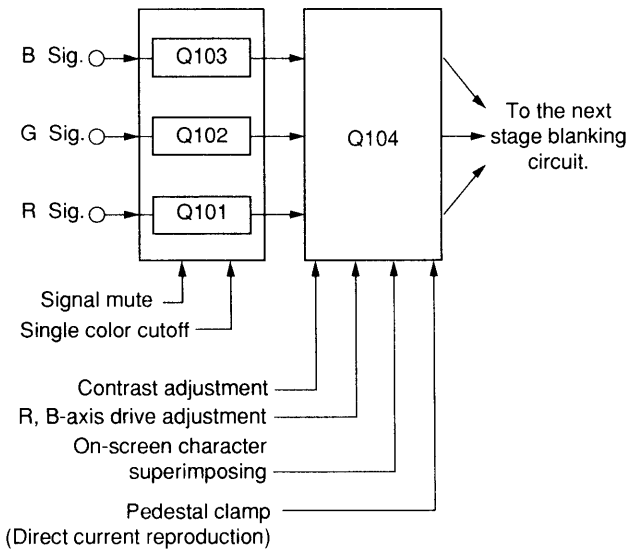


Fig. 6-2

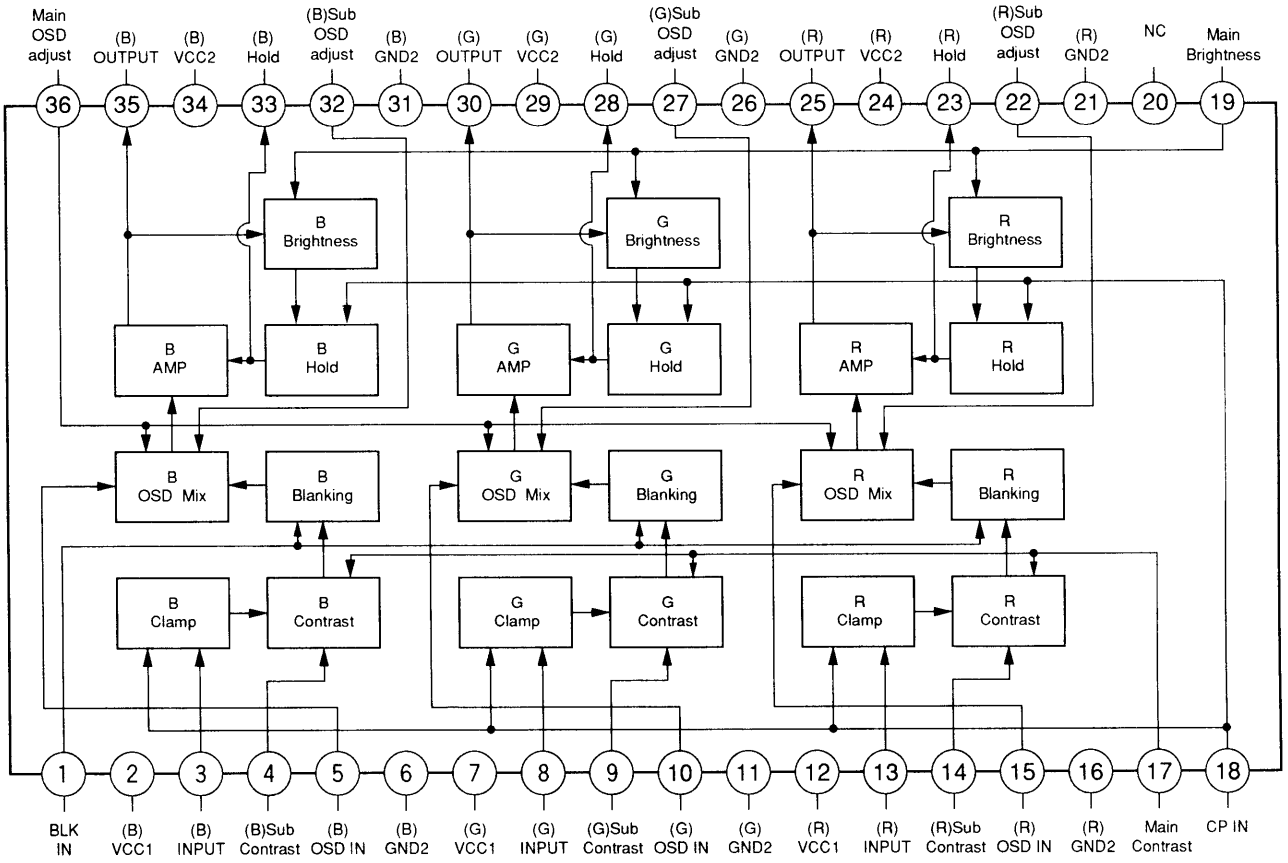


Fig. 6-3 M52320SP block diagram

4. VIDEO BLANKING CIRCUIT

After applying the blanking to the video signal supplied from the pre-stage video signal amplifier circuit, the signal is supplied to the CRT drive circuit via the buffer.

Blanking operation is carried out with the signal added by the ORed signals of horizontal blanking, vertical blanking, DEF mute, clamp pulse and trimming pulse through the Or-gate Q162. And this circuit outputs the signal to the CRT drive circuit via the buffers of Q106, Q109 and Q112.

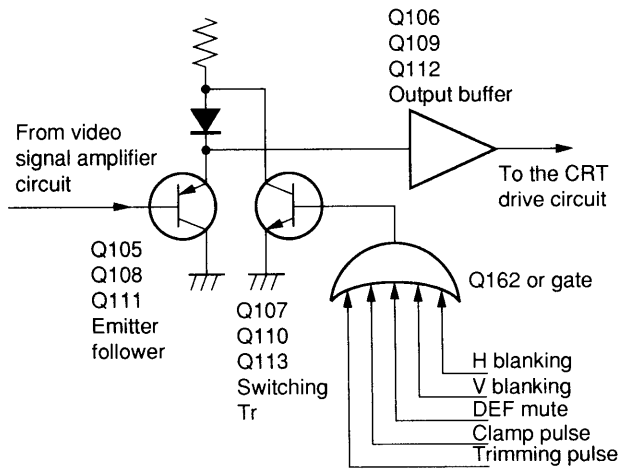


Fig. 6-4

5. ON-SCREEN SIGNAL/TEST SIGNAL PROCESS CIRCUIT

The ON-SCREEN character generation circuit is composed of 2 ICs (Q211, Q212). The test signal is supplied from the control circuit in each color of R, G and B. This is switched by the Q214 gate so that the color selection may be available. The ON-SCREEN signal and test signal are added at the Q213 or-gate, and is supplied to the 3-channel video amplifier IC Q104 of video signal amplifier circuit.

6. BRIGHTNESS CONTROL CIRCUIT

The brightness control is carried out by varying the G1 bias. The bias voltage is generated inside the RGB circuit and supplied to the CRT drive circuit.

The brightness control voltage is supplied from the DAC (see the item of control circuit described later). The DC voltage is amplified and level shifted.

The R-axis and B-axis bias adjustment can be performed by Q149 and Q152 so that the cut-off bias fine adjustment is carried out.

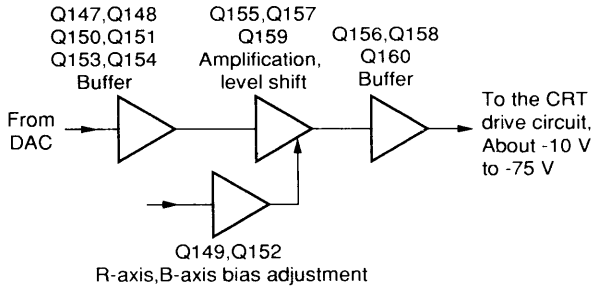


Fig. 6-5

7. CONTROL CIRCUIT

Various switching inside the RGB circuit and the DC control are carried out by the DA converter (CXA1315, Q201 – Q204) applying to I^2C bus control. Tables 6-1 to 6-4 show the contents of control.

Table 6-1 Q201

Pin No.	Name	Function	Output level	
7	DAC0	Contrast	0V – 9V	
6	DAC1	Brightness	0V – 9V	
5	DAC2	ABL level	0V – 9V	
4	DAC3	YPbPr selection	During selection: 0V	During no selection: 4.5V
3	DAC4	Not used	—	
2	SW0	RGB1 selection	During selection: OFF (0.7V)	During no selection: ON (0V)
1	SW1	RBG2 selection	During selection: OFF (0.7V)	During no selection: ON (0V)
9	SW2	YPbPr, Video selection	During selection: OFF (5V)	During no selection: ON (0V)
10	SW3	Trimming ON/OFF	During ON: OFF (5V)	During OFF: ON (0V)

Table 6-2 Q202

Pin No.	Name	Function	Output level	
7	DAC0	R drive adjustment	0V – 9V	
6	DAC1	B drive adjustment	0V – 9V	
5	DAC2	R cutoff bias adjustment	0V – 9V	
4	DAC3	B cutoff bias adjustment	0V – 9V	
3	DAC4	Not used	—	
2	SW0	R single color cutoff	During cutoff: OFF (5 V)	During projection : ON (0V)
1	SW1	G single color cutoff	During cutoff: OFF (5 V)	During projection : ON (0V)
9	SW2	B single color cut off	During cutoff: OFF (5 V)	During projection : ON (0V)
10	SW3	Video mute	During mute: OFF (5V)	During projection : ON (0V)

Table 6-3 Q203

Pin No.	Name	Function	Output level
7	DAC0	Trimming TOP	0V – 9V
6	DAC1	Trimming BOTTOM	0V – 9V
5	DAC2	Trimming LEFT	0V – 9V
4	DAC3	Trimming RIGHT	0V – 9V
3	DAC4	Not used	—
2	SW0	Identification when fH higher than 40 kHz	Higher than fH 40 kHz: OFF (5V) Lower than fH 40 kHz: ON (0V)
1	SW1	Not used	—
9	SW2	Test/reception switching	When receiving the test signal: OFF (5V) During reception: ON (0V)
10	SW3	HD clamp setting	When setting the HD clamp: ON (0V) When setting the AUTO clamp: OFF (5V)

Table 6-4 Q204

Pin No.	Name	Function	Output level
7	DAC0	Not used	—
6	DAC1	Not used	—
5	DAC2	Not used	—
4	DAC3	Not used	—
3	DAC4	Not used	—
2	SW0	Not used	—
1	SW1	Not used	—
9	SW2	Not used	—
10	SW3	Not used	—

8. SYNC SIGNAL PROCESS CIRCUIT

This unit applies to various sync signal patterns of green ON sync (sync negative), composite sync (0.3 V(p-p) to 5 V(p-p), positive/negative polarities, including high vision 3-value sync) and HV separate sync (0.3 V(p-p) to 5 V(p-p), positive/negative polarities). This circuit automatically selects these input sync signals, performs the waveform shaping, and supplies them to each of other circuits as the 5 V(p-p) positive polarity pulse. The circuit diagram is shown in Fig. 6-6.

8-1. Sync Separation Circuit

Q3051 is the dedicated IC (M52036) to automatically perform the selection, sync separation and waveform shaping, and outputs the green ON sync signal to pin 4, the H sync and composite sync signals to pin 6 and the V sync signal to pin 8 respectively. H sync and the composite sync (negative) signals are output from pin 15, V sync signal (positive) is output from pin 13, and H sync signal (positive) is output from pin 14. The output signal from pin 15 is HV separated and inverted, and then input to pin 11. The input sync signal automatically selected, sync-separated and waveform-shaped is supplied to the multiplexer Q3061 after the polarity of the output signal from pins 13 and 14 is inverted to negative. The negative polarity signal from pin 15 is used as the H sync signal for deflection because the front edge phase compensation accuracy of pulse is high, while the positive polarity signal from pin 14 is used as the back porch clamp pulse generation signal because the back edge phase compensation accuracy is high.

8-2. Switching Circuit (1)

Q3061 switches the signal supplied from the sync separation circuit and the H and V sync from HD/VIDEO. The signal supplied from the sync separation circuit is selected when pin 1 develops Lo, and the signal from HD/VIDEO is selected when pin 1 develops Hi. The selection is ANDed 2 kinds of signals input to Q214. Q201 SW2 develops Hi only when selecting the PbPr and video, while the Q201 DAC 3 develops Lo only when selecting the YPbPr. Therefore, the AND gate output develops Hi when selecting the video and Lo when selecting the RGB 1, 2 and PbPr. The signals which have been selected in this way are output as the H sync (negative polarity) from pin 4, V sync (negative polarity) from pin 12 and H pulse (positive polarity) from pin 7 of Q3061, respectively.

8-3. Sync Signal Presence or Absence Identification Circuit

The output from the Q3061 switch is identified by the monostable multivibrator circuit. The horizontal sync signal is identified by Q3063 (TC74HC123), the trigger is set to the leading edge of the signal, and the output pulse width is set to 100 µs. This setting is available because the applicable maximum length period of this unit is 66 µs (15 kHz). Therefore, if a signal is present, the output $\overline{Q}$ develops Lo re-triggered at all times within the period less than the pulse width. The output $\overline{Q}$ develops Hi when the signal is not present.

The vertical sync signal is identified by the Q3062 (TC4538), the trigger is set to the leading edge of the signal and the output pulse width is set to 32 ms. This setting is available because the applicable maximum length period of this unit is 26 ms (38 Hz). Therefore, if a signal is present, the output $\overline{Q}$ develops Lo re-triggered at all times with the period less than the pulse width. The output $\overline{Q}$ develops Hi when the signal is not present.

The output $\overline{Q}$ of the monostable multivibrator is added by the Q3057 or-gate, and is output to the control circuit with the Hi logic during no signal is present.

The Hi logic signal is added to the signal by Q3057 or-gate during the test mode, not only for controls the next selector switch, and then supplied to the deflection circuit as the INT/EXT signal.

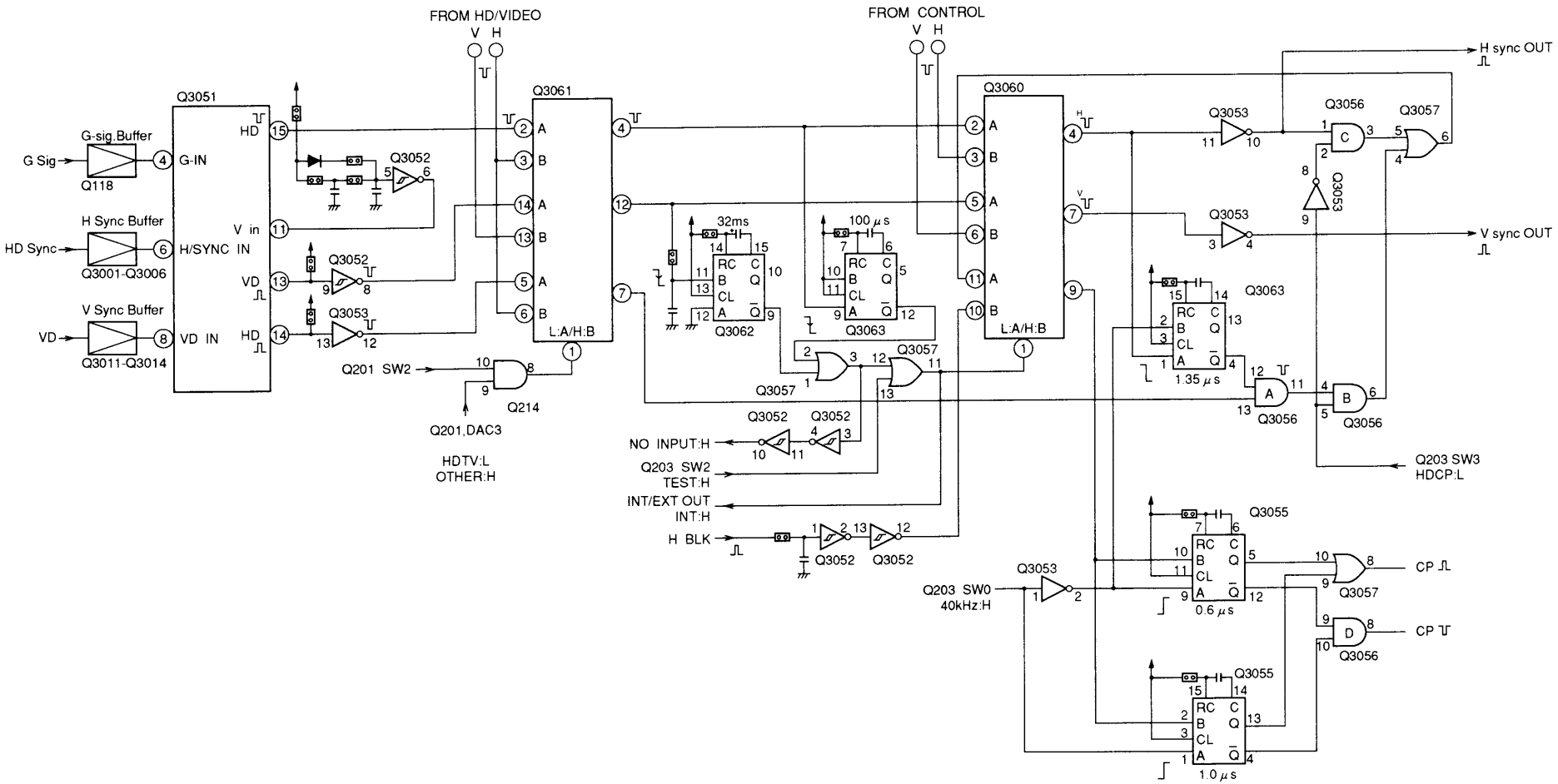


Fig. 6-6 Sync signal process circuit diagram

8-4. Switch Circuit (2)

The Q3060 switches the signal from the switch circuit (1) and the internal sync signal from the control circuit. The signal from the switch circuit (1) is selected when pin 1 develops Lo, and the internal signal from the control circuit is selected when pin 1 develops Hi. The selection is carried out by the output signal of from the identification circuit in item 8-3. Therefore, the internal sync signal is selected when any of H sync and V sync doesn't exist and during the test mode, and the reception sync signal is selected during the usual reception mode.

The signal selected in this way is output from pin 4 as the horizontal sync signal and pin 7 as the vertical sync signal. Then the output signal is output to each circuit after inverted at Q3053.

8-5. Clamp Pulse Generation Circuit

This unit is also applicable to the high vision signal which is superimposed by 3-value sync signal. Therefore, all the signals lower than 40 kHz of horizontal frequency are integrated to be clamped in the same phase with the high vision signals, and the automatic clamp setting is realized.

The pulse of 1.35 μs is generated from the leading edge of sync signal selected by the Q3063 monostable multivibrator. This is shows the 3-value sync signal period of high vision signal is the specified value of 1.186 μs.

Next, the pulse of 1.35 μs (negative polarity) and the signal selected in the switch circuit (1) Q3061, pin 7, negative polarity) is multiplied by the Q3056A (AND gate).

As shown in Fig. 6-7, if the negative polarity pulse is multiplied, any of wider pulses is obtained as the output. Therefore, here the pulse of minimum width 1.35 μs whose front edge coincides with the horizontal sync signal phase is obtained.

For reference, because the pulse of 1.35 μs may be too wide when the signal higher than fH = 40 kHz is used, the monostable multivibrator output is fixed to Hi by the Q203 SW0. Since the high vision signal is decided to fH = 33.75 kHz, it is not necessary to specify the clamp pulse phase with the front edge of horizontal sync signal.

The pulse and the inverted signal of horizontal sync signal selected by Q3060 is selected by the switch circuit composed of Q3056A, B and Q3053 inverter. The pulse described previously is selected since the Q203 SW3 develops Hi during the AUTO clamp setting.

If the HD clamp is selected by the menu setting, the inverted signal of horizontal sync signal is selected.

In this way, when the matching with the input signal is worse and the defective appears on the back porch clamp, the HD clamp is carried out forcibly.

The selected pulse is supplied to the switching SW Q3060 via the Q3057 or-gate. The Q3060 switching SW performs the switching operation between the pulse described previously and the horizontal blanking pulse. This is because, when the internal signal is selected, the clamp pulse is generated with the blanking pulse which is the reference signal of the signal.

With the rising edge of the signal selected by Q3060 as its trigger, 2 kinds of pulse, 0.6 μs and 1.0 μs are generated by Q3055 monostable multivibrator. Here, the pulse of 1.0 μs is output by the Q203 SW0 when the fH is lower than 40 kHz, and the pulse of 0.6 μs is output when the fH is higher than above. This is because the pulse width is as much wider as possible if the fH is low.

Thus, the clamp pulse with both positive/negative polarities is obtained and supplied to the video signal amplifier circuit.

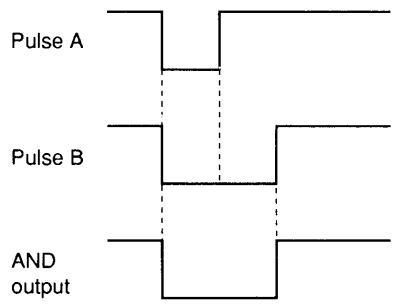


Fig. 6-7

9. TRIMMING CIRCUIT

9-1. Vertical Trimming Circuit

The pulse, which is generated by slicing the vertical saw tooth waveform (supplied from the convergence circuit) with the Q3041 OP amp., is supplied to the blanking circuit by the vertical trimming circuit. The slice DC voltage is supplied from the control circuit (DA converter IC).

9-2. Horizontal Trimming Circuit

The pulse, which is generated by the Q3044 monostable multivibrator with the horizontal blanking pulse as its trigger, is supplied to the blanking circuit by the horizontal trimming. The feedback is applied by the Q3042 OP amp. to obtain the stable operation.

SECTION VII
CRT-D CIRCUIT

1. OUTLINE

In the CRT-D circuit, the video signal supplied from the RGB circuit is amplified to the amplitude that can drive the CRT (projection cathode ray tube). In addition, the bias necessary for each electrode is also supplied. The circuit is identical in 3 axis of R, G and B. The cathode and G1 (G1-K drive) are also driven.

The block diagram and major waveforms are shown in Fig. 7-1.

The video signal supplied from the RGB circuit, after passing through the input buffer, is supplied to the hybrid IC (VPA 13), and amplified up to the cathode drive level.

The cascade connection amplifier circuit is built-in inside the IC, and the buffer is added to the output portion. The gain of the IC is 14 times as much as the specified value.

On the other hand, the G1 drive is amplified up to G1 drive level by the cascade connection circuit consisting of Q902, Q932, Q962 and the internal transistor of the hybrid IC. And then, it is output to the G1 electrode via the buffer. The video signal here becomes the positive polarity.

The signal is C-cut here, and the peak portion of blanking is clamped by the diode (D915, D945, D975). The brightness variable operation is carried out by changing the bias.

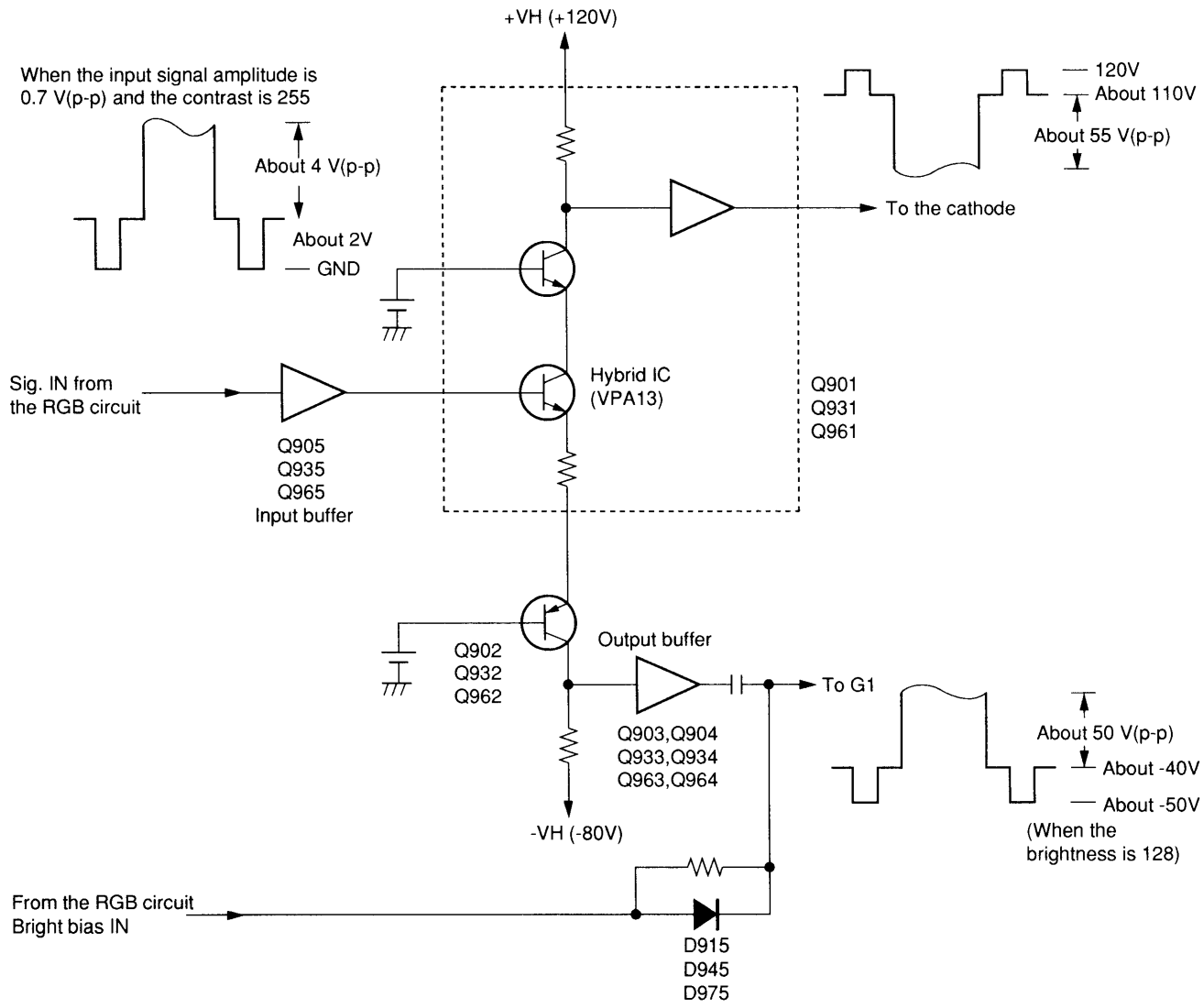


Fig. 7-1

SECTION VIII
DEF CIRCUIT

1. OUTLINE

1-1. Features

(1) Corresponds to the input frequency fv = 38 Hz to 160 Hz.

(2) Adopts the vertical phase circuit less in drift against the temperature change.

(3) The both positive/negative power supply system is applied for the vertical output circuit and the DC cut capacitor is eliminated in the output stage and this realizes the DC amplifier system.

(4) The vertical output stage is independently structured for each system of red, green and blue colors. Thereby, it makes it possible to perform the vertical centering adjustment independently on each system.

(5) The voltage switching system for applying a high voltage only during the vertical feedback period is adopted to the positive side power supply of vertical output circuit. This realizes less power consumption of the output circuit.

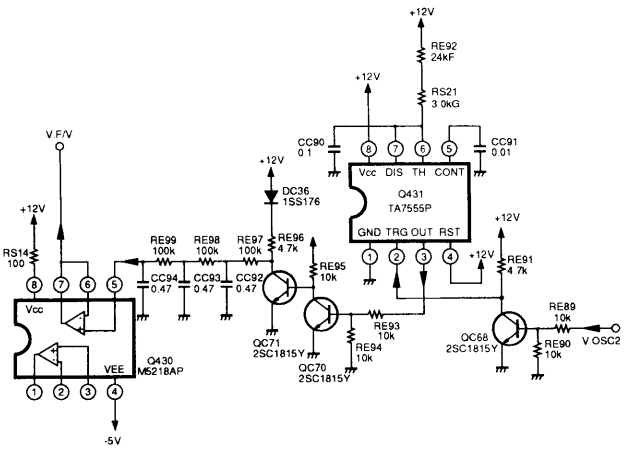


Fig. 8-1

2. VERTICAL F/V CONVERSION CIRCUIT

This circuit outputs the direct current voltage proportional to the vertical frequency of video signal. Hereunder, this direct current voltage is called the V. F/V (Vertical F/V voltage).

In the vertical reference waveform generation circuit (item 6) and the convergence reference waveform generation circuit (section 11), the charging/discharging current flow amount in the reference waveform generation block is changed according to the frequency by using the V. F/V voltage as the input so that the amplitude of reference waveform becomes constant at the frequency range from 38 Hz to 160 Hz.

Fig. 8-1 shows the circuit construction.

The pseudo sync signal V. OSC2 output from the vertical oscillation circuit via QC50 is inverted in its polarity by QC68, and input to pin 2 of Q431. Q431 is generally called the timer IC, triggers the input signal to pin 2 and outputs the HIGH pulse of constant time width to pin 3. The output pulse width Tw of pin 3 is proportional to the resistors (RE92 + RS21) connected to pin 6 and the capacitor (CC90).

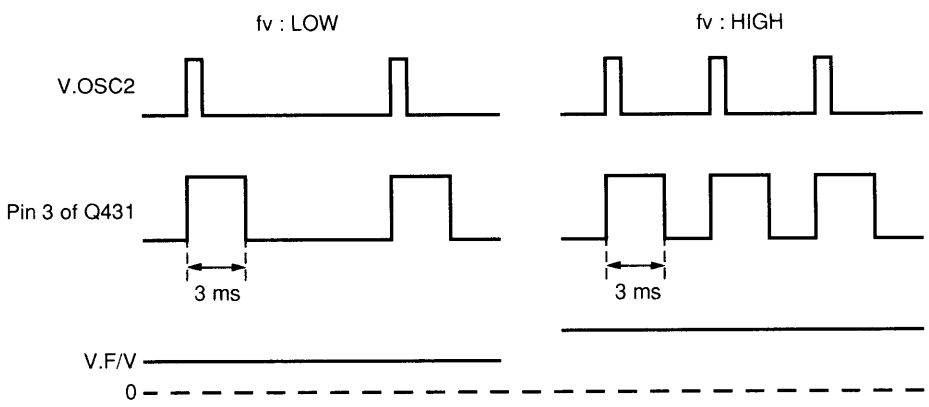


Fig. 8-2

Here, the relation between them is as follows;

$Tw = 1.1 \times (RE92 + RS21) \times CC90$ (s)

Actually the pulse of Tw = 3.0 (ms) is output from pin 3.

The signal input to pin 2 is the vertical period signal as mentioned before, Q431 is triggered once at every vertical period, and thereby output the pulse of 3.0 ms to pin 3. The pulse output from pin 3 is twice inverted in its polarity at QC70 and QC71, then converted into the direct current voltage using the low pass filter consisting of RE97 to RE99 and CC92 to CC94, and output as the V. F/V voltage via the buffers of pins 5 to 7 of Q430.

Further, DC 36 is connected in series with the RE96 for its temperature compensation in order to lessen the variation due to the temperature drift of V. F/V voltage.

As it can be known from these facts, the pulse duty of pin 3 of Q431 is changed by the vertical frequency, and when the frequency is high (when one vertical period is short), the ratio of HIGH period becomes greater and the value of V. F/V voltage becomes higher.

Suppose the vertical frequency of image receiving signal as fv (Hz) and the value of V. F/V voltage as $V_{F/V}$ (V), the $V_{F/V}$ is proportional to fv, and the following relation exists between them :

$V_{F/V} = 0.031 \times fv$

3. VERTICAL PHASE CIRCUIT

This circuit triggers the vertical sync signal V. SYNC of image receiving signal and outputs the phase adjusted pseudo sync signal VD. The VD is delayed by approx. 1 vertical period against the V. SYNC using two stages of monostable multivibrator, and the vertical phase can be varied by finely adjusting this delay amount.

Fig. 8-3 shows the circuit construction.

V. SYNC is input to pin 2 of 1st stage monostable multivibrator QC51 and the signal is triggered. The output pulse width of pin 4 is determined by the charging current amount flowing into the time constant capacitor CC74. The charging current is supplied from pin 1 of QC52 via QC53, and the current flowing order is pin 1 of QC52 → QC53 → CC74 → pin 4 of QC51 → pin 2 of QC52 → pin 1 of QC52. In this order, the feedback loop is formed and the voltage comparison system between pin 2 of QC52 and pin 3 of QC52 is actuated. Accordingly, the charging current amount of CC74 is controlled so that the average voltage value of the output pulse from pin 4 of QC51 equals to the voltage at pin 3 of QC52.

Even when the vertical frequency changes, the constant duty pulse decided by the voltage of pin 3 of QC52 is output from pin 4 of QC51.

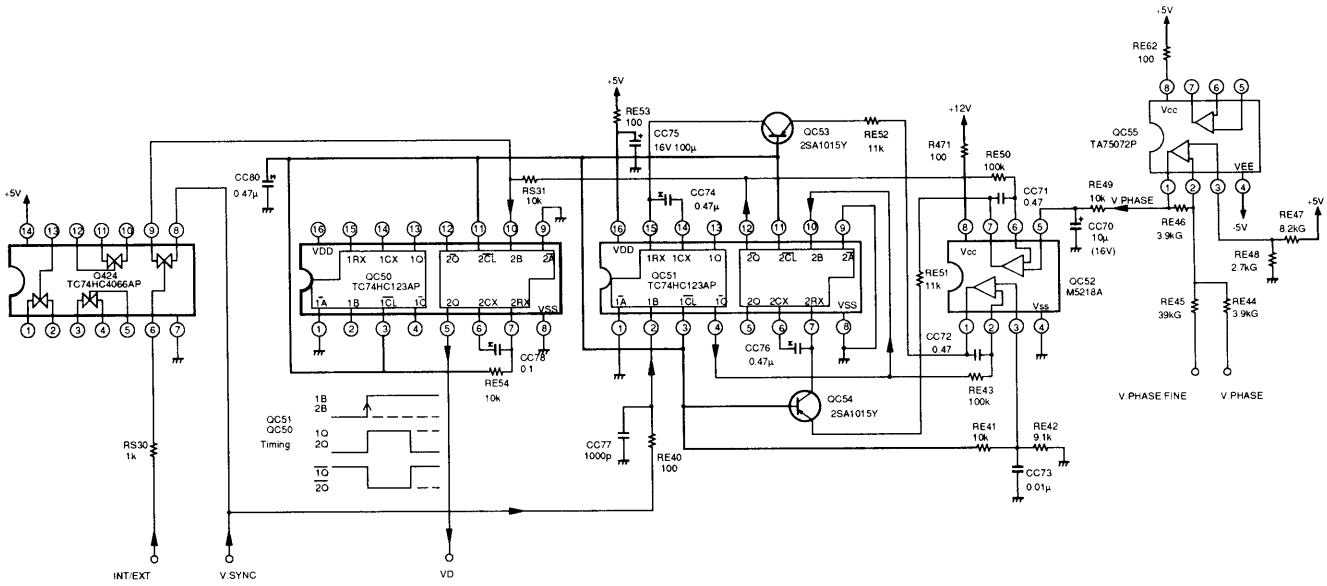


Fig. 8-3

Here, supposing the output pulse width from pin 4 of QC51 is referred as T_{OUT} and the one vertical period is as Tv, the average output value of pin 4 of QC51, V_{AV} is shown by the equation below.

$$V_{AV} = \frac{1}{Tv} \times (0 \times T_{OUT} + 5 \times (Tv - T_{OUT}))$$

$$= 5 \times (1 - \frac{T_{OUT}}{Tv}) \quad \ldots\ldots (1)$$

On the other hand, the voltage value $V_{(3)}$ of pin 3 of QC52 is shown by the equation below.

$$V_{(3)} = 5 \times \frac{RE42}{RE41 + RE42} \quad \ldots\ldots (2)$$

As described above, because the control is applied so that the value of Equation (1) becomes identical to the value of Equation (2), the output pulse width T_{OUT} of pin 4 of QC51 is determined by the following relational equation.

$$T_{OUT} = (1 - \frac{RE42}{RE41 + RE42}) \times Tv$$

In fact, the pulse of time width of 52% one vertical period is output to pin 4 of QC51.

The output of pin 4 of QC51 is input to pin 9 of 2nd stage monostable multivibrator QC51 and triggered at the back edge of pin 4 pulse. Thereby, the 2nd stage monostable multivibrator starts its operation delaying with 52% time of one vertical period against the V. SYNC.

The charging current flow of 2nd stage monostable multivibrator time constant capacitor CC76 is also composed of the feedback loop similar to the 1st stage, and the pulse width of 2nd stage output pin 12 of QC51 is determined by the voltage applied to pin 5 of QC52. The voltage applied to pin 5 of QC52 is varied in the range of 2.5 ± 0.33V in accordance with the user adjustment (V. SIZE, V. SIZE. FINE) state by remote control unit. Thereby, the pulse of time width of 50 ± 6.6% one vertical period is output to pin 12 of QC51. The signal is triggered and input to pin 10 of the monostable multivibrator QC51 for the pulse width conversion at the back edge of pin 12 of QC51 pulse (The conversion is necessary because the allowable pulse width of sync input terminal, pin 30, of the vertical oscillation circuit Q410 described later is 3.0 ms maximum.), and the pseudo sync signal VD with constant width of 1.0 ms) is output from pin 5.

As described before, the pseudo sync signal VD is generated at the position delayed by the total time of 102 ± 6.6% in one vertical period (one vertical period is 100%) summing up the 1st and 2nd stage delay amount against the vertical sync signal V. SYNC. Thereby, the VD phase adjustment can be carried out against the V. SYNC (= pattern).

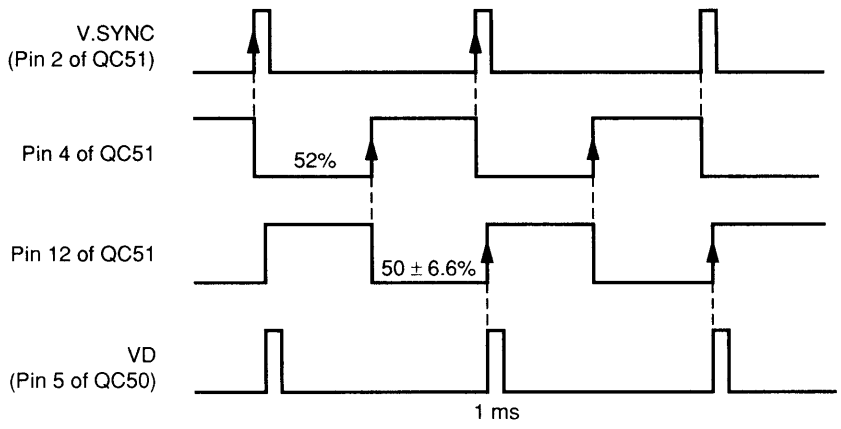


Fig. 8-4

4. VERTICAL OSCILLATION CIRCUIT

This circuit triggers the pseudo sync signal VD for its sync pull-in and performs the vertical oscillation.

Fig. 8-5 shows the circuit construction.

Q410 (LA7860) is the deflection IC to perform the vertical oscillation, sync pull-in, horizontal oscillation and sync pull-in. Pins 23 to 30 are the input/output terminals of vertical block.

The pseudo sync signal VD, after its polarity is inverted by QC56, is input to pin 30 of Q410.

Q410 triggers the falling edge of input signal to pin 30 and performs sync pull-in, and outputs the pseudo sync signal V.OSC1 to pin 24.

The V.OSC1 is converted to the HIGH pulse of 100 µs constant width in QC50 and output to the vertical saw tooth waveform generation circuit (to be described later) as the V. OSC2 from pin 13.

If no trigger input is observed at pin 30 of Q410 during no RGB signal input, the oscillation is carried out with the free-run frequency of approx. 32 Hz.

Pin 26 of Q410 (LA7860) is the variable terminal of vertical phase and the output timing of V. OSC1 signal at pin 24 can be changed by controlling the DC voltage of the terminal. Thereby, the phase adjustment can be adjusted. But in P7300U, since the vertical phase circuit described in item 3 is applied, the vertical phase variable function of LA7860 is not used.

Therefore, pin 26 is connected to the ground, and the phase delay of pin 24 is set to the minimum (zero) state.

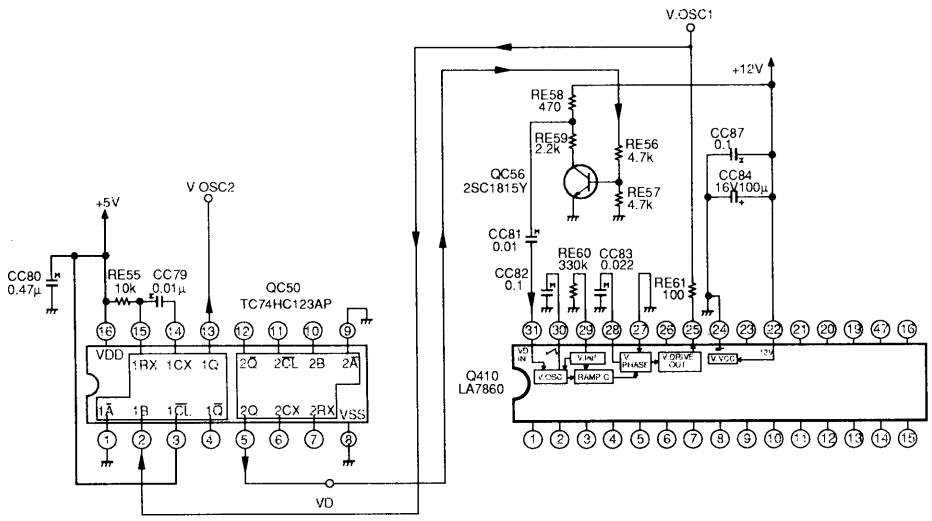


Fig. 8-5

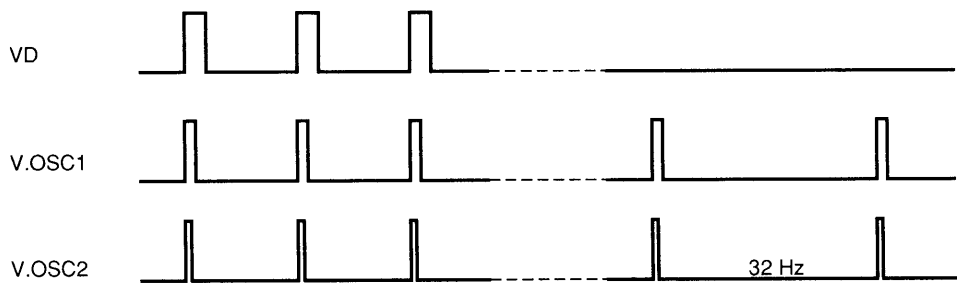


Fig. 8-6

5. VERTICAL SAW-TOOTH WAVE-FORM GENERATION CIRCUIT

This circuit generates the vertical period saw tooth waveform V. SAW1 using the pseudo sync signal V. OSC2 output from pin 13 of QC50 as an input signal. In order to keep the amplitude of V. SAW1 to the constant amplitude of 2.0V(p-p) within the frequency range from 38 Hz to 160 Hz, the discharging current amount of the saw tooth waveform generation capacitor is varied by the frequency in this circuit.

In the next stage circuit, the reference waveform for the deflection current using V.SAW1 is generated.

Fig. 8-7 shows the circuit construction.

CC07 and CC08 are the capacitors for the saw tooth waveform generation. The V. SAW is generated by flowing the charging current with QC02 and the discharging current with QC05 against these capacitors.

The pseudo sync signal V. OSC2 output from the vertical oscillation circuit is input to QC01.

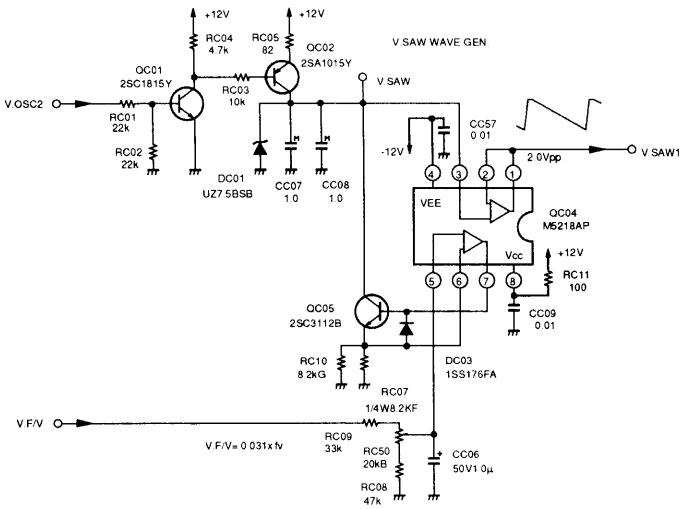


Fig. 8-7

Here, the V. OSC2 is a constant width pulse whose HIGH period of 100 μs as described above, and QC01 is turned on only during the period of 100 μs. Therefore, QC02 is turned on only during the period of 100 μs, and during this period, charges the CC07 and CC08 up to 7.5V which is the ON voltage of DC01.

When the HIGH period of V. OSC2 ends and develops the LOW level, QC02 is turned off, and the electric charge of CC07 and CC08 charged up to 7.5V starts discharging via the collector of QC05. Here, QC05 builds up the constant current circuit with QC04, and the collector current amount of QC05 is proportional to the voltage value applied to pin 5 of QC04. Since the voltage at pin 5 of QC04 is what the V. F/V is divided by the resistance, finally the collector current amount of QC05 is proportional to the vertical frequency. For example, when the image receiving frequency is doubled (the scanning period becomes half), the discharging current amount of CC07 and CC08 becomes double. Thereby, the saw tooth waveform of constant amplitude (adjusted to 2.0 V(p-p) with the semi-fixed VR RC50) is output to the V. SAW at all times even when the vertical frequency varies. V. SAW is output as the V. SAW1 via the buffers of pins 1 to 3 of QC04.

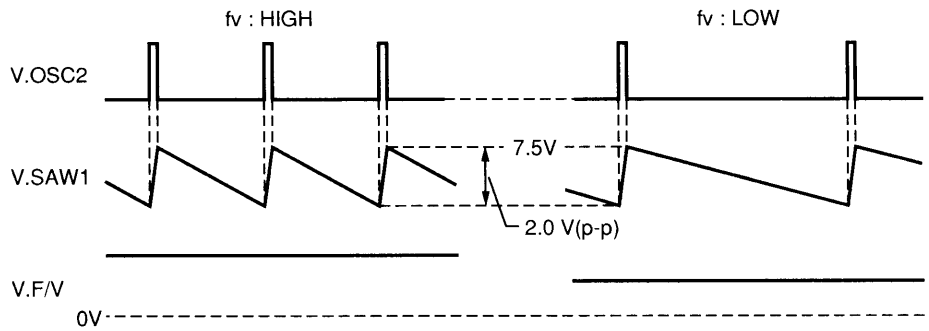


Fig. 8-8

6. VERTICAL REFERENCE WAVEFORM GENERATION CIRCUIT

This circuit generates a vertical reference signal. The vertical output circuit makes a current proportional to the reference signal flow into the vertical deflection coil.

Fig. 8-9 shows the circuit construction.

This circuit is so structured as being able to individually change the size of direct current voltage, saw tooth waveform, parabolic waveform and S-character type waveform building up the reference waveform using the microprocessor. The vertical centering (vertical direction raster shift), vertical amplitude, vertical linearity and vertical S-character type linearity are adjusted by the remote controller.

The direct current voltage, saw-tooth waveform, parabolic waveform and S-character waveform which are adjusted their amplitude by the microprocessor are added with the V. SAW3 at QC08 and QC07, and output as the red reference waveform R. REF to pin 7 of QC08, the green reference waveform G. REF to pin 1 of QC08 and the blue reference waveform B. REF to pin 7 of QC07.

Hereunder, the circuit operation is explained.

The output waveform V. SAW1 of above mentioned vertical saw tooth waveform generation circuit, after its direct current component is cut by CC13, is input to pin 2 of QC07. At the same time, V.SAW1 is input to pin 5 of QC25. QC25 is the multiplier IC, and the input waveform at pin 4 is multiplied with that at pin 5 and its result is output to pin 6 of QC25.

Here, supposing the voltages of pins 4 to 6 of QC25 as $V_{(4)}$, $V_{(5)}$ and $V_{(6)}$ respectively, the following relational equation is obtained.

$$V_{(6)} = \frac{1}{2} \times V_{(4)} \times V_{(5)}$$

The direct current voltage varying among the -2.5 V_{DC} to +2.5 V_{DC} according to the adjustment state of V. SIZE which is the user adjustment item is supplied to pin 4 of QC25 from pin 3 of QC25. The direct current voltage is multiplied with V. SAW1, and V. SAW1 becomes –1.25 times to +1.25 times. The voltage is output as the V. SAW2 to pin 6 of QC25. (–1.25 times when the V. SIZE adjustment value is 00, 0 time when the value is 128, and +1.25 times when the value is 255.)

The V. SAW2 and V. SAW1 which are generated in this way are input to pin 2 of QC07, added, and output as the saw tooth waveform V. SAW3 from pin 1. Therefore, the amplitude of V. SAW3 is varied owing to the V. SIZE adjustment value. When the adjustment value changes to 0 - 128 - 255, the saw tooth waveforms of 1.5 - 2.0 - 2.5 V(p-p) respectively is obtained. Thereby it is possible to vary the vertical amplitude.

QC09 is the same kinds of multiplier IC as QC25 and generates the parabolic waveform and S-character waveform using V.SAW3 as an input. After each amplitude of the parabolic waveform and S-character waveform is adjusted by QC27 and QC28 (DAC8840), the parabolic waveform and S-character waveform is superimposed on the saw tooth waveform adding V. SAW3 at QC08 and QC07. Thereby, the vertical linearity (upper portion shrinkage and lower portion elongation) and the vertical S-character linearity (upper and lower portion shrinkage and central portion elongation) are adjusted.

Moreover, the direct current voltages of –0.3V to + 0.3V are output from pins 1, 2, 3, 10, 11 and 24 of QC27 (DAC8840), which are added with the V. SAW3 with QC08 and QC07, the direct current voltages are superimposed on the saw tooth waveform, thereby the vertical centering (raster shift in vertical direction) is adjusted.

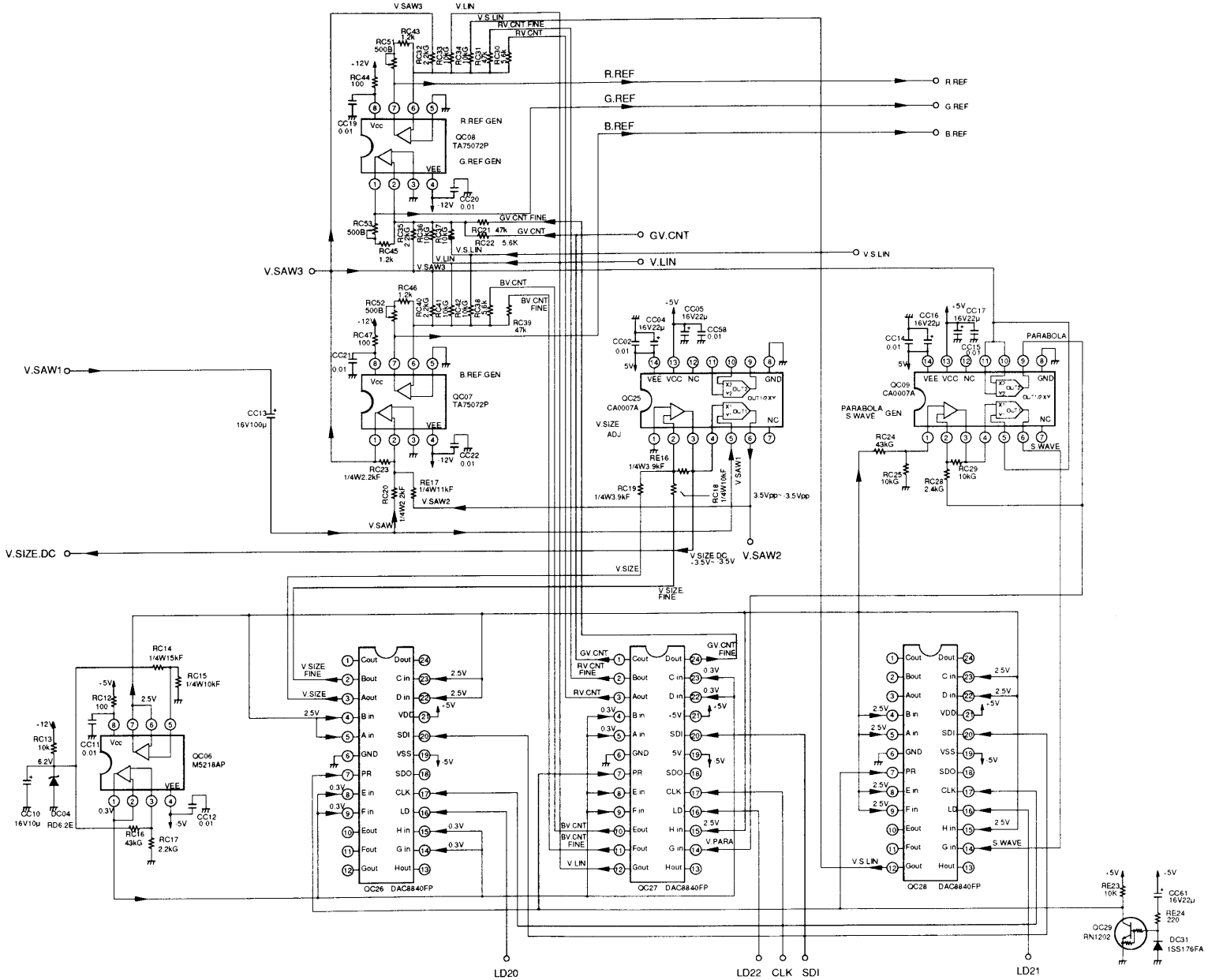

V.SAW3
V.LIN
V.S.LIN
RV.CNT FINE
RV.CNT
R.REF
G.REF
B.REF
R.REF GEN
G.REF GEN
B.REF GEN
QC08 TA75072P
QC07 TA75072P
GV.CNT FINE
GV.CNT
BV.CNT
BV.CNT FINE
V.SAW1
V.SAW2
V.SIZE.DC
V.SIZE
V.SIZE FINE
V.SIZE ADJ
QC25 CA0007A
QC09 CA0007A
PARABOLA
PARABOLA S.WAVE GEN.
S.WAVE
3.5Vpp~3.5Vpp
V.SIZE DC -3.5V~3.5V
QC06 M5218AP
QC26 DAC8840FP
QC27 DAC8840FP
QC28 DAC8840FP
V.PARA
QC29 RN1202
DC31 1SS176FA
LD20
LD22
CLK
SDI
LD21

Fig. 8-9

7. VERTICAL OUTPUT CIRCUIT

The current which is proportional to the reference waveform applied to the input portion is flown into the deflection coil to perform the vertical scanning of electron beam.

Fig. 8-10 shows the circuit construction.

The hybrid IC STK392-020 is used to the output portion and drives the vertical deflection yokes of red, green and blue respectively. The IC is composed of the differential amplifier in the first stage and the push-pull power amplifier in the final stage. The IC is considered as the power OP amp. built-in IC providing three channels.

The output portions of red, green and blue systems are the same construction and of same constant, the circuit operation is explained with reference to the output portion of green hereunder.

Pin 4 of QC10 corresponds to the + input terminal of OP amp, pin 5 to the – input terminal of OP amp. and pin 22 to the output terminal.

The green reference waveform G. REF is input to pin 4 of QC10 as the G. IN signal via the RC72.

On the other hand, the voltage which is generated at the current detection terminal RC68 of vertical deflection coil in green system is fed back to pin 5 of QC10. Pin 22 of QC10 output is connected to the vertical deflection coil in green system via PC04.

Because pin 22 of QC10 drives the vertical deflection coil so that the voltage waveform fed back to pin 5 may obtain the same shape as the waveform of pin 4, the deflection current which is proportional to the waveform of pin 4 flows into the vertical deflection coil. Further, the resistor and capacitor connected between the RC68 and pin 5 of QC10 are incorporated for the prevention of oscillation.

The power supply of the output circuit adopts the positive/negative 2 power supply system. On the positive side power supply, the voltage switching is carried out for the purpose of shortening the feedback time of the electron beam. The voltage switching is carried out by applying the blanking pulse V. BLK 2 to the gate of QC14 via QC11 to QC13, RC80 and CC25, QC14 is turned on during the feedback period and 40V is supplied. QC14 is turned off during the scanning period and 12V is supplied via DC06.

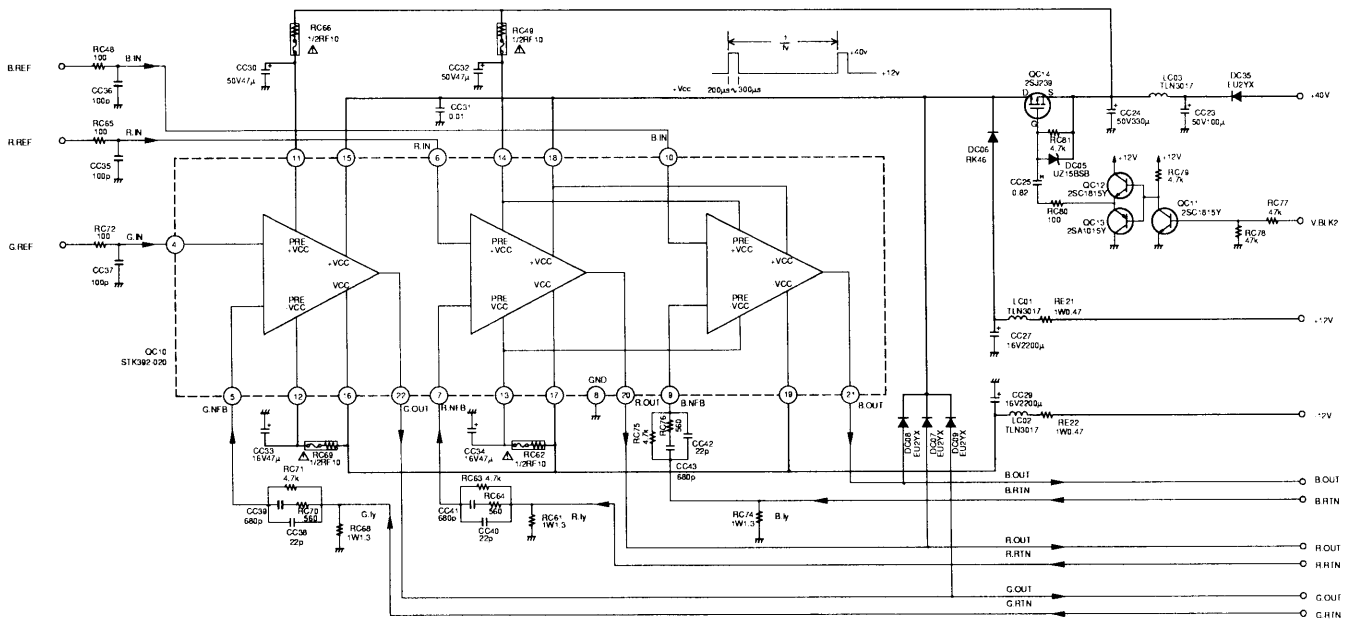


Fig. 8-10

8. VERTICAL DEFLECTION STOP PROTECTION CIRCUIT

When the deflection current is not supplied to the vertical deflection coil, one horizontal line appears on the screen. Unless this situation should last long in general TV sets, there is no problem. However, because the shadow mask is not used in the projection television, all the electron beams concentrate directly on the fluorescent screen and burn out it.

For preventing this, when one horizontal line appear on the screen, the vertical deflection stop protection circuit is operated to stop the supply of video signal so that the electron beam may not be irradiated on the fluorescent screen.

Fig. 8-11 shows the circuit construction.

The output of protection circuit is carried out by QC23, and its collector is connected to the vertical blanking circuit. This circuit detects that the deflection current stops, turns on QC23, makes the output V. BLK 2 signal of vertical blanking circuit to be HIGH level, applying the image blanking and preventing the fluorescent screen from a burning out.

The protection circuits of red, green and blue systems are of the same structure and have the same constant, so the circuit operation is explained with reference to the protective circuit of green system hereunder.

The vertical saw tooth voltage waveform G. Iy (the voltage being generated to the current detection circuit RC68) is applied to pin 6 of QC16 via RE13. When the vertical output circuit operates normally, the saw tooth waveform of 0.9 V(p-p) to 1.5 V(p-p) with 0V as its center is generated for G. Iy. The waveform is compared with the direct current voltage of 0.3V applied to pin 5, and the square pulse of vertical period is generated at pin 7 of QC16. The square pulse is input to pin 5 of the monostable multivibrator QC03 to be triggered. The time constant of output pulse G. VERT. STOP signal generated at pin 7 of QC03 is set to 38 ms longer than 1 vertical period of image receiving signal of 38 Hz to 160 Hz, and the next trigger is applied before the pulse output ends, so the pin 7 develops LOW level at all times.

Similarly, the R. VERT. STOP, B. VERT. STOP develop LOW level at all times when the vertical output circuit operates normally, and the V. STOP. PROTECT signal ORed with these diodes develops LOW level at all times, and QC23 turns off at all times.

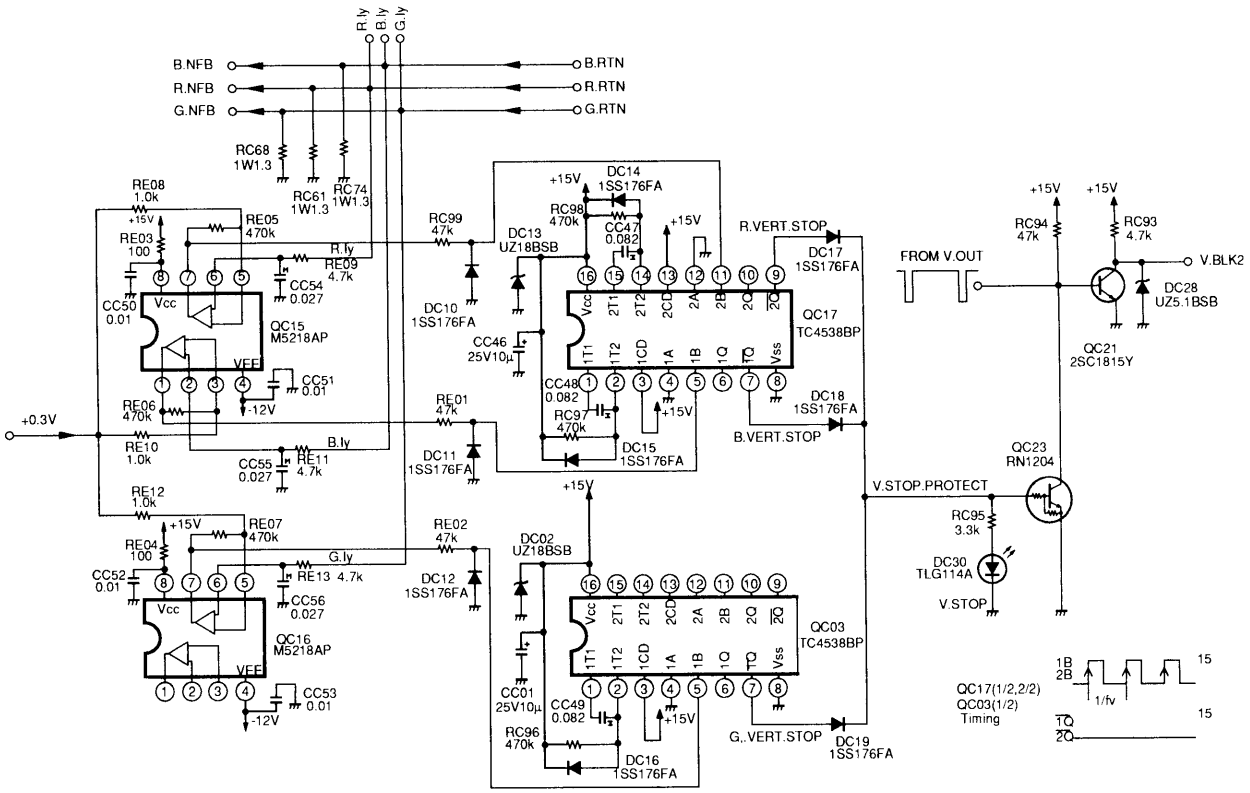


Fig. 8-11

On the other hand, when the deflection current stops, the HIGH level signal is always output to pin 7 of QC16 and the trigger can not be applied to pin 5 of QC03. G. VERT STOP signal develops HIGH level at all times, QC23 is turned on, the output V. BLK2 signal of vertical blanking circuit develops HIGH level, the video blanking signal is applied, and then the CRT stops its luminance.

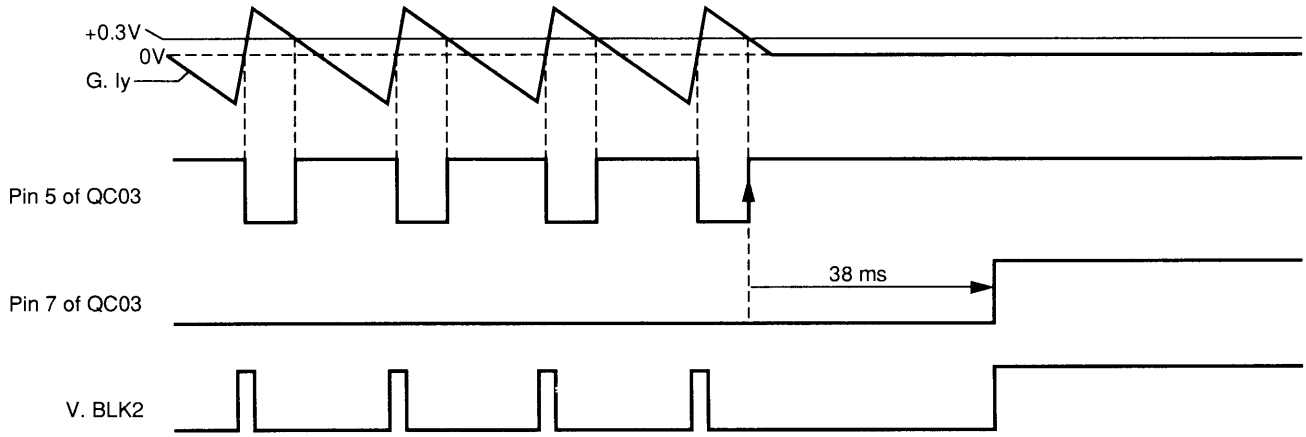


Fig. 8-12

9. VERTICAL BLANKING CIRCUIT

This circuit outputs the blanking pulse V. BLK2 which blanks the vertical retrace line.

Fig. 8-13 shows the circuit construction.

V. BLK2 signal is generated by adding the trigger signal V. BLK1 of vertical saw tooth waveform generation circuit to the blanking pulse of vertical output circuit.

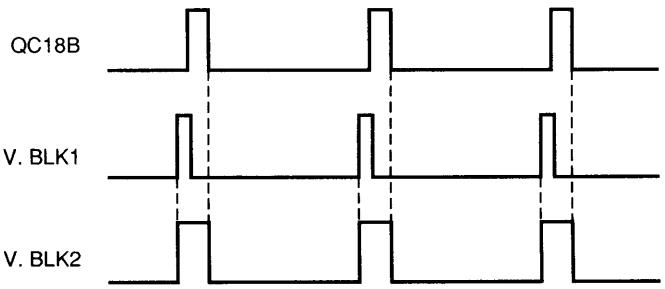


Fig. 8-14

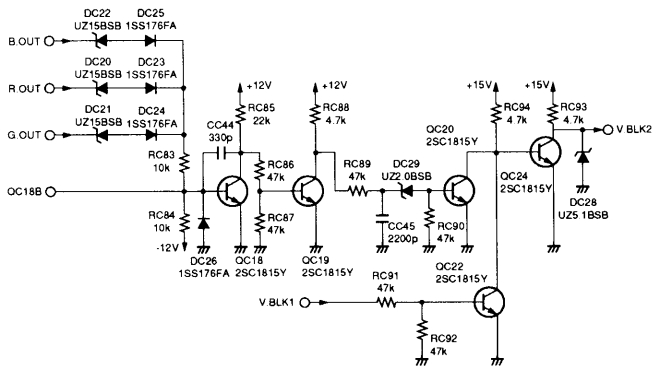


Fig. 8-13

10. OUTLINE OF HORIZONTAL OSCILLATION CIRCUIT

10-1. Features

This circuit makes the horizontal oscillation sync circuit to be the construction of multi scan correspondence in order to pull-in the input signal of horizontal frequency of 15.000 kHz to 100.0 kHz.

11. HORIZONTAL OSCILLATION SYNC CIRCUIT

Fig. 8-15 shows the construction of horizontal oscillation sync circuit.

Q410 (LA7860) is the deflection IC which performs the horizontal vertical oscillation and horizontal sync pull-in, and pins 1 to 22 are the input/ output terminals of horizontal block.

As the flow of signal, the H. SYNC pulse of 5 V(p-p) which the synchronizing separation is carried out is entered to R417, pulse-shaped into the signal with negative polarity of approx. 2 V(p-p), and input to pin 1 of Q410 (LA7860).

The sync signal is compared in phase with the AFC pulse input to pin 18, applied pulled-in sync, and output as the horizontal drive pulse from pin 16. The horizontal drive pulse is output from pin 11 through pin 4 of Q415 (MC74HC75N) latch, and sent to the horizontal output stage by the buffer.

The functions of main pins are to be explained below.

Table 8-1 Pin functions of LA7860

Pin No.	Function
1	Input terminal for the horizontal sync signal. Approx. 2 V(p-p) signal and the signal is input with the negative polarity and is triggered at the front edge of the sync signal.
2	By grounding the test pin TP01, the terminal voltage is raised up to more than 3V and the horizontal sync can be out of use.
4	The phase of horizontal sync signal input to pin 1 is delayed by this time constant. The delay time is constant.
6	The sync signal delayed by pin 4 is further delayed by this time constant. The delay time is changed by the horizontal sync frequency.
8	Control terminal for the horizontal saw tooth waveform oscillation frequency which is generated at pin 11. The oscillation frequency can be controlled the low frequency band from 13 kHz to 40 kHz and the high frequency band from 40 kHz to 100 kHz by controlling the terminal voltage from 0 to 2.5V
11	Generates the horizontal saw tooth wave.
12	Ground terminal for horizontal block.
14	Power supply terminal for horizontal block. The voltage of approx. 9V is supplied via R429.
15	Pulse duty control terminal of horizontal drive pulse of pin 16. The pulse duty of horizontal drive pulse can be varied by controlling it from 7.5 to 9V
16	Output terminal for horizontal drive pulse.
18	Input terminal for AFC pulse. The horizontal blanking pulse is passed through the phase adjustment circuit and its pulse is differentiated for its inputting.
19	Output terminal to output the identification signal whether the external horizontal sync signal input to pin 1 is synchronized with the AFC pulse input to pin 18. When the signal is synchronized, the identification result for High level (5V) is output. The output of the terminal is used as the video mute signal to erase the picture disturbance when the image reception signal is switched (horizontal non-synchronization)
22	Generates the AFC comparison saw tooth wave.

12. CONSTANT SWITCHING OF LOW FREQUENCY BAND AND HIGH FREQUENCY BAND

The horizontal sync signal frequency input to pin 1 of Q410 is ranged from 15 kHz to 100 kHz, but the entire frequency range can not be corresponded to the fixed constant owing to the specifications of LA7860.

For this reason, the frequency range is divided into 2 stages of the low frequency band from 15 kHz to 40 kHz and the high frequency band from 40 kHz to 100 kHz, and the peripheral constant of Q410 is switched according to the frequency band.

The low frequency band and the high frequency band are identified by pins 1 to 3 of Q430, and the identified signal of LOW for the low frequency band and that of HIGH for the high frequency band are output to pin 1. The identified signal is input to the analog switch control terminals of Q424 and Q425 (TC74HC4066AP) and the capacitors of C428, C430 and C441 are opened during the high frequency band.

13. H. STOP CIRCUIT

As mentioned before, when the horizontal sync frequency changes from low frequency band → high frequency band, or from high frequency bank → low frequency band, parameters associated with Q410 are switched. But a stress is given to the horizontal output circuit because the horizontal drive pulse frequency changes extremely at the switch instance. Therefore, the output of horizontal drive pulse is temporarily stopped by the H. STOP signal during the constant switching, and the output of horizontal drive pulse is restarted when the operation of Q410 peripheral circuit operation becomes stable after the constant switching ends.

The output/stop switching of horizontal drive pulse is carried out by Q414 and Q415 using the H. STOP signal. The H. STOP signal is generated by Q432 and Q439 using the frequency band identification signal (pin 1 of Q430) explained in the preceding paragraph, and the LOW pulse (fixed to HIGH level during the steady state) for approx. 1.5 seconds is generated in the collector of Q439 during the constant switching.

The horizontal drive pulse output from pin 16 of Q410 is input to pin 6 of Q415 (MC74HC75N). In the steady state, since the HIGH level signal is applied to pin 4 (G3) which is the output control terminal of Q415 via Q414, the signal input to pin 6 is output to pin 11 as it is. On the other hand, when the H. STOP signal develops LOW during the constant switching, the LOW level signal is applied to pin 4 of Q415 and Q415 enters the hold mode, and hence, pin 11 of output is kept to a constant level of HIGH, thereby the horizontal output circuit stops its operation.

What's more, the output control of Q415 is not carried out directly by the STOP signal, but synchronizes the switching timing of horizontal drive pulse generation stop with the rising edge of the horizontal drive pulse by once inputting the H. STOP signal into the flip flop of Q414 (TC74HC74AP), generating the control signal to pins 5 and 6, which is timing- synchronized to the rising edge of the horizontal drive pulse, and by controlling the output of Q415 with the control signal.

14. CONTROL VOLTAGE OF HORIZONTAL OSCILLATION FREQUENCY

The control voltage of horizontal oscillation frequency input to pin 8 of Q410 (LA7860) is controlled by the horizontal F-V conversion voltage. The horizontal F-V conversion voltage in the low frequency band has a small voltage value, and hence it is amplified to approx. 2.5 times through the amplification circuit of Q413, and the voltage is switched between the low frequency band and high frequency band by the analog switch of Q424 (TC74HC4066AP). The horizontal F-V conversion voltage is converted by the level shift circuit Q411, and then input to pin 8 of Q410 so that the free-run frequency may automatically pursue the input signal frequency. The voltage value input into pin 8 is approx. 0.3V with the fH = 15 kHz and approx. 1.8V with the fH = 31 kHz which are the low frequency band, and is approx. 1.0V with the fH = 60 kHz and approx. 2.0V with the fH = 90 kHz which are the high frequency band.

15. HORIZONTAL DRIVE PULSE DUTY CONTROL VOLTAGE

The horizontal drive pulse duty control voltage input to pin 15 of Q410 (LA7860) is converted into the horizontal F-V conversion voltage by the R446, R447, R448 and R449, and is input through the buffer of Q413.

The voltage value input into pin 15 is approx. 8.1V when fH = 15 kHz with approx. 43% of the horizontal drive pulse duty and is approx. 8.4V when fH = 60 kHz with approx. 52% of the horizontal drive pulse duty.

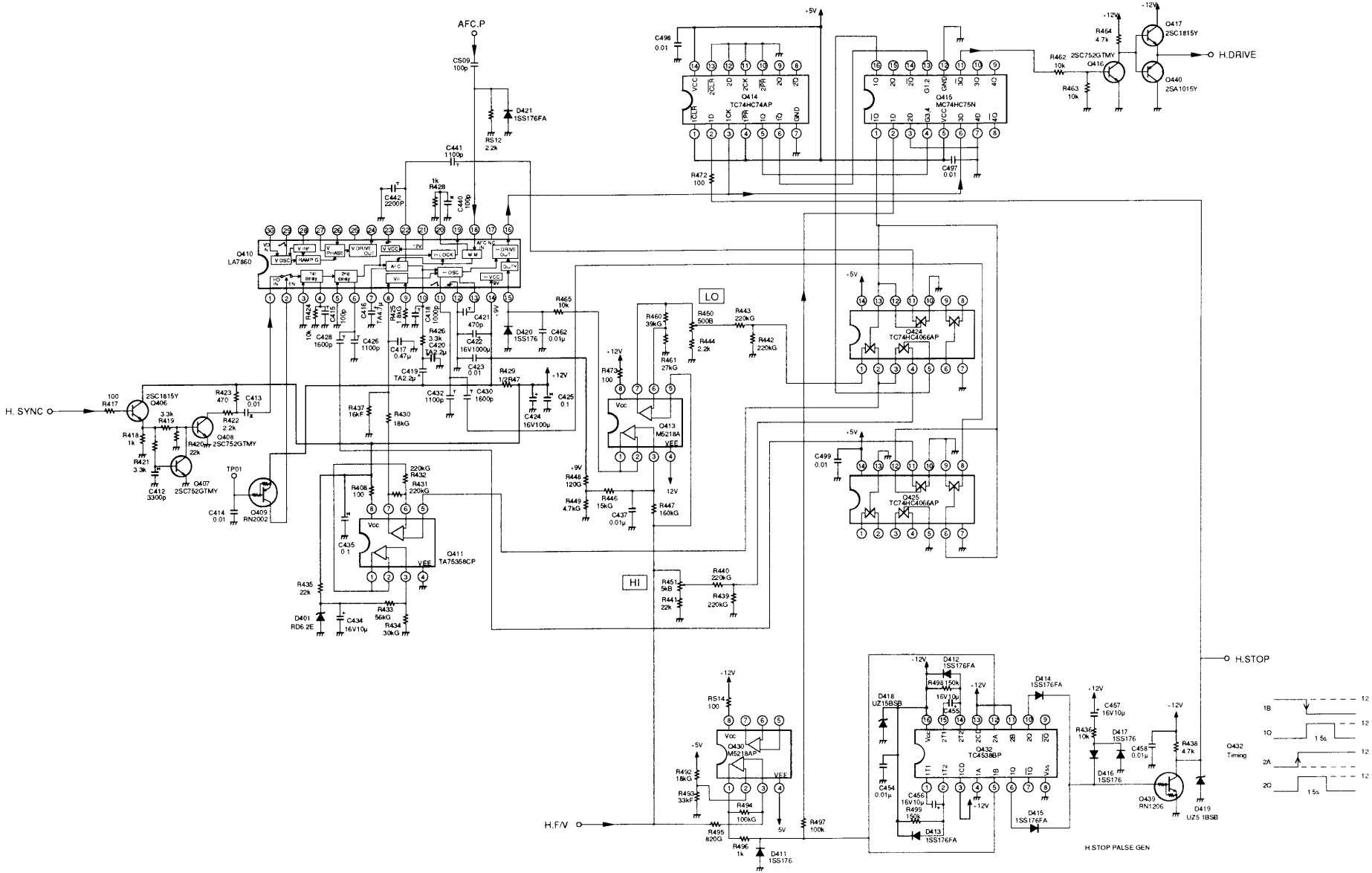

AFC.P
H. SYNC
H.F/V
H.DRIVE
H.STOP
H.STOP PALSE GEN
LO
HI
Q410 LA7860
Q411 TA75358CP
Q414 TC74HC74AP
Q415 MC74HC75N
Q424 TC74HC4066AP
Q425 TC74HC4066AP
Q430 M5218AP
Q432 TC4538BP
Q413 M5218A
Q416 2SC752GTMY
Q417 2SC1815Y
Q440 2SA1015Y
Q406 2SC1815Y
Q407 2SC752GTMY
Q408 2SC752GTMY
Q409 RN2002
Q439 RN1206
+5V
+12V
+9V
-12V
Timing
1S
1.5s

Fig. 8-15

16. HORIZONTAL PHASE ADJUSTMENT CIRCUIT

Fig. 8-16 shows the circuit construction.

This circuit outputs the pseudo blanking pulse HPC. P whose phase is adjusted to the blanking pulse H. BLK generated at the horizontal output block.

The same circuit construction as that of the vertical phase adjustment block is employed, and makes the horizontal phase variable by delaying the AFC.P by approx. 1 horizontal cycle against the H. BLK using two stages of monostable multivibrator and by finely adjusting the delay time.

For the circuit operation, refer to the item of vertical phase adjustment circuit.

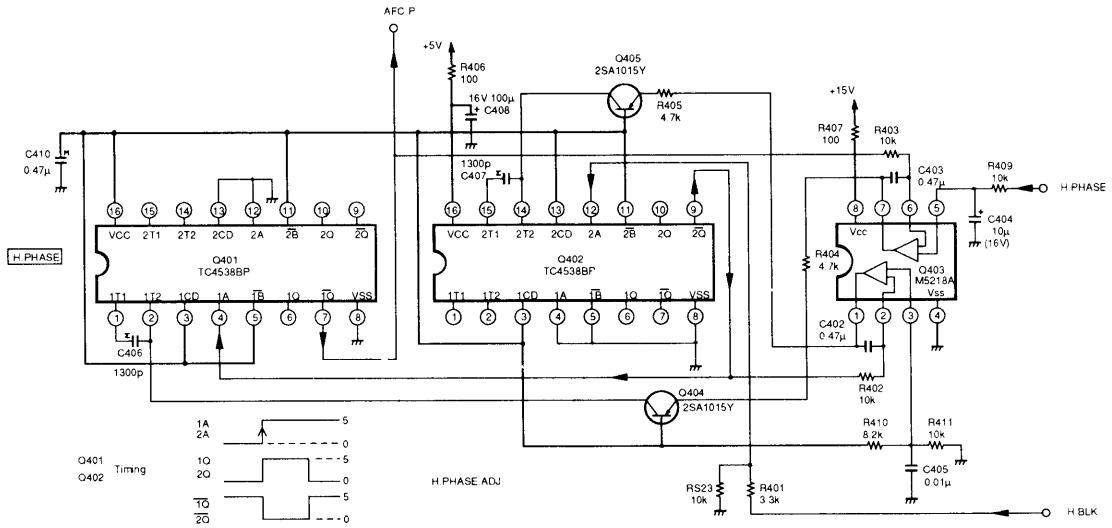


Fig. 8-16

17. HORIZONTAL F/V CONVERSION CIRCUIT

This circuit outputs the direct current voltage proportional to the horizontal frequency of image receiving signal. Hereunder, the direct current voltage is called the H. F/V voltage (horizontal F/V voltage).

The control of horizontal oscillation frequency and the rough control of horizontal amplitude are carried out using the H. F/V voltage.

Fig. 8-17 shows the circuit construction.

The horizontal sync signal H. SYNC is input to pin 6 of Q428 via Q447. Q428 is generally called the F/V conversion IC, and the direct current voltage proportional to the input signal frequency of pin 6 is output to pin 1. The voltage at pin 1 is input to pin 3 of Q429 via the low pass filter consisting of RS18 and CS16 and output from pin 1 as the H. F/V voltage.

For information, the circuit composed of Q441 and Q442 triggers the vertical sync signal V. SYNC and outputs the pulse of approx. 0.15 x Tv (Tv is the time of 1 vertical cycle) before and after the V. SYNC, and the horizontal F/V conversion operation is stopped for the period before and after the V. SYNC using this output pulse. By employing this kind of construction, an error is prevented from appearing to the H. F/V voltage by the influence of the cut-in pulse and equalizing pulse which are superimposed on the H. SYNC signal.

Supposing the frequency of H. SYNC as f_H (kHz) and the H. F/V voltage as $V_{H.F/V}$, the following relational equations are obtained.

$$V_{H.F/V} = 0.08 \times f_H \quad (12.5 \leqq f_H \leqq 100)$$

$$V_{H.F/V} = 1.0 \times f_H \quad (f_H < 12.5)$$

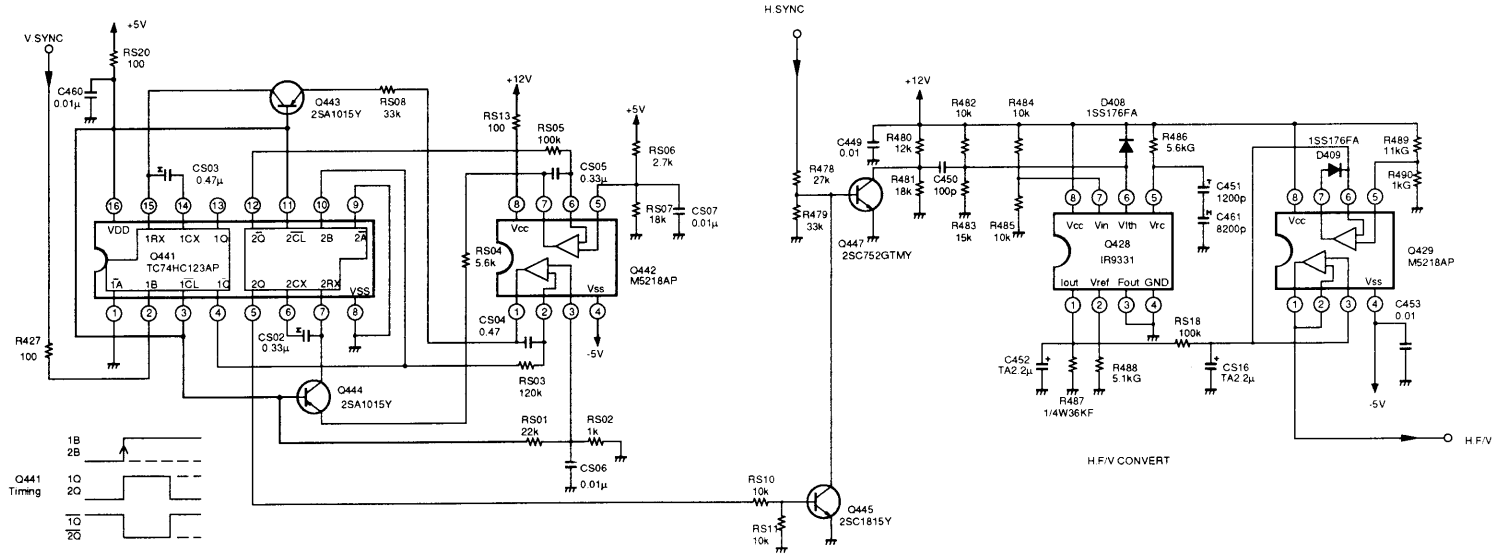

V.SYNC
+5V
RS20
100
C460
0.01µ
Q443
2SA1015Y
RS08
33k
+12V
RS13
100
RS05
100k
+5V
RS06
2.7k
CS03
0.47µ
CS05
0.33µ
RS07
18k
CS07
0.01µ
VDD
1RX
1CX
1Q
2Q
2CL
2B
2A
Q441
TC74HC123AP
1A
1B
1CL
1Q
2Q
2CX
2RX
VSS
Vcc
Vss
Q442
M5218AP
RS04
5.6k
CS04
0.47
-5V
R427
100
CS02
0.33µ
Q444
2SA1015Y
RS03
120k
RS01
22k
RS02
1k
CS06
0.01µ
1B
2B
Q441
Timing
1Q
2Q
1Q
2Q
H.SYNC
RS10
10k
RS11
10k
Q445
2SC1815Y
+12V
R482
10k
R484
10k
D408
1SS176FA
C449
0.01
R480
12k
R486
5.6kG
1SS176FA
D409
R489
11kG
R490
1kG
R478
27k
R481
18k
C450
100p
R483
15k
R485
10k
R479
33k
Q447
2SC752GTMY
C451
1200p
C461
8200p
Vcc
Vin
Vth
Vrc
Q428
IR9331
Iout
Vref
Fout
GND
Vcc
Vss
Q429
M5218AP
C453
0.01
RS18
100k
C452
TA2.2µ
R488
5.1kG
CS16
TA2.2µ
R487
1/4W36KF
-5V
H.F/V
H.F/V CONVERT

Fig. 8-17

SECTION IX
HORIZONTAL FOCUS OUTPUT CIRCUIT

1. OUTLINE

The electron beam in the projection cathode ray tube is swept horizontally by the horizontal deflection coil. In this case, the distance of electron beam (the distance from the electron gun to the fluorescent body) reaching the central portion of projection cathode ray tube differs from that of electron beam reaching the left end or right edge of projection cathode ray tube.

For this reason, to obtain the optimum focus performance on the entire tube face of projection cathode ray tube, the horizontal dynamic focus circuit is provided. (The vertical dynamic focus circuit described in section 10 is also provided for the similar reason).

Because the electron beam is focused by the magnetic force, the parabolic current synchronizing with the horizontal sweep signal is flown into the dynamic coil built-in inside the focus magnet to perform the horizontal dynamic focus, and the magnet force varies synchronizing with the horizontal sweep. The correction signal uses the parabolic voltage of horizontal cycle which is generated by the CONV/FOCUS unit. This circuit amplifies the input signal and supplies it to the dynamic coil.

2. DESCRIPTION OF OPERATION

Three output circuits are provided so that the electron beam may be supplied to the focus magnets existing in the projection cathode ray tubes of red, blue and green respectively. However, as the circuit element, the single hybrid IC (QF01) built-in 3 amplifiers is used.

The horizontal parabolic signal input is input to the inverted signal input terminal pin 3 of OP amp. QF11 via the RF73. The output is divided into 3 at pin 1 and input to pins 4, 6 and 10 of QF01 via the resistor, etc. The QF01 can be imagined that it contains 3 OP amp. that can supply large power. The function of each pin is listed in Table 9-1.

As the operation of 3 circuits is the same, the operation is explained with the circuit consisting of pins 4, 5 and 22 of QF01. In addition, 40V is applied to +Vcc, and –40V is applied to –Vcc. The input signal is applied to non inverted input of pin 4 of QF01. The output current passes through the feedback resistor RF12 via the dynamic coil and flows to the ground.

The voltage proportional to the output current is developed at both ends of RF12 and is fed back to pin 5 (inverted input terminal) of QF01.

Since the feedback signal is applied to pins 4 and 5 of QF01, the same voltage is developed at pins 4 and 5. Namely, the circuit operates in such that the voltage identical to the input voltage may be applied to the feedback resistor RF12. The value of the output current I_O becomes equal to the value of which Vi is divided by the resistance value of RF12.

Since the load of dynamic focus output circuit consists mainly of the inductance component, the input voltage waveform is not similar to the output voltage waveform. The waveform of the voltage necessary to flow the current to the inductance component is equal to that of current differentiated. Since the input voltage waveform shows a parabolic waveform, the output voltage waveform becomes a saw tooth waveform because of the reason above.

RF09 is the damping resistance of dynamic coil and prevents the generation of unnecessary ringing.

Table 9-1

Pin No.	Function	Pin No.	Function
1	NC	11	+Vcc
2	NC	12	–Vcc
3	NC	13	–Vcc
4	CH1 non inverted input	14	+Vcc
		15	+Vcc
5	CH1 inverted input	16	–Vcc
6	CH2 non inverted input	17	–Vcc
		18	+Vcc
7	CH2 inverted input	19	–Vcc
8	Ground	20	CH2 output
9	CH3 inverted input	21	CH3 output
		22	CH1 output
10	CH3 non inverted input		

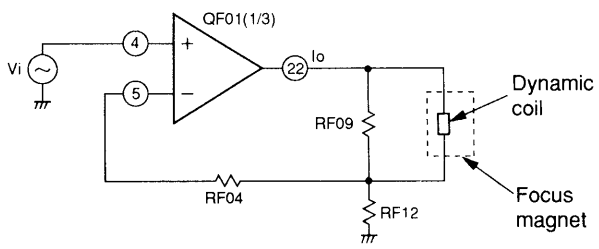


Fig. 9-1

SECTION X
CONVERGENCE CIRCUIT
(CONV/FOCUS PC BOARD)

1. OUTLINE

The convergence circuit has the function to adjust the color deviation of three primary color image of red, green and blue which are projected in expansion on the screen. This circuit also has the function to adjust the distortion of image.

The convergence circuit of P7300U adopts the analog system, and has the features as follows .

1-1. The precision Adjustment is Available

The adjusting order both in the convergence and picture distortion are specified, and the positions of 25 points on the screen shown in Fig. 10-1 can be precisely adjusted.

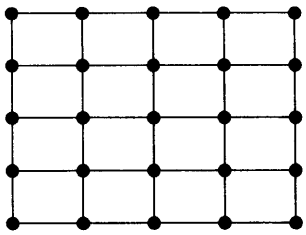


Fig. 10-1

1-2. Easy to Adjust

Since the adjustment can be performed with the feeling like adjusting the convergence of digital system by the remote control operation, no skill is required for the adjustment.

1-3. Simplification of Adjustment Work

The number of maximum input signal sources of P7300U is 30 kinds, and 7 kinds alone need to be adjusted according to the horizontal sync frequency for the convergence. Hence, the trouble for the adjustment for every input signal source can be saved.

The convergence adjusting data bank is provided with 7 banks. Since the data copy function between the banks is provided, it is possible to simplize the adjusting operations.

1-4. Picture Size Pursuit System

The convergence hardly gets deviated even after adjusting the picture to the desired picture size for every input signal source. Therefore, it is not necessary to readjust the convergence every time when changing the picture size as it is in the digital convergence system.

2. DESCRIPTION OF CIRCUIT OPERATION

2-1. Horizontal Timing Correction Circuit

The horizontal period convergence correction signal delays for a slight time in the signal processing process of circuit. The horizontal timing correction circuit corrects the time delay.

Q713a is the monostable multivibrator, is triggered at the front edge H. BLK (Horizontal Blanking Pulse) input to pin 2, and the pulse of width determined by the time constant of R724 and C715 is output to pin 13. The pulse width of the output pulse is approx. 1 μs (Typ.) wider than that of H. BLK.

On the other hand, the H. BLK is also input to pin 9 of Q713b, and triggers Q713b at the back edge of H. BLK. The pulse width of the pulse output from pin 5 of Q713b is determined by the collector current of transistor Q714 and the static current capacitance of C723. The OP amp. Q725b controls the collector current of Q714 to obtain the average value of pulse voltage output to pin 13 of Q713a and the average value of pulse voltage output to pin 12 of Q713b.

As a result, the t_1 equals to t_2 shown in Fig. 10-2, and the front edge of HD pulse output to pin 5 of Q713 advances by the time Δt or 1 μs (Typ.) more than the front edge of H. BLK. The timing pulse generated by differentiating the HD pulse with C717 and R725 is added to pin 4 of Q708a.

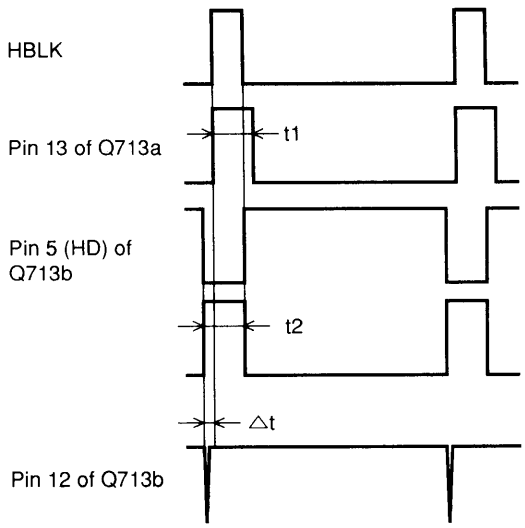


Fig. 10-2

2-2. Horizontal Saw-tooth Waveform Voltage H1 Generation Circuit

When the timing pulse explained in the preceding item is applied to pin 4 of R – S flip-flop Q708a, pin 5 develops H level (Logic Level "H") and pin 6 develops L level (Logic Level "L"). Thereby, the analog switch Q715d is turned on and Q715c is turned off.

The OP amp. Q716b and C719 build up the integration circuit. When Q715d is turned on, the negative integration current is supplied via R731 from the –5V power supply, and the output terminal voltage of Q716b goes up linearly. When the output terminal voltage of Q716b goes up and exceeds the direct current voltage level V_3 applied to pin 3 of comparator Q718, pin 7 (output terminal) of Q718 develops H level and pin 6 (output terminal) of inverter gate Q710c develops L level. As a result, Q708a is reset, pin 5 (output terminal) develops L level and pin 6 (output terminal) develops H level, thus turning on Q715c and turning off Q715d.

The direct current voltage HFV proportional to the horizontal sync frequency is divided by R763 and R764 and applied to pin 3 of OP amp. Q725a. The HFV is supplied from the control circuit (CONTROL PC board).

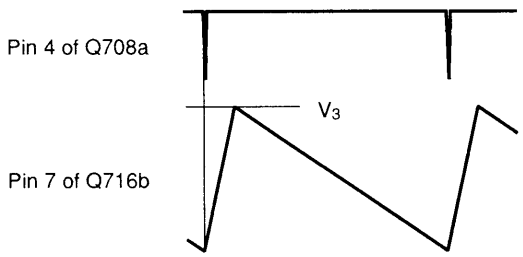


Fig. 10-3

When Q715c is turned on, the positive integration current is supplied via R755 from the output terminal of Q725a, and the output voltage of Q716b linearly descends. This operation continued for the period when the next timing pulse is applied. Because the timing pulse is the horizontal period pulse, the horizontal period saw tooth wave voltage can be obtained to the output terminal of Q716b. Because the saw tooth wave voltage obtained to the output terminal of Q716b contains the direct current offset voltage constituent, it is removed by C718 and output as H1 via the buffer by the operational amplifier Q716a.

H1 output to the output terminal of Q716a is half wave rectified with the wave detection circuit composed of the OP amp. Q711a and D703, D704, R741 and R742.

As a result, the voltage of waveform shown in the thick solid line in Fig. 10-4 can be obtained to the connection point of D703 and R741. This voltage is converted to the direct current voltage with the filter circuit consisting of R740 and C721 and output via the buffer by the OP amp. Q711b.

The direct current output from Q711b becomes Vpp/8 supposing the amplitude of H1 output from Q716a as Vpp. This voltage is input to the differential amplifier circuit consisting of the OP amp. Q712b, compared with the reference voltage V_{REF} applied to pin 5 and outputs the AGC voltage to the output terminal pin 7.

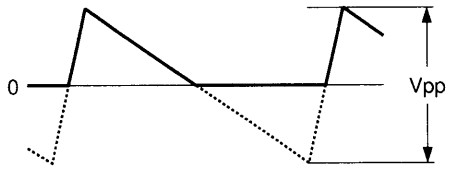


Fig. 10-4

The AGC output voltage is fed back to the integration circuit by R750 and then controls the charged current so as to make V_{REF} = Vpp/8. The V_{REF} is 0.5 V(Typ.), and the amplitude V(p-p) of H1 becomes 4 V(p-p)(Typ.).

The V_{REF} is changed by the control voltage HSIZE for adjusting the horizontal size of screen. Namely, when adjusting the horizontal size, the V_{REF} is interlock controlled and changes the amplitude of H1 at the same time. By this operation, the convergence is prevented from deviating even if the horizontal size is changed.

2-3. Horizontal Parabolic Wave Voltage H2 Generation Circuit

The horizontal parabolic wave voltage H2 is basically formed by squaring the horizontal saw tooth wave voltage.

Q723a is the analog multiplier, which multiplies the voltage input to the input terminals 4 and 5 and outputs to pin 6. The scale factor in case of the multiplication is 0.5, and for example, suppose two input voltages as 2V, then the output voltage will be 2 x 2 x 0.5 = 2V.

During the retrace period tr, the analog switch Q715a is turned on, and makes the input voltage of Q723a to be the direct current voltage forcibly output from Q712a. As a result, the waveform of voltage input to the input terminal pins 4 and 5 of Q723a becomes as shown in Fig. 10-5.

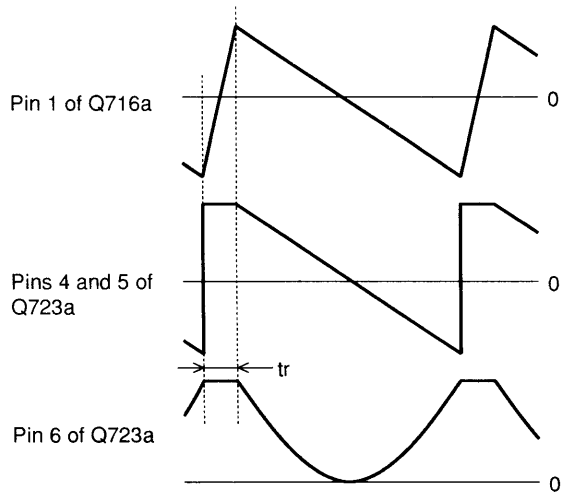


Fig. 10-5

By squaring this voltage with Q723a, the parabolic wave voltage whose retrace period is flat as shown in Fig. 10-5 can be obtained to the output terminal pin 6.

Why flattening the retrace period in this way is to prevent the waveform distortion in the later processing circuit. For information, in the actual operation waveform, the retrace period is distorted more than the ideal waveform shown in Fig. 10-5.

The input impedance of analog multiplier becomes a comparatively low value at 20 k ohm (Typ.).

As a result, because the amplitude of parabolic wave voltage obtained to the output terminal is decreased, which is amplified by the OP amp. Q754b, and the parabolic wave voltage H2 of about 2V(p-p)(Typ.) is obtained to the output terminal pin 7.

2-4. Horizontal S-character Wave Voltage H3 Generation Circuit

The horizontal S-character wave voltage H3 is formed by adding the horizontal saw tooth wave voltage H1 to the input terminal 11 of analog multiplier Q723b and adding the horizontal parabolic wave voltage H2 to the input terminal and by multiplying both the voltages.

The retrace period of H2 obtained to the output terminal of Q754b at this time is clamped to zero potential by the analog switch Q715b and then input to Q723b. As a result, the S-character wave voltage whose retrace period is in zero potential is output as shown in Fig. 10-6 to the output terminal pin 9 of Q723b. The S-character wave voltage output from Q723b is amplified with the OP amp. Q755a, and output as H3 with the amplitude of about 3.7 V(p-p)(Typ.).

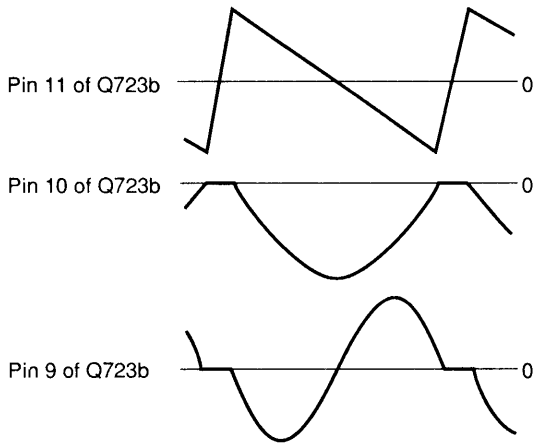


Fig. 10-6

2-5. Vertical Saw Tooth Wave Voltage V1 Generation Circuit

The vertical saw tooth wave voltage V1 is formed in the similar method to the horizontal saw tooth wave voltage H1 explained in item 2-2, but the differences are explained hereunder.

Because the frequency is low in case of the vertical period circuit, the time delay in the signal processing process doesn't become any problem. Therefore, there is no timing correction circuit, and the VBLK (Vertical Blanking Pulse) is used, as it is, as the timing pulse.

In the horizontal saw tooth wave voltage generation circuit, the amplitude of H1 is stabilized and interlocked to the horizontal size adjustment using the AGC circuit, but the AGC circuit isn't used here.

In the vertical saw tooth wave voltage generation circuit, the integration circuit is structured of the OP amp. Q703a and C711. The analog switches to supply the charging/discharging current to the integration circuit are Q707d and Q707c, and the voltage source is output from Q706a and Q706b.

The direct current voltage of positive polarity proportional to the vertical frequency is output to the output terminal of Q706a, and the direct current voltage of negative polarity whose polarity is inverted is output to the output terminal of Q706b.

In other words, in case of the vertical saw tooth wave voltage generation circuit, both the charging and discharging currents become proportional to the vertical frequency, so the amplitude of saw tooth wave voltage obtained to the output terminal of Q703a becomes constant even if the frequency varies.

Instead, the retrace time of obtained saw tooth wave voltage changes inversely proportion to the frequency, but in case of the vertical voltage, the change of retrace time doesn't become problem. (In case of the horizontal voltage, the retrace time is set to the constant value because it has an influence on the dynamic range of convergence output circuit). The interlock operation of saw tooth wave voltage when adjusting the vertical size is realized by the analog multiplier Q705a. The saw tooth voltage output from Q703a is applied to the input terminal pin 4 of Q705a, and the direct current voltage varying with the control voltage VSIZE when adjusting the vertical size is applied to the input terminal pin 5 from Q703b.

As a result, the saw tooth voltage whose amplitude varies according to the adjustment of vertical size can be obtained to the output terminal pin 6 of Q705a. The saw tooth voltage output from Q705a is output as V1 with the amplitude of 4 V(p-p) (Typ.) via the buffer by the OP amp. Q705c.

For information, Q705c is the OP amp. incorporated into the CA0007AD, but this OP amp. is less in the negative output current (sink current) as compared with the general OP amp, so RR29 is additionally connected for supplementing the current. Q705c may be replaced with the OP amp. of another circuit portion in future.

2-6. Vertical Parabolic Wave Voltage V2 Generation Circuit

The vertical parabolic wave voltage V2 is formed with quite the same principle as that of horizontal parabolic wave voltage generation circuit explained in the preceding item 2-3.

During the retrace period, the saw tooth voltage is replaced with the direct current voltage using the analog switch Q707b similarly to the case of horizontal voltage. In case of the vertical voltage, the buffer by OP amp. Q754a is provided for compensating the reduction of level due to the analog multiplier Q705b.

The parabolic wave voltage that was formed by squaring the saw tooth wave voltage is obtained to the output terminal pin 9 of Q705b, and is output as V2 via the buffer by the ope. amplifier Q753b.

2-7. Vertical S-character Wave Voltage V3 Generation Circuit

The vertical S-character wave voltage V3 is formed by applying V1 to the input terminal 11 of analog multiplier Q720b, applying V2 to the input terminal 10 and by multiplying both the voltages.

In this case, the retrace period of parabolic wave voltage obtained to the output terminal of Q753b is clamped to zero potential with the analog switch Q707a similarly to the case of horizontal voltage, and then input to Q720b. As a result, the S-character wave voltage whose retrace period is zero potential is output to the output terminal pin 9 of Q720b. The S-character wave voltage output from Q720b is amplified with the OP amp. Q753a and is output as V3 with the amplitude of about 4.0 V(p-p) (Typ.).

2-8. Signal Modulation Circuit

The five systems of signal modulation (multiplication) circuit are provided for adjusting various picture distortions and convergence.

(1) Analog multiplier Q722b creates V1H3 by multiplying V1 and H3 and the OP amp. Q756a amplifies it up to 4.5V(p-p) (typical value) and outputs.

Fig. 10-7

(2) Analog multiplier Q721a creates V3H3 by multiplying V3 and H3 and the OP amp. Q756b amplifies it up to 4.5V(p-p) (typical value) and outputs.

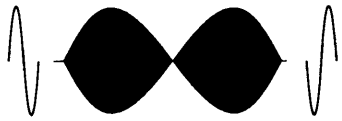


Fig. 10-8

(3) Analog multiplier Q721b creates V1H1 by multiplying V3 and H1 and the OP amp. Q757b amplifies it up to 4.5V(p-p) (typical value) and outputs.

Fig. 10-9

(4) Analog multiplier Q720a creates V3H1 by multiplying V3 and H1 and the OP amp. Q756a amplifies it up to 4.5V(p-p) (typical value) and outputs.

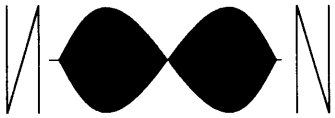


Fig. 10-10

Two pieces off-set adjustments are added to the 4 system modulation circuits respectively, but this function is explained with reference to the circuit forming the V1H3. The variable resistor (rheostat) RP90 adjusts the direct current offset voltage of V1 to be input to Q722b. By this adjustment, the cross point timing of V1H3 waveform changes. In this adjustment, the cross point timing should be set to the center of vertical scanning period. (Refer to Fig. 10-11.)

The variable resistor PR89 adjusts the direct current level of V1H3 waveform. By this adjustment, the cross point should be set to DC0V. (Refer to Fig. 10-12.)

During this offset adjustment, the accuracy of V1H1 needs to be raised highest. If this accuracy should be insufficient, there may be the case where the horizontal stripes appear around the center in vertical direction of picture. The off-set adjustment of the other 3 kinds of signals will possibly be deleted in the future because it has no great influence on the picture.

The 5th system signal modulation circuit using the analog multiplier Q722a is to be explained on the next item.

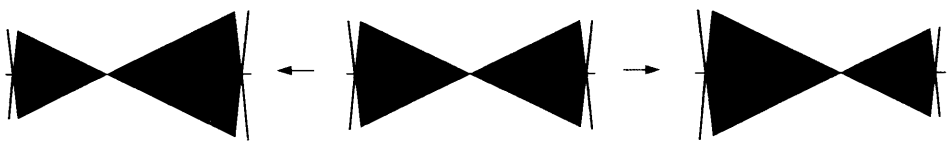


Fig. 10-11

Fig. 10-12

2-9. Picture Distortion Correction Circuit

There are pincushion distortion, keystone distortion, etc. to the typical picture distortion of projector. The linearity distortion 1 (Linearity), linearity distortion 2 (Inside Size), tilt distortion (Tilt), bow distortion (Bow), etc. can be adjusted besides the said distortions in P7300U. Here explained are the correction circuits of pincushion distortion, keystone distortion and linearity distortion 2.

Q728 (DAC8840) is the 8-channel, 8-bits, 4-quadrant multiplication type DAC, and has the function of adjusting the individual signal voltage levels input to the input terminals AI to HI by the 8-bits serial data SDI and outputting the respective levels to the output terminals AO to HO. The output voltage can be adjusted to an optional value (however, 256 steps) within the range of –V to V against the input voltage V.

Upper and lower side keystone distortion can be adjusted by inputting V1H1 to the DAC of Q728A, B, C.

The red is assigned to DAC-A, the green to DAC-B and the blue to DAC-C, and the output signal of respective DACs are applied to the vertical convergence circuits of red, green and blue. Further, when the Green was adjusted, the Red and Blue move simultaneously.

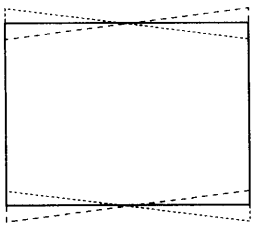


Fig. 10-13

The side keystone distortion can be adjusted by inputting V1 to the DAC-D of Q728. The side pindushion distortion can also be adjusted by inputting V2 to the DAC-F of Q728.

The output signals of DAC-D and DAC-F are supplied to the horizontal deflection circuit and not to the convergence circuit, for adjusting 2 kinds of picture distortion of left and right. During the adjustment of 2 kinds of picture distortion of left and right, the red, green and blue colors move simultaneously.

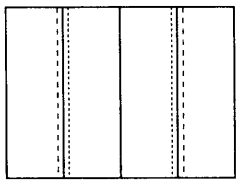


Fig. 10-14

The linearity distortion 2 (Inside Size) can be adjust by inputting H3 to the DAC-H of Q728. The output signal of DAC-H is applied to the horizontal convergence circuit of red, green and blue, and 3 colors move simultaneously during the adjustment (Fig. 10-14). For reference, the adjustment circuit in vertical direction resides in the DEF PC board.

The top/bottom pincushion distortion can be basically corrected with the signal voltage which multiplied V1 with H2. In case of the projector, it is general that the projection angle in vertical direction against the screen is not a right angle. Then, there appears the optical magnification difference between the upper side and the lower side of screen, and the pincushion distortion becomes unbalance between the upper side and the lower side if it should be simply corrected with V1 x H2. Therefore, the top/bottom pincushion distortion correction circuit of P7300U makes it possible to adjust the top/bottom balance.

The V1 is applied to the input terminal pin 6 of OP amp. Q755b via the RP98 and moreover the output signal of DAC-G of Q728 is also applied to the said terminal via the RP97. Because the V2 is input to the DAC-G, the signal voltage which is inverted and amplified with the V1 + V2 can be obtained to the output terminal of Q755b. At this time, because the V2 can be made an optional polarity and an optional level depending on the adjustment method of DAC-G, the output terminal voltage wavefrom of Q755b changes variously as shown in Fig. 10-15.

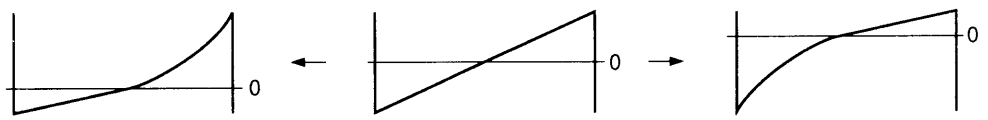


Fig. 10-15

Since the analog multiplier Q722a multiplies the output voltage of Q755b with H2, its output voltage waveform becomes as shown in Fig. 10-16. In the waveform in the center figure, the electric distortion correction sizes in the upper and lower sides of screen become equal, but in the waveform in the left figure the correction size of screen lower side becomes greater while in the waveform in the right figure the correction size of screen upper side becomes greater. That is to say, the balance of upper and lower sides can be adjusted by the DAC-G.

The output voltage of Q722a is input into the DAC-E of Q728. The output voltage of DAC-E is applied to the vertical convergence circuit of red, green and blue. By adjusting the DAC-E, the correction size of top/bottom pincushion distortion can be changed with the balance correction added. During this adjustment, the red, green and blue colors simultaneously move.

2-10. Signal Dividing Circuit

For adjusting the convergence partially on the screen, various signal voltages need to be divided in correspondence to the screen position. The screen position has the relation with the scanning timing, and for example, the upper half portion of screen is the first half of vertical scanning whereas the left half portion is the first half of horizontal scanning. Therefore, if various signal voltages should be divided into the first half and latter half of scanning, the independent adjustment becomes possible for every place of screen.

The signal for discriminating the first half and latter half of scanning is formed by the comparators Q704a and Q717. Any of the comparators works as the zero cross comparator, the vertical saw tooth wave voltage V1 is input to the input terminal pin 3 of Q704a while the horizontal saw tooth voltage H1 is input to the input terminal pin 2 of Q717. Because both the V1 and H1 are the signals which become the positive polarity potential in the first half of scanning, the signal becoming the H level and the signal becoming the L level can be obtained in the first half and the latter half respectively of scanning to the output terminals of respective comparators. (Fig. 10-17)

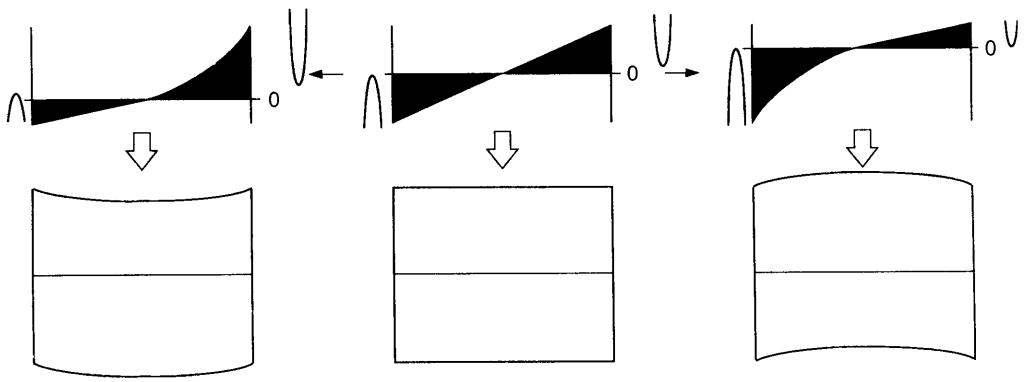


Fig. 10-16

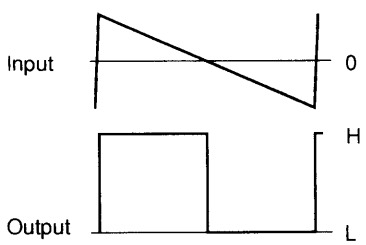


Fig. 10-17

The signal of vertical cycle output from Q704a has no casual sequence with the horizontal scanning. If this signal should be used as it is, the signal is divided with an optional timing of horizontal scanning though it is the center of vertical scanning, causing a trouble to the screen in some cases. Therefore, the level is inverse during the horizontal retrace period by the flip flop Q709. (Fig. 10-18)

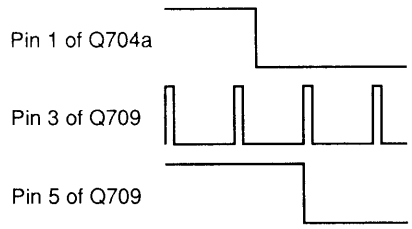


Fig. 10-18

4 kinds of modulation signal voltages, namely, V1H3, V3H3, V1H1 and V3H1 use the analog multiplexer 74HC4052 (Q724, Q719). The 74HC4052 is the IC working as the 2-circuit 4-contact switch, and controls the switch which is turned on by the logic level of signal input to pins A and B (10 and 9). The operation modes are as listed in table 10-1.

Table 10-1

A	B	On Switch
L	L	X0, Y0
H	L	X1, Y1
L	H	X2, Y2
H	H	X3, Y3

The division control signal of vertical cycle output from Q709 is applied to the A-terminal of Q724 and Q719, and the division control signal of horizontal cycle output from Q717 is applied to the B-terminal. Comparing the logic levels of these two signals with the said table, it can be known, for example, that the switches X3 and Y3 are turned on and output the modulation signal voltages to the first half of vertical scanning and moreover to the first half of horizontal scanning. The first half of vertical scanning and moreover the first half of horizontal scanning fall under the left above zone of screen.

Namely, it can be known the left above zone can be adjusted by adjusting the convergence with the signals output from the switches X3 and Y3. In the similar manner, the right above zone can be adjusted by the signals output from the switches X1 and Y1, the right lower zone by the signals output from X0 and Y0, the left lower zone by the signals output from X2 and Y2. (Refer to Fig. 10-19.)

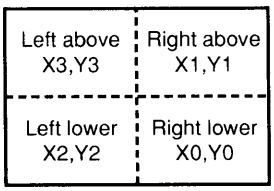


Fig. 10-19

The V3 and H3 are the wave detecting circuits (wave detectors) and divide the screen into the first half and latter half of scanning. V3 is divided into signal voltages for a first half scanning and a later half scanning by the detection circuit consisting of Q721c, D707, D708 and the other detection circuit consisting of Q720c, D705, D706. H3 is divided into signal voltages for a first half scanning and a later half scanning by the detection circuit consisting of Q762, Q761, Q760, and the other detection circuit consisting of Q759, Q758, Q763, and are output via the buffer by Q723c and Q722c respectively. Why the circuit construction of V3 and that of H3 differs is because the required frequency characteristics differ from each other. The wave detecting circuit of H3 has superior frequency characteristics but requires many more number of parts. The wave detecting circuit of V3 has a simple circuit construction but has a demerit in the frequency characteristics, and causes a waveform distortion if it processes the H3.

2-11. Convergence Adjusting Circuit

The convergence adjusting circuit is structured by using 18 pieces of DAC8840 as explained in the preceding item 2-9. The relation between the parts of DAC and the circuit is as listed in table 10-2.

Table 10-2

Q729, Q730, Q731	Red vertical convergence adjustment circuit
Q732, Q733, Q734	Green vertical convergence adjustment circuit
Q735, Q736, Q737	Blue vertical convergence adjustment circuit
Q738, Q739, Q740	Red horizontal convergence adjustment circuit
Q741, Q742, Q743	Green horizontal convergence adjustment circuit
Q744, Q745, Q746	Blue horizontal convergence adjustment circuit

The output voltages of respective DACs are input into the mixer circuit for their amplification, that is structured of the OP amp. (Q747 to Q752) via the resistor. The output voltage of mixer circuit is supplied to the convergence output circuit (FOCUS/CONV-OUT PC board).

The output voltage waveform of mixer circuit varies with the adjustment method of convergence. Therefore, it is difficult to clearly indicate a standard waveform during the service, but at least the case where the signal voltage isn't output or the case where the direct current is output needs to be judged to be abnormal. The figures 4 to 23 and the symbols H1, H2, V1 and V2 are described inside ⇨ mark of DAC8840 in the circuit diagram. (These figures and symbols are described in the similar way even in various signal generation circuits and signal dividing circuits that have been explained in this manual).

The relation among these figures and symbols and the movement in the screen when adjusting the convergence is as listed in the below description.

The figures 4 to 23 coincide with the figures CONV4 to CONV23 described in the adjustment edition of installation manual. In other words, the figures show the respective locations on the screen. The relation between the H1, H2, V1 and V2 and the remote control adjusting keys are shown in table 10-3.

For information, the center position adjusting circuit and the linearity distortion 1 (Linearity) adjusting circuit reside on the DEF PC board and H-OUT PC board.

Table 10-3

Symbol	Adjusting key	Contents to be adjusted	Adjusting key	Contents to be adjusted
H1		TILT		C. SIZE
H2	▲	BOW	◀ ▶	C. LIN
V1		C. SIZE		TILT
V2	▼	C. LIN		BOW

2-12. DAC Control Circuit

19 pieces of DAC (Q728 to Q746) are controlled by the Clock (DAC), Serial Data (DAD), MUTE and A0 to A3 and G0 and G1 supplied from the control circuit (CONTROL P.C. Board). The Clock (DAC) is applied to the CLK input terminal of DAC and the Serial Data (DAD) is applied to the SDI input terminal of DAC. The A0 to A3 and G0 and G1 are the code signals for selecting the controlling DAC, and supplied to the LD input terminals of respective DACs after decoded by the decoder IC (Q727, Q726). The decode signals LD20 to LD23 output to pins 5 to 8 of Q726 are supplied to the respective circuit boards for controlling the DAC on the other circuit boards.

The signal applied to the MUTE terminal of respective DACs is for temporarily resetting the DAC when switching on the power source and changing over the input source so that the signal may not be output. Thereby, the excessive load is prevented from applied on the convergence output circuit.

2-13. Buffer Circuit

This circuit supplies the H1, H2, V1 and V2 to the RGB circuit (RGB P.W. circuit board) and FOCUS OUT. circuit (FOCUS/CONV- OUT P.W. circuit board) by the OP amp. Q764a, Q764b, Q765a, and Q765b.

2-14. Focus Circuit

A part of focus circuits resided in the CONV/FOCUS PC board, so this circuit is to be explained. This circuit block supplies the focus correction current to the static focus coil residing in the focus yoke. The static focus coil corrects the static focus and corrects the vertical dynamic focus. The vertical parabolic wave voltage V2 is divided by the RP66 and RP67 and applied to pin 5 of OP amp. QF01, and the direct current voltage is applied to pin 6 from the – 5V power source. The voltage mixing two voltages is output to the output terminal of QF01, and is supplied to the respective circuits of red, green and blue. The vertical dynamic focus is corrected by the voltage of V2 constituent contained in this output voltage.

The parts of red circuit is quoted and explained hereunder out of the red, green and blue circuits. The signal voltage output from QF01 and the static focus adjusting voltage RED of red supplied from the control circuit are mixed by the OP amp. QF02b for its amplification. The adjusting voltage RED varies within the range from 0V to +5V. For keeping the balance with this change range, the direct current constituent is mixed to the voltage output from QF01.

The voltage output from QF02b is applied to pin 3 of QF02a, and the output voltage of QF02a is supplied to the static focus coil via the buffer transistors QF03 and QF04. The current flowing to the static focus coil flows into the GND through the RF11. By this current, the voltage of same waveform as the current waveform can be obtained to both the ends of RF11. The current of same waveform as that of output terminal voltage of QF02b can be flown to the static focus coil by feeding this voltage back to pin 2 of QF02a.

SECTION XI
CONVERGENCE OUTPUT CIRCUIT
(FOCUS/CONV-OUT PC BOARD)

1. OUTLINE

The convergence output circuit is the circuit for amplifying the convergence adjusting signal supplied from the convergence circuit and for supplying the current to correct the picture distortion and convergence to the convergence yoke.

Since the circuit consists of a simple discrete components and uses a sufficient high power transistor to the final output stage, a high reliability is obtained.

2. DESCRIPTION OF OPERATION

The circuit to give the bias to the entire convergence output circuit is composed of QF10, DF07, RF30, RF31 and RF32. The current of 5 mA (Typ.) flows to RF32, develops the voltage of 0.5 V(Typ.) at both ends. The voltage is supplied to 6 systems of convergence output circuit by the current mirror circuit. The QF01 is short-circuited between the collector and the base, so it functions in the same way as a diode and functions to stabilize the temperature against its variation.

The convergence output circuit has 6 systems in total because the horizontal and vertical circuits for red, green and blue are provided. They have quite the same circuit components, so the vertical circuit for green (GV) is quoted here for the explanation.

Q602 is a twin transistor. The left side transistor shown in the circuit diagram is called as Q602L, while the right side transistor as Q602R to explain the operation. The convergence adjusting signal for GV is input to the base of Q602L from the CONV/FOCUS P.W. circuit board.

The signal current amplified by the Q602L is transmitted to the pre-drive circuit consisting of Q626 and Q614 by the current mirror circuit consisting of Q620, Q626, R628 and R622, and amplified further. The output signal of pre-drive circuit is applied to the base of final output transistors Q650 and Q644 via the drive circuit consisting of Q638 and Q632. The drive circuit and the output transistor should be considered as the emitter follower circuit.

The vertical coil of convergence yoke is connected as a load to the emitter of output transistor, and the convergence correction current flowing to the load flows into the GND through R670. At this time, the voltage of same waveform as the convergence correction current develops at R670, and the voltage is fed back to the base of Q602R. Here, the polarity of signal voltage which is input to the Q602L and then output is described as follows:

(1) For example, suppose that the input voltage goes up and the base voltage of Q602L goes up.

(2) The collector current of Q602L increases and the current of Q620 also increases.

(3) The collector current of Q626 is increased by the current mirror operation.

At this time, since the collector current of Q614 becomes a constant current of 6.7 mA (Typ.) by the current mirror operation from the bias current previously mentioned, the increment current of the collector of Q626 flows to R694.

(4) As a result, the collector voltage of Q626 goes up, and the output voltage is increased by the emitter follower circuit.

(5) The load current increases, the voltage generating to R670 goes up, and the voltage fed back to the base of Q602R goes up.

(6) The collector current of Q602R must increase.

However, since the total current adding the collector currents of Q602L and Q602R becomes a constant current of 5 mA (Typ.) by the current mirror operation from the bias circuit, the collector current of two transistors cannot increase at the same time.

The circuit operation described above is called the negative feed back loop. As a result, the circuit balances the operation so that the base voltage of Q602L equals to that of Q602R. That is to say, the input voltage waveform and the load current waveform become similar.

As the load of convergence output circuit mainly includes the inductance component, the input voltage waveform and the output voltage waveform observed at the emitters of Q650 and Q644 don't become similar. Since the voltage necessary to flow the current to the inductance component becomes the differentiated value of current, the voltage V_O of square waveform is required when flowing, for example, the current I_O of saw tooth waveform shown in Fig. 11-1.

In the convergence output circuit where the voltage of waveform quite different from the input voltage waveform must be output in this way, a large amount of voltage amplification gain and a wide frequency band are necessary.

The convergence output circuit composes the feedback loop as explained above. Therefore, if any of the parts may be defective, the feedback loop is disconnected, and the circuit can not work normally any longer. For this reason, it is difficult to specify the defective part(s) when the circuit is defective.

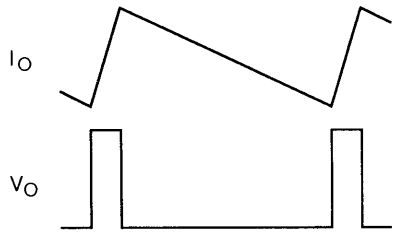


Fig. 11-1

SECTION XII
HIGH VOLTAGE CIRCUIT

1. HIGH VOLTAGE OSCILLATION CIRCUIT

This is the circuit outputting the pulse for driving the high voltage output, and is laid out in the PC board PB6307-5 in the P-RECT/HV PC board.

The source of 3.58 MHz is output from pin 2 of QB21 by the oscillation circuit inserted the crystal oscillation circuit to the both ends (pins 1 and 2) of inverter QB21. The output signal is input to pin 13 of QB21 and the inverted pulse is ouput from pin 12 of QB21. This pulse is input into the clock terminal pin 1 of pre-settable-counter QB22, and frequency-divides it into the value preset to QB22.

The frequency-divided signal is output from pin 14 of QB22 and input into pin 3 of flip flop QB23. Since QB23 is set with the pulse input to pin 3 and outputs the square wave repeating Hi/Lo from pin 5, the pulse of duty 1 : 1 which frequency divided into 1/2 frequency of pulse input to pin 3 is output to pin 5. The pulse whose polarity is inverted against pin 5 is output to pin 6.

2. OUTPUT CIRCUIT

The pulse from the oscillation circuit is input to the base of QB05 via RB08, QB05 performs the switching operation, and drives QB06. QB06 performs the switching operation similarly and drives the drive transformer TB02. The output transistor QB03 is driven with the pulse output to the secondary side of TB02, and performs the switching operation.

When QB03 is on, the primary side current of TB98 increases, and when QB03 is turned off, its current charges CB11 and CB12, and the oscillation pulse is generated to both the ends of CB11. The voltage which raised its pulse on the secondary side of TB98 is rectified with the diode incorporated into TB98, and outputs the high voltage (30.5 kV) as a direct current.

The circuit structured of QB07, QB08, QB04, CB08, CB09 and TB99 performs the similar operation but its phase is inverted as compared with the above mentioned circuit.

3. HIGH VOLTAGE CONTROL CIRCUIT

This circuit controls the power voltage supplied to the high voltage output circuit and stabilizes the output high voltage. This circuit is laid out in the PC board (PB6307-4) in the P-RECT/HV PC board.

The output high voltage is divided into 1/3444 voltage with the internal resistance of the high voltage capacitor arranged in the MOTHER-3 PC board (PB6317-3), and fed back to pin 1 of PB14. The voltage whose impedance is converted with QB30a and divided with PB51 to 53 is input into pin 3 of QB30b. QB30b compares its voltage with the voltage which divided the reference voltage at both ends of DB30 with RB57 and RB58, amplifies its difference, and inputs it into the base of QB31 via DB32.

When the high voltage becomes higher, the voltage fed back to pin 5 of QB30a also becomes high, its output voltage (pin 7 of QB30a) becomes high, the voltage of pin 3 of QB30b develops high, that of pin 1 of QB30b also develops high and the collector voltage of QB31 develops low. Therefore, the emitter voltages of QB32 and QB33 develop low and the base and emitter voltages of QB01 and QB02 develop low respectively.

Therefore, since the power supply voltage input to TB98 and TB99 develops low, the high voltage output voltage falls down. Because the inverse operation is obtained if the high voltage develops low, the high voltage output voltage is stabilized to a constant state.

4. X-RAY PROTECTION CIRCUIT

When the high voltage abnormally goes up or the high voltage current abnormally increases, the X-ray amount released from the projection tube increases. To prevent this, the power supply of unit is turned off for its protection when the high voltage or the high voltage current exceeds the specified value. Since the high voltage control voltage is proportional to both the high voltage and high voltage current, the high voltage control voltage is detected to perform the protection operation.

The high voltage control voltage is input to the base of QB14 via DB14, RB27 and RB28, and a constant voltage determined by DB17 is input to the emitter of QB14.

Therefore, QB14 operates as the comparator, and when the high voltage control voltage exceeds the specified level, QB14 is turned on, QB15 is also turned on, and DB18, DB19 and DB20 are turned on, outputting the signal to the P-RECT/HV circuit via RB39 and turning off the power supply of unit.

The operation of X-ray protection circuit can be confirmed by short-circuiting the R terminal (PB51) and the X terminal (PB50). When the R terminal (PB51) and the X terminal (PB50) are short-circuited, QB24 and QB25 are turned on, shut off the drive pulse to the output circuit and stop the operation of output circuit.

Thereby, the high voltage falls down, the high voltage control circuit raises the high voltage, the anode voltage of DB01 goes up and the X-ray protection circuit operates.

5. HV STOP CIRCUIT

The deflection is temporarily stopped when changing the constant of horizontal deflection, but in combination with its operation, during that period, high voltage is dropped to prevent the fluorescent burning of projection cathode ray tube. The deflection stop signal (H. STOP) which developos Lo when stopping the deflection is input to pin 10 of PB12 and then input to pin 5 of the inverter QB21 via RB45. The logically inverted signal (HV. STOP) of H. STOP is output to pin 6 of QB21, and is output from pin 5 of PB12 via DB28. The signal is supplied to the base of QB34 via RB19 from pin 7 of PB13, and when the deflection is stopped, QB34 is turned on, and both-end voltage of CB41 is discharged via RB18.

Therefore, the emitter voltage of QB35 falls down and lowers the base voltage of QB32 via DB35. Thereby the high voltage control voltage falls down and the high voltage also falls down.

Further, the output of pin 6 of QB21 is input to pin 11 of QB21 via DA28, and the logical inverted signal is output from pin 10. The signal is input to pin 9 of QB21, logically inverted, and output to pin 8. The signal drives QB24 and QB25 via DA26, R-terminal and RB41 and RB42. When the H.STOP signal becomes Lo, the R terminal becomes Hi, QB24 and QB25 are turned on and shut off the drive pulse to the output circuit and stop the operation of output circuit.

Similarly when the power supply voltage of the video circuit is not supplied, the operation of high voltage output circuit is stopped.

When the power supply of the video circuit is not supplied, an excessive current flows to the projection tube, and hence the projection tube may be damaged burning down. In this case, stopping the operation of high voltage prevents form the damage.

The power supply of the video circuit is input into pin 4 of PB12, and input into pin 3 of inverter QB21 via RB64, RB65 and RB22.

When the voltage is low, pin 4 of QB21 outputs Hi, DB 27 is turned on, and operates similarly during the operation of above mentioned H. STOP.

When these protection circuits operate, the operation of X-ray protection circuit is temporarily stopped by turning on QB16 via RB37.

6. SCREEN VOLTAGE GENERATION CIRCUIT

The output pulse is rectified by DB94 to DB97 and DB87 to DB90, smoothed by CB86 into the formation of direct current voltage, and a bias is applied to RB88 and RB89 by RB83 to RB87 using the voltage as the power source, and is supplied to the base of QB99. Therefore the emitter potential of QB99 is stabilized to a constant voltage. The stabilized voltage is adjusted by the variable resister RB78, RB79 and RB80 to adjust the screen voltages of R, G, B and is supplied to the screen electrode of projection tube.

7. ABL VOLTAGE GENERATION CIRCUIT

The high voltage current is supplied to the anode of projection tube via RB91, RB94 and TB98 or via RB90, RB95 and TB99 from the +125V power source.

Therefore, the circuit detects the voltage drop by RB91 and RB94 or RB90 and RB95 and limits the high voltage current. When the high voltage current has increased, the voltage drop by RB91/RB94 and RB90/RB95 becomes larger, and the voltage smoothed by RB93 and CB80 and also the voltage smoothed by RB92 and CB81 fall down respectively. The voltage is output to the video circuit from pin 3 of PB85.

Since the video circuit operates to darken the video image when the voltage falls down, it operates so as to limit the high voltage current. DB92 and DB93 are inserted so that the high voltage current may not get deviated to any of TB98 and TB99.

8. HIGH VOLTAGE LIMITATION CIRCUIT

The high voltage output is divided in voltage into 1/3444 by the resistance inside the high voltage capacitor CB98 of HV.CAP-2 PC board (PB6313-3), fed back to pin 1 of PB11 of PRO/ERR PC board (PB6307-4) from pin 1 of PB90, divided in voltage by RB21 and RB23 via the buffer of QB10a, and input to the non-inverted input terminal.

Since the voltage which has divided in resistance the constant voltage at both ends of DB10 with RB24 and RB25 is input to the non-inverted input terminal of QB10b, QB10b operates as a comparator, and outputs Hi when the non-inverted input terminal voltage becomes higher than the inverted input terminal voltage.

That is to say, when the high voltage becomes high, QB10b outputs Hi, the DB12 and DB11 are turned on and turn on QB34 via RB26. Thereafter, the circuit operates in the same manner as the operation of previously mentioned HV. STOP circuit, and the high voltage does not go up higher than a constant level to lower the high voltage.

SECTION XIII
H-OUT CIRCUIT

1. HORIZONTAL SIZE CIRCUIT

The amplitude control circuit is the circuit to obtain a constant amplitude without depending on the deflection frequency and to adjust the size in horizontal direction of input image.

The F/V conversion voltage proportional to the deflection frequency is input to pin 5 of PA03. The F/V conversion voltage is input to pin 3 of QA21 via the buffer composed of pins 5 to 7 of QA20 and via RA80. The adjustment voltage of picture size input via RA81 into pin 3 and the F/V conversion voltage are added at QA21, and amplitude adjustment voltage is output from pin 1. The amplitude adjustment voltage is input to pin 3 of QA37 from pin 1 via the buffer composed of pins 1 to 3 of QA23. At that time, the triangle wave voltage synchronizing with the deflection frequency is superimposed on the amplitude adjustment voltage via CA41 from QA24. QA37 is the comparator for comparing the amplitude adjustment voltage input to pin 3 with the feedback voltage from output input to pin 2. When the voltage of pin 3 of QA37 is higher than that of pin 2, the output of pin 7 of QA37 develops Lo, and in the reverse case, the pin develops Hi. Because the triangle wave voltage synchronizing with the deflection frequency is superimposed as described above on pin 3 of QA37, the output voltage of pin 7 of QA37 becomes the square wave voltage synchronizing with the deflection frequency, and its duty becomes narrow when the direct current level of pin 3 voltage is higher than pin 2 voltage, and becomes wider in the reverse case. QA25 performs the switching operation with the square wave output from pin 7 of QA37, and the polarity of square wave is reversed, and drives the drive transformer TA01 via the follower composed of QA31 and QA32.

The square wave of the same polarity as the primary side is output to the secondary side of TA01, and drives QA10 gate.

Therefore QA10 performs the switching operation with the square wave input to the gate, and interrupts the power source to the coil LA08. The current flowing to LA08 rises gradually while QA10 is turned on, and DA01 is tuned on when QA10 is turned off and then the current flow in LA08 gradually decreases.

Therefore, the alternating current square wave voltage whose upper limit is clamped to the power supply voltage is developed at the cathode of DA01. The direct current voltage whose negative voltage portion is rectified with DA01 is output to CA32.

The direct current voltage of CA32 decreases when the duty of square wave voltage of DA01 cathode becomes narrow and increases when the duty becomes wider. The direct current voltage is inverted and amplified with the amplifier composed of pins 1 to 3 of QA38 via RD65, RA52 and RD04, via the buffer composed of pins 5 to 7 of QA38 and via RQ08 and RD09, and fed back to pin 2 of QA37. The direct current voltage output to CA32 of above construction becomes the negative direct current voltage proportional to the amplitude control voltage input to pin 3 of QA37. In other words, the direct current voltage of CA32 becomes the negative voltage proportional to the deflection frequency, and the deflection output circuit can obtain a constant amplitude even if the deflection frequency should change by adopting this voltage as the power supply.

Further, the adjustment voltage of picture size is input to pin 3 of QA21 via RA81. This voltage adds a constant direct current adjustment voltage with RA76 and RA77 without depending on the deflection frequency input to pins 3 and 4 of PA03, is output from pin 1 of QA20 and is input to pin 11 of multiplier QA28. Because the F/V conversion voltage is input to pin 10 of QA28, its multiplied result is output from pin 9 of QA28.

Therefore, the direct current voltage whose variable width differs due to the deflection frequency is output to pin 9 of QA28. In short, even if the changing width of pins 3 and 4 voltages of PA03 should be constant without depending on the frequency, the F/V conversion voltage is low when the deflection frequency is low, and the changing width of output voltage of pin 9 of QA28 becomes small, so it makes it possible to obtain the picture size adjustment of constant variable width without depending on the deflection frequency. Further, the amplitude adjustment voltage is output to the convergence circuit from pin 4 of PA13 via the inverse amplifier composed of pins 1 to 3 of QA18 and via RD63.

TA01 is not driven when the pulse to drive QA10 becomes the direct current. To prevent this, the circuit composed of QA30 and QA33 is provided and the square wave to drive the horizontal output is input to the base of QA30 via RA99, and then the inverted square wave is output to the collector of QA30. The pulse of narrow width which differentiated the square wave with the CA48 and RD05 and RD06 is input to the base of QA33. QA33 is turned on with the fall of square wave to drive the horizontal output.

For this reason, the drive of TA01 doesn't become the direct current but surely becomes the square wave.

The current when QA10 is turned on flows via LA08 and via RA70 and RA71. Its current is converted into the voltage with RA70 and RA71, and when the voltage becomes a level higher than a certain value, DA15 is turned on with QA34 also turned on, and the current flowing to QA10 is prevented from flowing excessively in order to stop the drive of TA01.

2. KEYSTONE AND PINCUSHION DISTORTION CORRECTION CIRCUIT

The keystone and pincushion distortion are corrected by superimposing the vertical period saw tooth wave and parabolic wave voltage to the above mentioned amplitude adjustment voltage.

The vertical period saw tooth wave voltage is input to pin 3 of PA13, and the vertical period parabolic wave voltage is input to pin 2 of PA13, both the voltages are added with RA84 and RA85, amplified and inverted by QA22, output from pin 7 of QA22 and input to pin 4 of multiplier QA28. Because the amplitude control voltage is input to pin 5 of QA28, the keystone and pincushion distortion correction voltages of amplitude proportional to the amplitude and frequency are output to pin 6 of QA28, its correction voltage is input to pin 5 of QA23, amplified by the non-inverted amplifier composed of pins 5 to 7 of QA23, the direct current is prevented with the CA19 from pin 7 of QA23, and input to the cathode of DA02. Since the anode of DA02 is the amplitude control voltage, the keystone and pincushion distortion correction voltage becomes the voltage whose bottom is clamped by the amplitude control voltage, and input to pin 5 of QA18 via RA57.

Since the feedback voltage from the output is input to pin 6 of QA18, QA18 drives the follower consisting of QA11 to QA16 so that the voltage equal to the voltage input to pin 5 may be fed back to pin 6. For this reason, the keystone and pincushion distortion correction voltage whose bottom is clamped to the amplitude control voltage is output to the emitter of QA12, and is supplied to the deflection output circuit via RA62 to RA65.

The dynamic range portion of keystone/pincushion distortion correction voltage with the amplitude control voltage as its center is required as the power source of QA18, so the secondary side direct current voltage level of switching transformer TA05 (pin 8 of TA05) driven by QA19 is biased to the foregoing amplitude control voltage.

3. H.STOP CIRCUIT

The F/V conversion voltage proportional to the deflection frequency is output from pin 7 of QA20 via the buffer QA20 as described above, input to pin 3 of QA55 via RD79, non-inverted amplified by QA55, and input to the inverted input terminal (pin 2) of QA54 from pin 1 of QA55. The voltage which is divided by RD66 and RD67 is input to non-inverted input terminal (pin 3). QA54 operates as a comparator, outputs the Hi when pin 2 voltage is higher than pin 3 voltage and develops Lo when the former voltage of lower. Usually divided by RD66 and RD67, pin 3 is lower than pin 2, and the output of QA54 (pin 1) develops Lo. When the F/V conversion voltage lowers, pin 2 voltage also lowers following the drop voltage. But pin 3 voltage falls down in late by discharge time constant portion, the output of QA54 develop Hi during that period, DA30 is turned on to turn on QA57, QA35 is turned off, the collector of QA35 develops Hi, DA16 is turned on, and QA34 is turned on, stops the drive of amplitude control circuit and lowers the amplitude control voltage. At the same time, DA34 is turned on via RD75 and QA56 is turned on and discharges the voltage of CA99. Pin 7 voltage of QA55 falls down following the discharging, pin 3 voltage of QA23 also rises gradually, and the amplitude control voltage rises slowly to reach the normal voltage. When pin 3 voltage of QA54 becomes lower than pin 2 voltage, this operation is released and becomes the usual operation. Namely, a drive is given to the amplitude control circuit, QA56 is turned off, and CA99 charges it gradually up to the F/V conversion voltage via the RD77. Because pin 7 of QA55 goes up following it, pin 3 voltage of QA23 also gradually goes up, and the amplitude control voltage slowly rises and resets at the usual voltage. The direct current voltage which divided the power supply voltage with RD68 and RD69 is input to pin 5 of QA54, and goes up in proportion to the rise of power supply when the power supply is switched on. Since pin 6 of QA54 slowly goes up with the time constant of RD70 and CA98, the output (pin 7) voltage of QA54 outputs the Hi until pin 6 voltage becomes equal to pin 5 voltage, and DA31 is turned on and operates similarly when the F/V conversion voltage has fallen down. Because the signal which develops Hi while switching the constant of DEF circuit from pin 7 of PA03 is input to the base of QA35 via RD71 and RD14, it operates similarly when this signal develops Hi.

4. DRIVE CIRCUIT

The horizontal output transistor QA53 is driven via the drive transformers TA02 and TA03. TA02 and TA03 are driven by the drive transistor QA43, and in the timing that QA53 is turned on when QA43 is turned off. DA22 and DA24 are turned on when QA43 is turned on, QA49 and QA50 are turned off, and when QA43 is turned off, QA49 and QA50 are biased from RD64 and RD50 and are turned on. The drive amount of QA53 is proportional to the power supply voltage applied to the drive transformer. The average of square wave applied to pin 1 of TA02 and TA03 is charged in CA65, and its direct current voltage becomes the power supply of drive transformer. When QA43 is turned on, the primary side of TA02 and TA03 is driven via RD53 and RD54 from CA65. The drive current is detected by RD53 and RD54, amplified by QA52 and is input to pin 3 of QA45. Pins 1 to 3 of QA45 are the buffers, and the direct current voltage of the peak output is charged to CA60 via DA37. The voltage is input to the non-inverted input of QA44. The voltage dividing the voltage with RD46, RD45, RD35 and RD54, which rectified the output pulse, is input to the non-inverted input of QA44, and QA44 compares them with each other and outputs the signal controlling the drive power supply from pin 7. The output pulse is proportional to collector current Icp of output transistor, and when the Icp increases, pin 6 voltage of QA44 goes up, pin 7 voltage of QA44 goes down, the collector of QA48 goes up, the base voltage of QA46 goes up, the emitter voltage also goes up, the base voltage of QA47 goes up and the emitter voltage of QA47 goes up. Therefore, since the power supply of drive goes up, the base current of QA53 is increased. The reverse operation is obtained when the collector current of QA53 decreased, so the current meeting the collector current of QA53 is flown to the base.

5. CENTERING ADJUSTMENT CIRCUIT

The centering circuit is the circuit to move the raster in horizontal direction. The deflection current is blocked in direct current by CA76, CA77 and CA78, only the alternating current flows to the deflection coil, and the direct current is supplied from the constant current circuit connected to one end of respective direct current block condensers. When this should be explained with reference to the R circuit, the centering adjustment voltage is input to pins 6 and 7 of PA02, added with the RA11 and RA12, and then input to the non-inverted input terminal of QA07.

The output of QA07 is supplied as the direct current via RA20 to one end of CA78 via the emitter follower composed of QA01 and QA04. Because this output current is detected by RA16, inverted into the voltage and input to the inverted input of QA07, QA07 operates as the constant current circuit supplying to the output circuit the current identical to the input centering adjustment voltage. The centering circuits other than the R operate in the similar manner.

6. LINEARITY ADJUSTMENT CIRCUIT

With the over-saturation coil LA13 inserted in series with the deflection coil, this circuit adjusts the linearity. The over-saturation coil LA13 is to change the output side (pins 4 and 6) inductance with the current flown to the bias side (pins 2 and 9), input to pin 5 of QA58 the voltage which divided with RD96 and RD97 the linearity adjustment voltage input to pin 8 of PA03, and flows the bias current to LA13 via the follower composed of QA59 and QA60 from the output (pin 1) of QA58 input to pin 3 of QA58 via the buffer. The current is detected by RQ01 and fed back to the inverted input (pin 2) of QA58 via the RD99 as the voltage. Therefore, the direct current proportional to the linearity adjustment voltage flows as the bias current of LA13, and the output side inductance of LA13 varies according to it, the linearity of deflection current can be adjusted.

7. R, G AND B AMPLITUDE VARIATION ADJUSTMENT

The deflection output circuit drives three deflection coils of R, G and B parallely, but the amplitudes of R, G and B don't become equal due to the scattering of deflection sensibility, so the variable coils LA09, LA10 and LA11 are inserted in series with the deflection coils.

8. BLANKING PULSE GENERATION CIRCUIT

This circuit converts into the negative polarity with TA04 the pulse for the output circuit to output to the blanking time, inputs the pulse into the base of QA36 via CA50 and RD19 from its secondary side pin 14, and outputs the positive polarity pulse output to the collector of QA36 to the video circuit as the blanking pulse and outputs it to the horizontal synchronous circuit as the AFC pulse. Because the blanking pulse of output circuit uses the negative polarity and blocks the direct current by CA50, the blanking pulse develops Hi when the pulse of output circuit isn't output, and protects the burning of projection tube by blanking the entire period of image.

9. PROTECTION CIRCUIT

The blanking pulse of output circuit is rectified by RD47, D21 and CA64 from pin 12 of TA04 into the formation of direct current voltage, and supplied to the base of QA51 via RD49. When the deflection stops, the direct current voltages at both ends of CA64 fall down, QA51 is turned off, both ends voltages of CA46 ascend, and when DA13 is turned on, DA12 is turned on and outputs the protection signal to the power supply and drops the power supply of set. Because the connection to the collector of QA35 is made to the base of QA51 via RD84 and DA38, this protection operation is prevented from performed during the H.STOP operation.

TOSHIBA AMERICA CONSUMER PRODUCTS, INC.
NATIONAL SERVICE DIVISION
1420-B TOSHIBA DRIVE
LEBANON, TENNESSEE 37087